Integrated Device Technology, Inc.

FAST CMOS OCTAL BUFFER/LINE DRIVER

IDT54/74FCT240T/AT/CT
IDT54/74FCT241T/AT/CT
IDT54/74FCT244T/AT/CT
IDT54/74FCT540T/AT/CT
IDT54/74FCT541T/AT/CT

FEATURES:

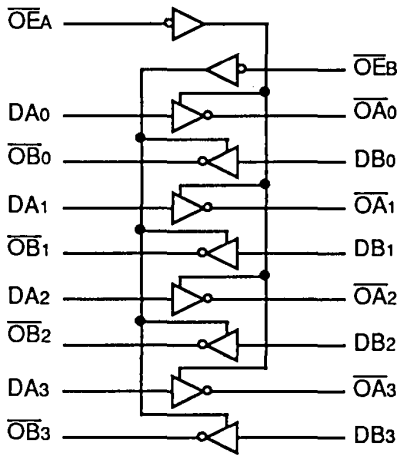
- IDT54/74FCT240T/241T/244T/540T/541T equivalent to FAST™ speed and drive
- **IDT54/74FCT240AT/241AT/244AT/540AT/541AT 25% faster than FAST™**
- **IDT54/74FCT240CT/241CT/244CT/540CT/541CT up to 55% faster than FAST™**
- True TTL input and output compatible
  - — V_{OH} = 3.3V (typ.)
  - — V_{OL} = 0.3V (typ.)
- I_{OL} = 64mA (commercial) and 48mA (military)
- CMOS power levels (1mW typ. static)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Meets or exceeds JEDEC Standard 18 specifications

DESCRIPTION:

The IDT octal buffer/line drivers are built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT240T/AT/CT, IDT54/74FCT241T/AT/CT and IDT54/74FCT244T/AT/CT are designed to be employed as memory and address drivers, clock drivers and bus-oriented transmitter/receivers which provide improved board density.

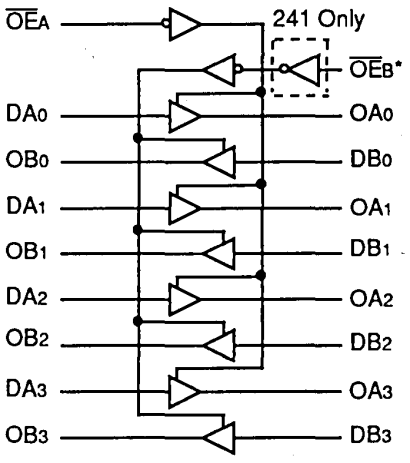
The IDT54/74FCT540T/AT/CT and IDT54/74FCT541T/AT/CT are similar in function to the IDT54/74FCT240T/AT/CT and IDT54/74FCT244T/AT/CT, respectively, except that the inputs and outputs are on opposite sides of the package. This pinout arrangement makes these devices especially useful as output ports for microprocessors and as backplane drivers, allowing ease of layout and greater board density.

FUNCTIONAL BLOCK DIAGRAMS



IDT54/74FCT240T

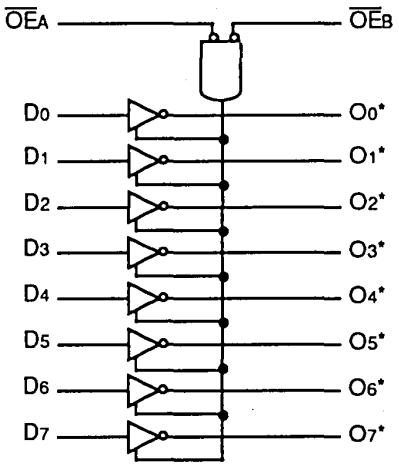
2565 cnv* 01



IDT54/74FCT241T/244T

*$\overline{OE}_B$ for 241T, $\overline{OE}_B$ for 244T

2565 cnv* 02



IDT54/74FCT540T/541T

*Logic diagram shown for 'FCT540T. 'FCT541T is the non-inverting option.

2565 cnv* 03

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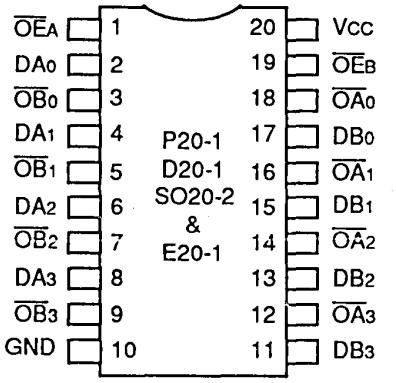
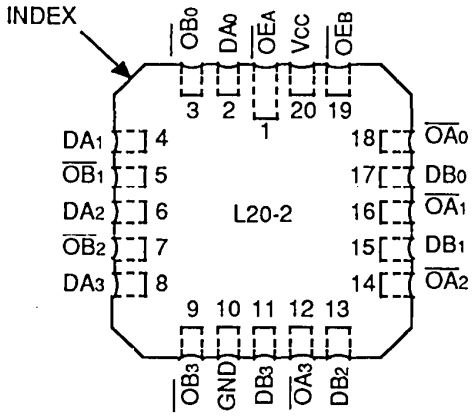
CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS

IDT54/74FCT240T



DIP/SOIC/CERPACK
TOP VIEW

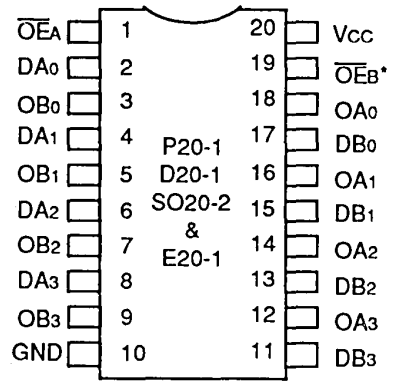


LCC
TOP VIEW

2565cnv* 04

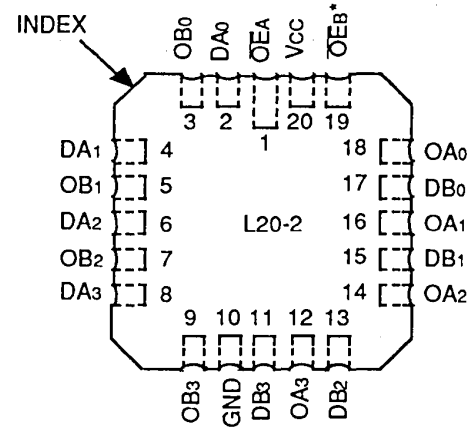
2565cnv* 07

IDT54/74FCT241T/244T



DIP/SOIC/CERPACK
TOP VIEW

*OEB for 241T, $\overline{OE_B}$ for 244T

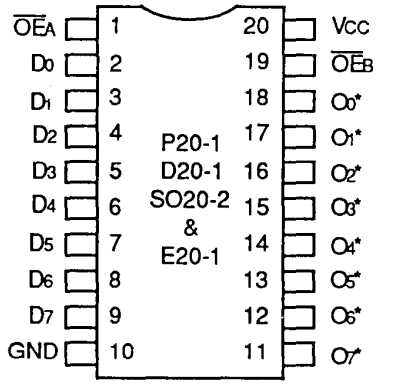


LCC
TOP VIEW

2565cnv* 05

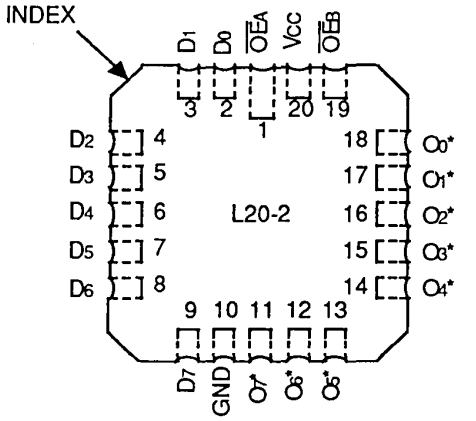
2565cnv* 08

IDT54/74FCT540T/541T



DIP/SOIC/CERPACK
TOP VIEW

*OEB for 241T, OEB for 244T



LCC
TOP VIEW

2565cnv* 06

2565cnv* 09

PIN DESCRIPTION

Pin Names	Description
$\overline{OE_A}$, $\overline{OE_B}$	3-State Output Enable Inputs (Active LOW)
OE_B[1]	3-State Output Enable Input (Active HIGH)
Dxx	Inputs
Oxx	Outputs

NOTES: 2565 tbl 04
1. OE_B for 241 only

FUNCTION TABLE

Inputs[1]				Outputs[1]				
$\overline{OE_A}$	$\overline{OE_B}$	OE_B[2]	D	240	241	244	540	541
L	L	H	L	H	L	L	H	L
L	L	H	H	L	H	H	L	H
H	H	L	X	Z	Z	Z	Z	Z

NOTE: 2565 tbl 05
1. H = High Voltage Level
   X = Don't Care
   L = Low Voltage Level
   Z = High Impedance
2. OE_B for 241 only.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	−0.5 to Vcc	−0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2565 tbl 01
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2565 tbl 02
1. This parameter is measured at characterization but not tested.

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions (1)		Min.	Typ. (2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = 0.5V	—	—	−5	µA
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	10	µA
I_{OZL}			V_O = 0.5V	—	—	−10	µA
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = −18mA		—	−0.7	−1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		−60	−120	−225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −6mA MIL. I_{OH} = −8mA COM'L.	2.4	3.3	—	V
			I_{OH} = −12mA MIL. I_{OH} = −15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.3	0.55	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2565 tbl 03

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE_A}$ = $\overline{OE_B}$ = GND or $\overline{OE_A}$ = GND, OE_B = V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE_A}$ = $\overline{OE_B}$ = GND or $\overline{OE_A}$ = GND, OE_B = V_{CC} One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE_A}$ = $\overline{OE_B}$ = GND or $\overline{OE_A}$ = GND, OE_B = V_{CC} Eight Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	3.2	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	5.2	14.5[5]	

2565 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT240T

Symbol	Parameter	Condition[1]	54/74FCT240T				54/74FCT240AT				54/74FCT240CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay D_N to $\overline{O}_N$	C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	9.0	1.5	4.8	1.5	5.1	1.5	4.3	1.5	4.7	ns
tPZH tPZL	Output Enable Time		1.5	10.0	1.5	10.5	1.5	6.2	1.5	6.5	1.5	5.0	1.5	5.7	ns
tPHZ tPLZ	Output Disable Time		1.5	9.5	1.5	10.0	1.5	5.6	1.5	5.9	1.5	4.5	1.5	4.6	ns

2565 tbl 07

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT241T AND FCT244T

Symbol	Parameter	Condition[1]	54/74FCT241T/244T				54/74FCT241AT/244AT				54/74FCT241CT/244CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay D_N to O_N	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	7.0	1.5	4.8	1.5	5.1	1.5	4.1	1.5	4.6	ns
tPZH tPZL	Output Enable Time		1.5	8.0	1.5	8.5	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.5	ns
tPHZ tPLZ	Output Disable Time		1.5	7.0	1.5	7.5	1.5	5.6	1.5	5.9	1.5	5.2	1.5	5.7	ns

2565 tbl 08

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT540T AND FCT541T

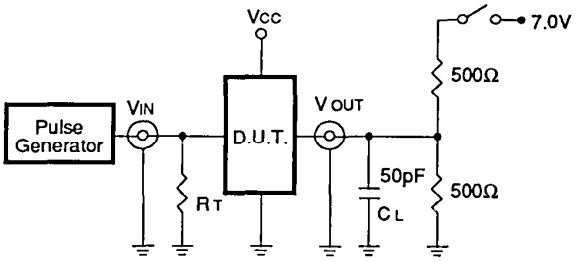
Symbol	Parameter	Condition[1]	54/74FCT540T/541T				54/74FCT540AT/541AT				54/74FCT540CT/541CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay D_N to $\overline{O}_N$ IDT54/74FCT540T	C_L = 50pF R_L = 500Ω	1.5	8.5	1.5	9.5	1.5	4.8	1.5	5.1	1.5	4.3	1.5	4.7	ns
tPLH tPHL	Propagation Delay D_N to O_N IDT54/74FCT541T		1.5	8.0	1.5	9.0	1.5	4.8	1.5	5.1	1.5	4.1	1.5	4.6	ns
tPZH tPZL	Output Enable Time		1.5	10.0	1.5	10.5	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.5	ns
tPHZ tPLZ	Output Disable Time		1.5	9.5	1.5	10.0	1.5	5.6	1.5	5.9	1.5	5.2	1.5	5.7	ns

NOTES:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2565 tbl 09

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

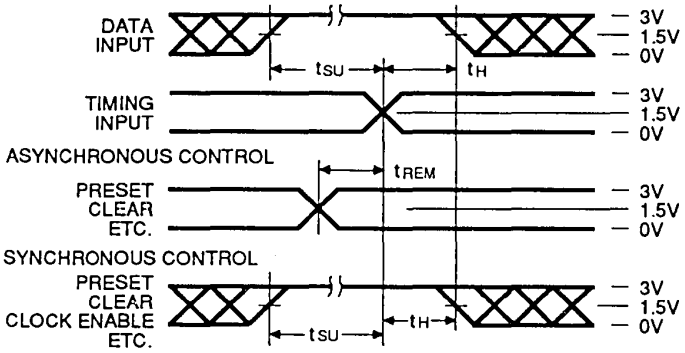
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

2565 tbl 10

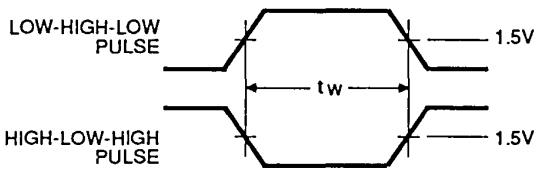
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

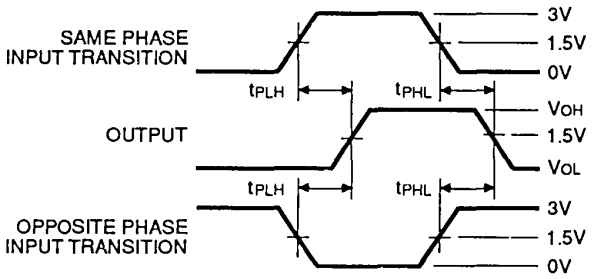
SET-UP, HOLD AND RELEASE TIMES



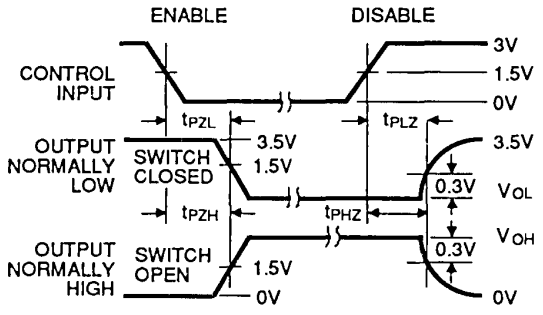
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



2565 drw 10

NOTES

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

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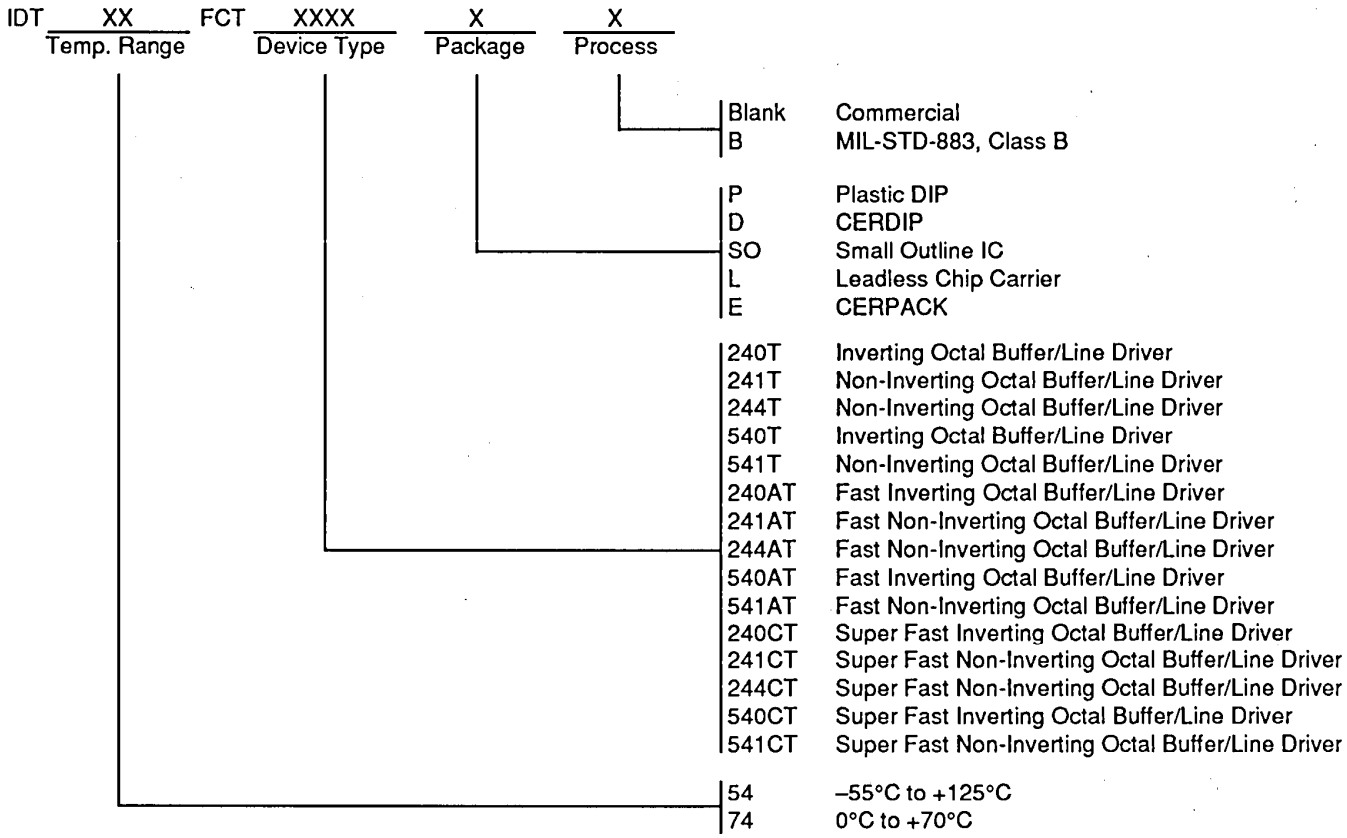
ORDERING INFORMATION



2565 cnv* 15