



Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUS INTERFACE REGISTERS

IDT54/74FCT821AT/BT/CT/DT
IDT54/74FCT823AT/BT/CT/DT
IDT54/74FCT825AT/BT/CT
IDT54/74FCT826AT/BT/CT

FEATURES:

- Fastest CMOS logic family available
- A, B, C and D speed grades with 4.2ns tPD
- Available in DIP, SOIC, SSOP, CERPACK and LCC packages
- High-speed parallel registers with positive edge-triggered D-type flip-flops
- Buffered common Clock Enable (\overline{EN}) and asynchronous Clear input (\overline{CLR})
- IOL = 48mA (commercial) and 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (1mW typ. static)
- True TTL input and output compatibility
 - VOH = 3.3V (typ.)
 - VOL = 0.3V (typ.)
- Substantially lower input current levels than AMD's bipolar Am29800 series (5µA max.)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Meet or exceed JEDEC Standard 18 specifications

DESCRIPTION:

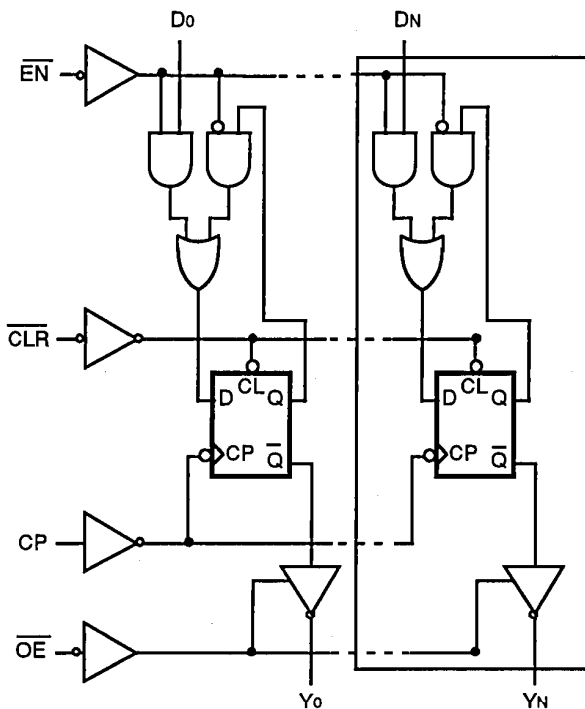
The IDT54/74FCT800 series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT820 series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The IDT54/74FCT821AT/BT/CT/DT are buffered, 10-bit wide versions of the popular '374 function. The IDT54/74FCT823AT/BT/CT/DT are 9-bit wide buffered registers with Clock Enable (\overline{EN}) and Clear (\overline{CLR}) – ideal for parity bus interfacing in high-performance microprogrammed systems. The IDT54/74FCT825AT/BT/CT and IDT54/74FCT826AT/BT/CT are 8-bit buffered registers with all the '823 controls plus multiple enables ($\overline{OE1}$, $\overline{OE2}$, $\overline{OE3}$) to allow multiuser control of the interface, e.g., \overline{CS} , DMA and RD/WR. They are ideal for use as an output port requiring high IOL/IOH.

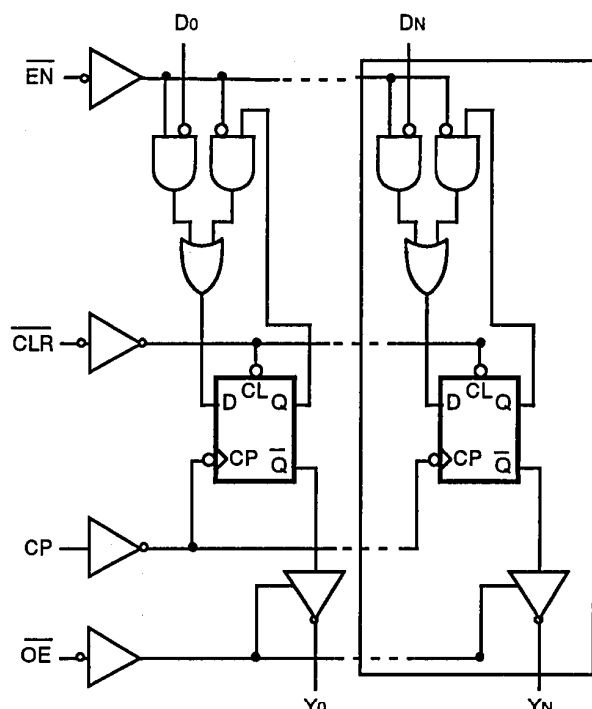
All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in high-impedance state.

FUNCTIONAL BLOCK DIAGRAM

IDT54/74FCT821/823/825T



IDT54/74FCT826T



CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

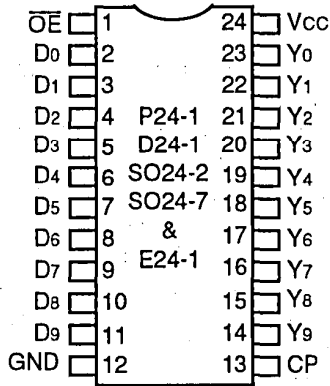
MILITARY AND COMMERCIAL TEMPERATURE RANGES

MAY 1992

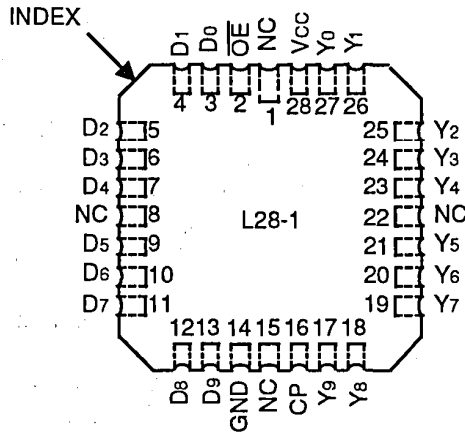
PIN CONFIGURATIONS

LOGIC SYMBOLS

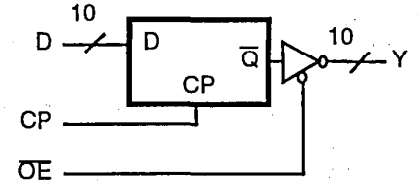
IDT54/74FCT821T 10-BIT REGISTER



DIP/SOIC/SSOP/CERPACK
TOP VIEW

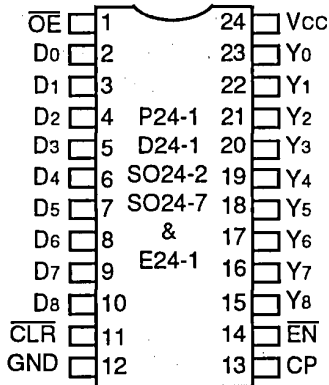


LCC
TOP VIEW

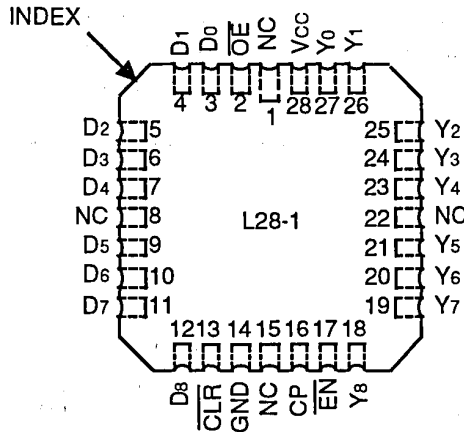


2567 cnv* 02

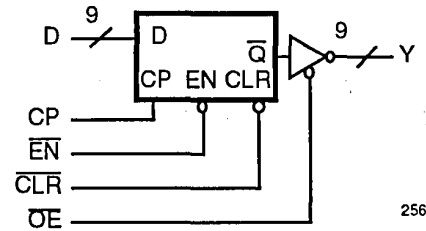
IDT54/74FCT823T 9-BIT REGISTER



DIP/SOIC/SSOP/CERPACK
TOP VIEW

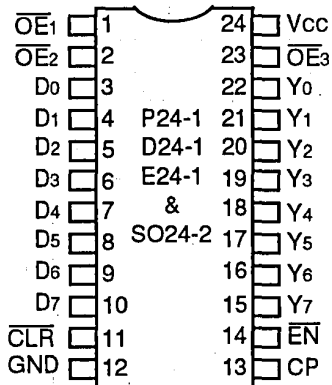


LCC
TOP VIEW

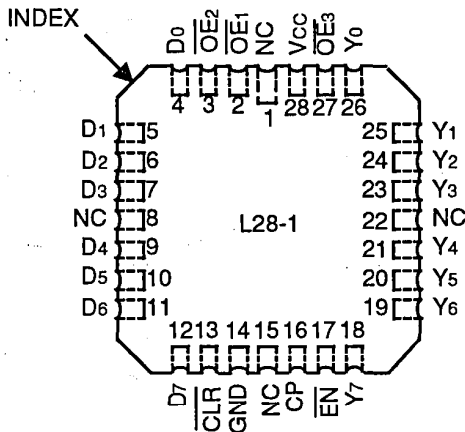


2567 cnv* 03

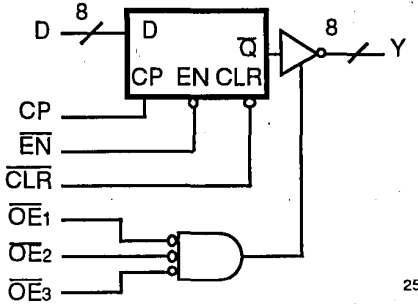
IDT54/74FCT825/826T 8-BIT REGISTER



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW



2567 cnv* 04

PRODUCT SELECTOR GUIDE

	Device		
	10-Bit	9-Bit	8-Bit
Non-inverting	FCT821AT/BT/CT/DT	FCT823AT/BT/CT/DT	FCT825AT/BT/CT
Inverting			FCT826AT/BT/CT

2567 tbl 01

PIN DESCRIPTION

Names	I/O	Description
DI	I	The D flip-flop data inputs.
CLR	I	When the clear input is LOW and OE is LOW, the QI outputs are LOW. When the clear input is HIGH, data can be entered into the register.
CP	I	Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.
YI	O	The register 3-state outputs.
EN	I	Clock Enable. When the clock enable is LOW, data on the DI input is transferred to the QI output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the QI outputs do not change state, regardless of the data or clock input transitions.
OE	I	Output Control. When the OE input is HIGH, the YI outputs are in the high-impedance state. When the OE input is LOW, the TRUE register data is present at the YI outputs.

2567 tbl 02

FUNCTION TABLE⁽¹⁾
IDT54/74FCT821/823/825T

Inputs					Internal/Outputs		Function
OE	CLR	EN	DI	CP	QI	YI	
H	H	L	L	↑	L	Z	High Z
H	H	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

NOTE:

- H = HIGH
L = LOW
X = Don't Care
NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

2567 tbl 03

FUNCTION TABLE⁽¹⁾
IDT54/74FCT826T

Inputs					Internal/Outputs		Function
OE	CLR	EN	DI	CP	QI	YI	
H	H	L	L	↑	H	Z	High Z
H	H	L	H	↑	L	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	H	Z	Load
H	H	L	H	↑	L	Z	
L	H	L	L	↑	H	H	
L	H	L	H	↑	L	L	

NOTE:

- H = HIGH
L = LOW
X = Don't Care
NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

2567 tbl 10

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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC}	-0.5 to V _{CC}	V
T _A	Operating Temperature	0 to +70	-55 to +125	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P _T	Power Dissipation	0.5	0.5	W
I _{OUT}	DC Output Current	120	120	mA

NOTES:

2567 tbl 04

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
- Input and V_{CC} terminals only.
- Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

NOTE:

2567 tbl 05

- This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level	Guaranteed Logic HIGH Level	2.0	—	—	V
V _{IL}	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max. V _I = 2.7V	—	—	5	μA
I _{IL}	Input LOW Current	V _{CC} = Max. V _I = 0.5V	—	—	-5	μA
I _{OZH}	High Impedance Output Current	V _{CC} = Max. V _O = 2.7V	—	—	10	μA
I _{OZL}		V _{CC} = Max. V _O = 0.5V	—	—	-10	μA
I _I	Input HIGH Current	V _{CC} = Max., V _I = V _{CC} (Max.)	—	—	20	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _N = -18mA	—	-0.7	-1.2	V
I _{OS}	Short Circuit Current	V _{CC} = Max. ⁽³⁾ , V _O = GND	-60	-120	-225	mA
V _{OH}	Output HIGH Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL} I _{OH} = -6mA MIL. I _{OH} = -8mA COM'L.	2.4	3.3	—	V
		I _{OH} = -12mA MIL. I _{OH} = -15mA COM'L.	2.0	3.0	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL} I _{OL} = 32mA MIL. I _{OL} = 48mA COM'L.	—	0.3	0.5	V
V _H	Input Hysteresis	—	—	200	—	mV
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max. V _{IN} = GND or V _{CC}	—	0.2	1.5	mA

NOTES:

2567 tbl 06

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max. V _{IN} = 3.4V ⁽³⁾		—	0.5	2.0	mA
I _{CCD}	Dynamic Power Supply Current ⁽⁴⁾	V _{CC} = Max. Outputs Open OE = EN = GND One Input Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	—	0.15	0.25	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max. Outputs Open f _{CP} = 10MHz 50% Duty Cycle OE = EN = GND One Bit Toggling at f _i = 5MHz 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	—	1.7	4.0	mA
			V _{IN} = 3.4V V _{IN} = GND	—	2.2	6.0	
		V _{CC} = Max. Outputs Open f _{CP} = 10MHz 50% Duty Cycle OE = EN = GND Eight Bits Toggling at f _i = 2.5MHz 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	—	4.0	7.8 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND	—	6.2	16.8 ⁽⁵⁾	

NOTES:

2567 tbl 07

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} \cdot DH_{NT} + I_{CCD} (f_{CP}/2 + f_i N_i)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
 DH = Duty Cycle for TTL Inputs High
 NT = Number of TTL Inputs at DH
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = Input Frequency
 N_i = Number of Inputs at f_i
 All currents are in milliamps and all frequencies are in megahertz.



SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	FCT821AT-826AT				FCT821BT-826BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay CP to Y _i (OE = LOW)	CL = 50pF RL = 500Ω	1.5	10.0	1.5	11.5	1.5	7.5	1.5	8.5	ns
		CL = 300pF ⁽⁴⁾ RL = 500Ω	1.5	20.0	1.5	20.0	1.5	15.0	1.5	16.0	
tSU	Set-up Time HIGH or LOW DI to CP	CL = 50pF RL = 500Ω	4.0	—	4.0	—	3.0	—	3.0	—	ns
tH	Hold Time HIGH or LOW DI to CP		2.0	—	2.0	—	1.5	—	1.5	—	ns
tSU	Set-up Time HIGH or LOW EN to CP		4.0	—	4.0	—	3.0	—	3.0	—	ns
tH	Hold Time HIGH or LOW EN to CP		2.0	—	2.0	—	0	—	0	—	ns
tPHL	Propagation Delay, $\overline{\text{CLR}}$ to Y _i		1.5	14.0	1.5	15.0	1.5	9.0	1.5	9.5	ns
tREM	Recovery Time $\overline{\text{CLR}}$ to CP		6.0	—	7.0	—	6.0	—	6.0	—	ns
tW	Clock Pulse Width HIGH or LOW		7.0	—	7.0	—	6.0	—	6.0	—	ns
tW	$\overline{\text{CLR}}$ Pulse Width LOW		6.0	—	7.0	—	6.0	—	6.0	—	ns
tPZH tPZL	Output Enable Time $\overline{\text{OE}}$ to Y _i	CL = 50pF RL = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	9.0	ns
		CL = 300pF ⁽⁴⁾ RL = 500Ω	1.5	23.0	1.5	25.0	1.5	15.0	1.5	16.0	
tPHZ tPLZ	Output Disable Time $\overline{\text{OE}}$ to Y _i	CL = 5pF ⁽⁴⁾ RL = 500Ω	1.5	7.0	1.5	8.0	1.5	6.5	1.5	7.0	ns
		CL = 50pF RL = 500Ω	1.5	8.0	1.5	9.0	1.5	7.5	1.5	8.0	

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.
4. This condition is guaranteed but not tested.

2567tbl08

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	FCT821CT-826CT				FCT821DT		FCT823DT		Unit
			Com'l.		Mil.		Com'l.		Com'l.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay CP to Yi ($\overline{OE} = \text{LOW}$)	CL = 50pF RL = 500Ω	1.5	6.0	1.5	7.0	1.5	4.2	1.5	5.0	ns
		CL = 300pF ⁽⁴⁾ RL = 500Ω	1.5	12.5	1.5	13.5	1.5	8.0	1.5	8.5	
tsu	Set-up Time HIGH or LOW DI to CP	CL = 50pF RL = 500Ω	3.0	—	3.0	—	2.0	—	2.0	—	ns
th	Hold Time HIGH or LOW DI to CP		1.5	—	1.5	—	1.0	—	1.0	—	ns
tsu	Set-up Time HIGH or LOW \overline{EN} to CP		3.0	—	3.0	—	3.0	—	3.0	—	ns
th	Hold Time HIGH or LOW \overline{EN} to CP		0	—	0	—	0	—	0	—	ns
tPHL	Propagation Delay, \overline{CLR} to Yi		1.5	8.0	1.5	8.5	1.5	5.0	1.5	5.0	ns
tREM	Recovery Time \overline{CLR} to CP		6.0	—	6.0	—	3.0	—	3.0	—	ns
tw	Clock Pulse Width HIGH or LOW ⁽³⁾		6.0	—	6.0	—	3.0	—	3.0	—	ns
tw	\overline{CLR} Pulse Width LOW ⁽³⁾		6.0	—	6.0	—	3.0	—	3.0	—	ns
tPZH tPZL	Output Enable Time \overline{OE} to Yi	CL = 50pF RL = 500Ω	1.5	7.0	1.5	8.0	1.5	4.8	1.5	4.8	ns
		CL = 300pF ⁽⁴⁾ RL = 500Ω	1.5	12.5	1.5	13.5	1.5	9.0	1.5	9.0	
tPHZ tPLZ	Output Disable Time \overline{OE} to Yi	CL = 5pF ⁽⁴⁾ RL = 500Ω	1.5	6.0	1.5	6.0	1.5	4.0	1.5	4.0	ns
		CL = 50pF RL = 500Ω	1.5	6.5	1.5	6.5	1.5	4.0	1.5	4.0	

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.
4. This condition is guaranteed but not tested.

2567 tbl 09

