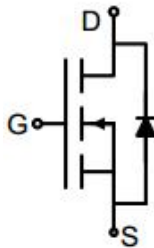



N-Channel Enhancement Mode Power MOSFET

<p>Description</p> <p>The GC11N65K uses advanced super junction technology and design to provide excellent $R_{os(on)}$, low gate charge and operation. This device is suitable for industry's AC-DC SMPS requirement for PFC, AC/DC power conversion, and industrial power application.</p> <p>General Features</p> <ul style="list-style-type: none"> ● V_{DS} 650V ● I_D (at $V_{GS} = 10V$) 11A ● $R_{DS(ON)}$ (at $V_{GS} = 10V$) < 360mΩ ● 100% Avalanche Tested ● RoHS Compliant <p>Application</p> <ul style="list-style-type: none"> ● Power switch ● DC/DC converters 	 <p>Schematic diagram</p>  <p>TO-252</p>
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Ordering Information

Device	Package	Marking	Packaging
GC11N65K	TO-252	GC11N65	2500pcs/Reel

Absolute Maximum Ratings $T_C = 25^\circ C$, unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	650	V
Continuous Drain Current	I_D	$T_C = 25^\circ C$	11
		$T_C = 100^\circ C$	7
Pulsed Drain Current (note1)	I_{DM}	33	A
Gate-Source Voltage	V_{GS}	± 30	V
Power Dissipation	P_D	78	W
Single pulse avalanche energy (note2)	E_{AS}	125	mJ
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	$^\circ C$

Thermal Resistance

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient	R_{thJA}	62	$^\circ C/W$
Thermal Resistance, Junction-to-Case	R_{thJC}	1.6	$^\circ C/W$

Specifications $T_J = 25^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	650	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 650V, V_{GS} = 0V$	--	--	1	μA
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 30V$	--	--	± 100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.5	3.5	4.0	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 5.5A$	--	330	360	m Ω
Forward Transconductance	g_{FS}	$V_{GS} = 5V, I_D = 5.5A$	--	6	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{GS} = 0V,$ $V_{DS} = 400V,$ $f = 1.0MHz$	--	768	--	pF
Output Capacitance	C_{oss}		--	19	--	
Reverse Transfer Capacitance	C_{rss}		--	0.2	--	
Total Gate Charge	Q_g	$V_{DD} = 400V,$ $I_D = 5.5A,$ $V_{GS} = 10V$	--	21	--	nC
Gate-Source Charge	Q_{gs}		--	4.5	--	
Gate-Drain Charge	Q_{gd}		--	7	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 400V,$ $I_D = 5.5A,$ $R_G = 25\Omega$	--	42	--	ns
Turn-on Rise Time	t_r		--	20	--	
Turn-off Delay Time	$t_{d(off)}$		--	123	--	
Turn-off Fall Time	t_f		--	6.4	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	$T_C = 25^\circ\text{C}$	--	--	11	A
Body Diode Voltage	V_{SD}	$T_J = 25^\circ\text{C}, I_{SD} = 5.5A, V_{GS} = 0V$	--	--	1.2	V
Reverse Recovery Charge	Q_{rr}	$I_F = 5.5A, V_{GS} = 0V$ $di/dt = 100A/\mu s$	--	2.8	--	μC
Reverse Recovery Time	T_{rr}		--	280	--	ns

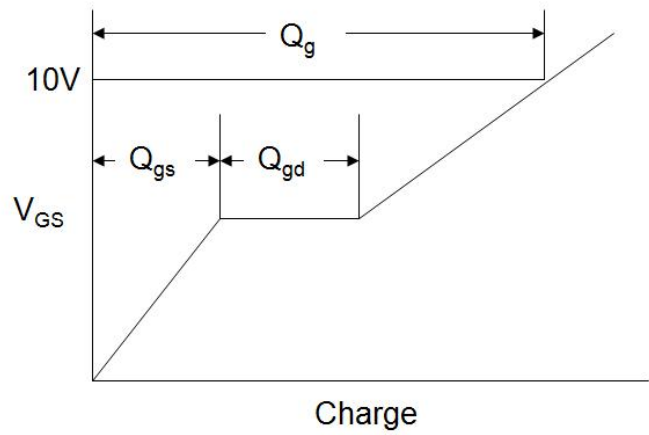
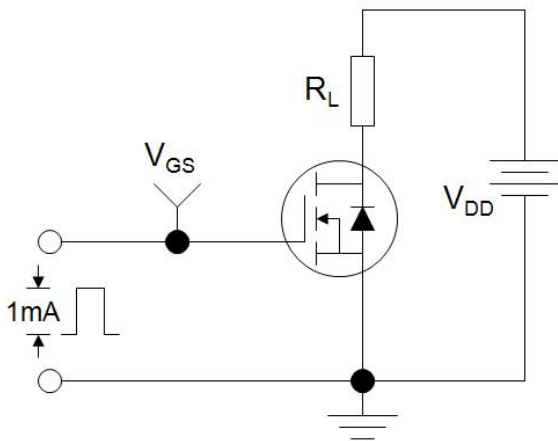
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. EAS condition : $T_J = 25^\circ\text{C}, V_{DD} = 50V, V_{GS} = 10V, L = 10mH, R_G = 25\Omega$

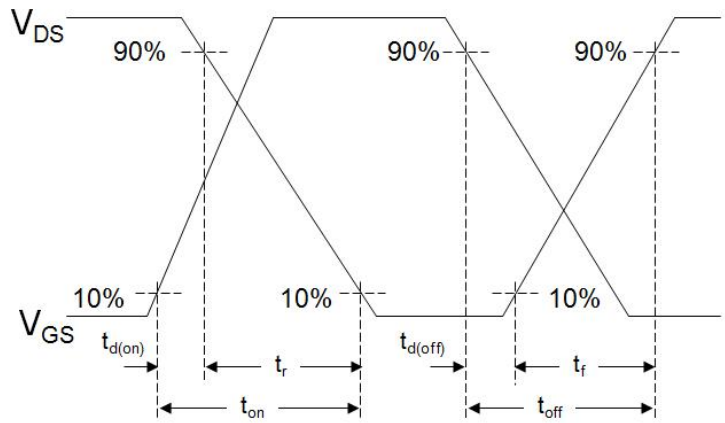
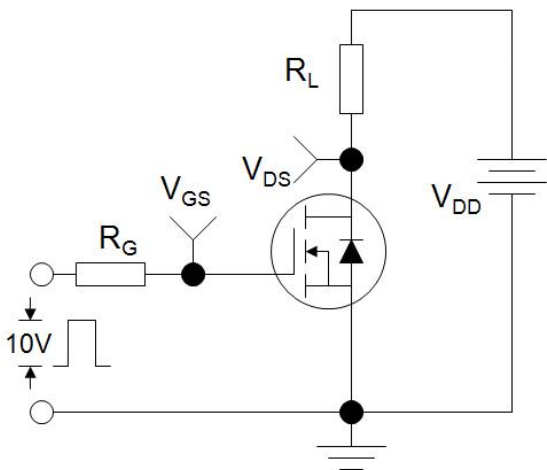
The table shows the minimum avalanche energy, which is 405mJ when the device is tested until failure

3. Identical low side and high side switch with identical R_G

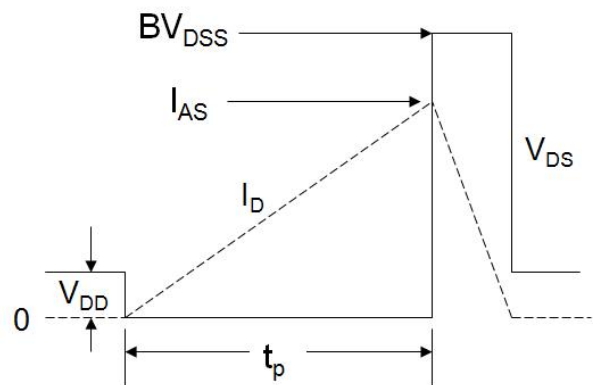
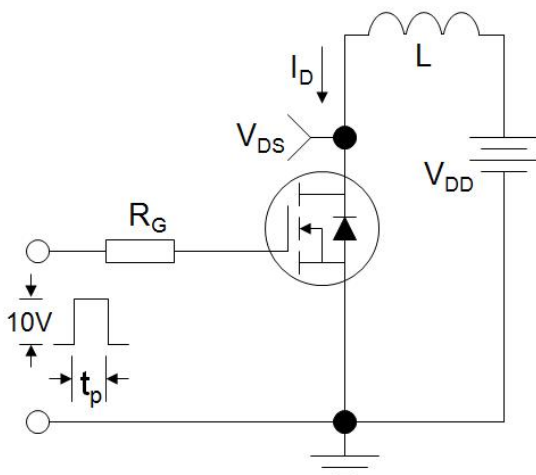
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 1. Output Characteristics

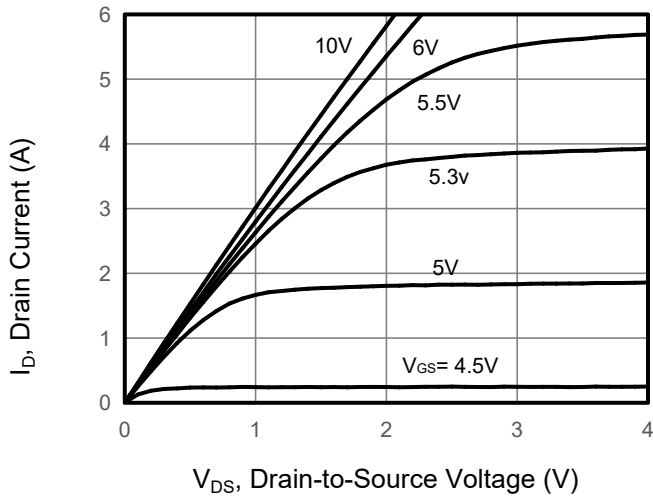


Figure 2. Transfer Characteristics

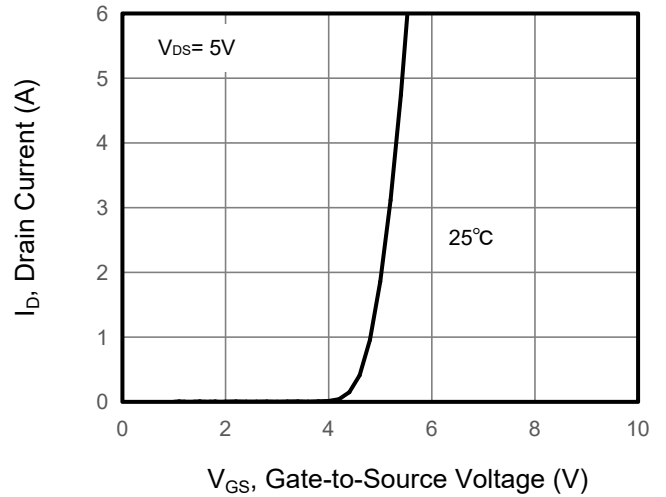


Figure 3. Drain Source On Resistance

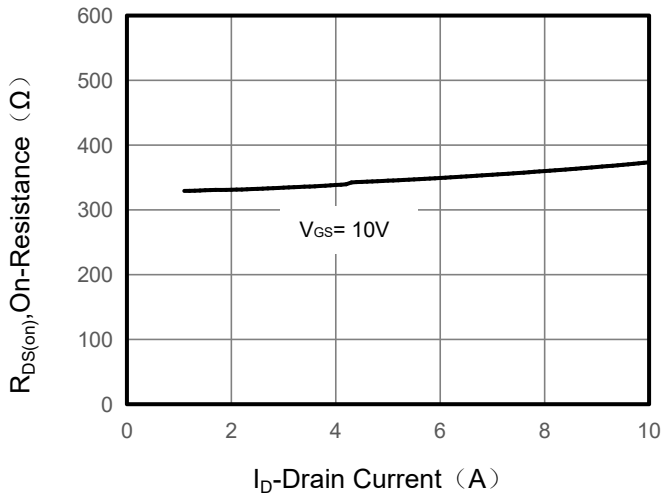


Figure 4. Gate Charge

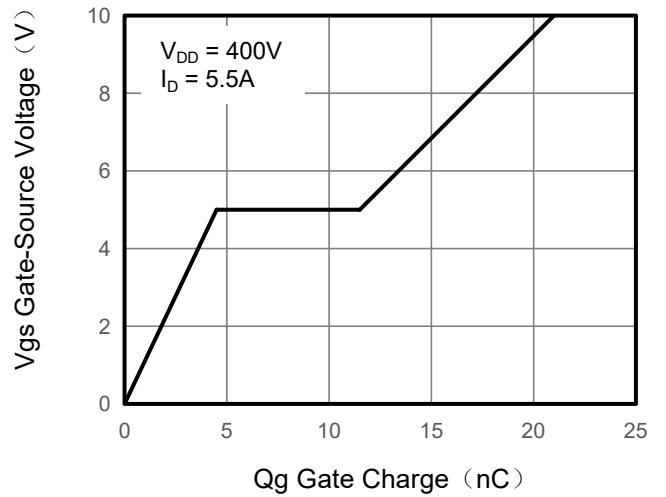


Figure 5. Capacitance

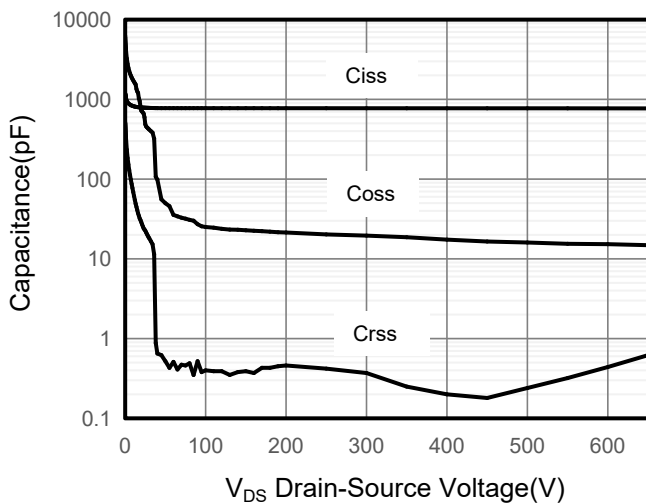
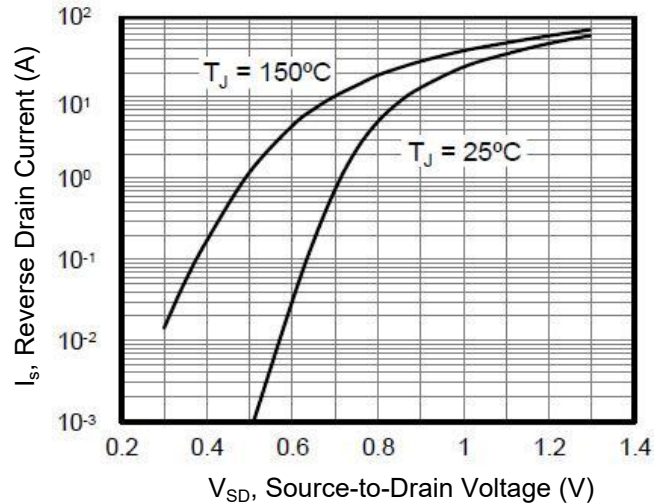


Figure 6. Source-Drain Diode Forward



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 7. Drain-Source On-Resistance

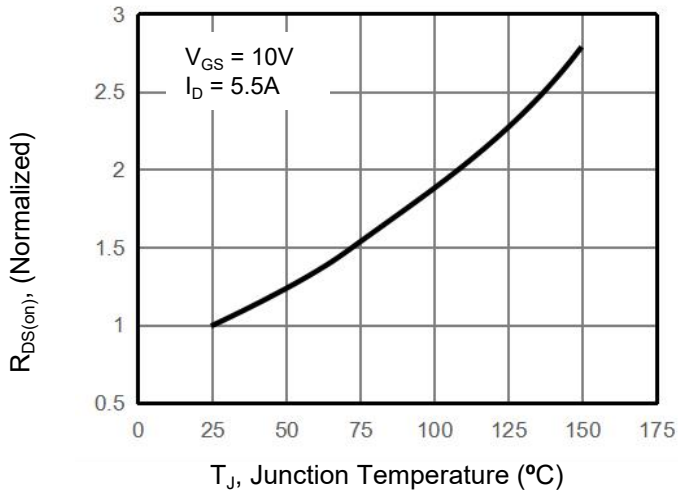


Figure 8. Safe Operation Area

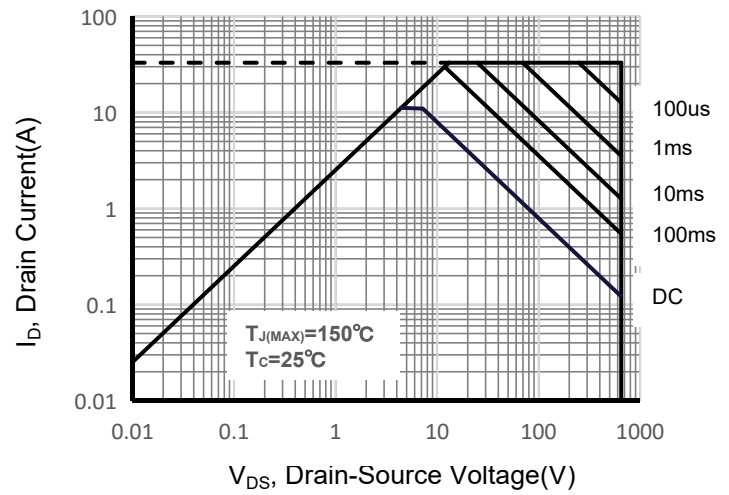


Figure 9. Maximum Continuous Drain Current vs Case Temperature

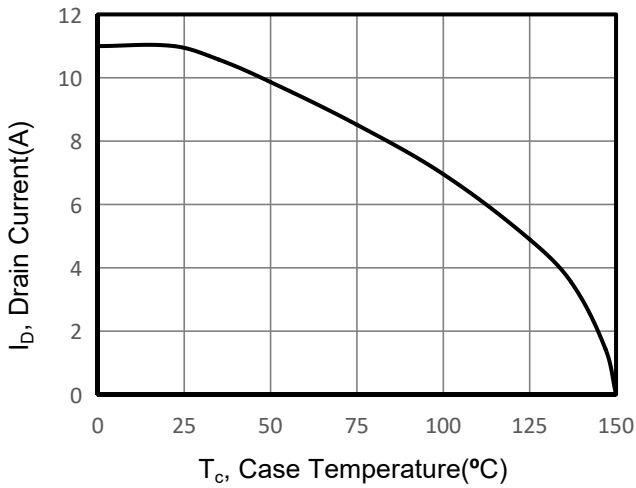
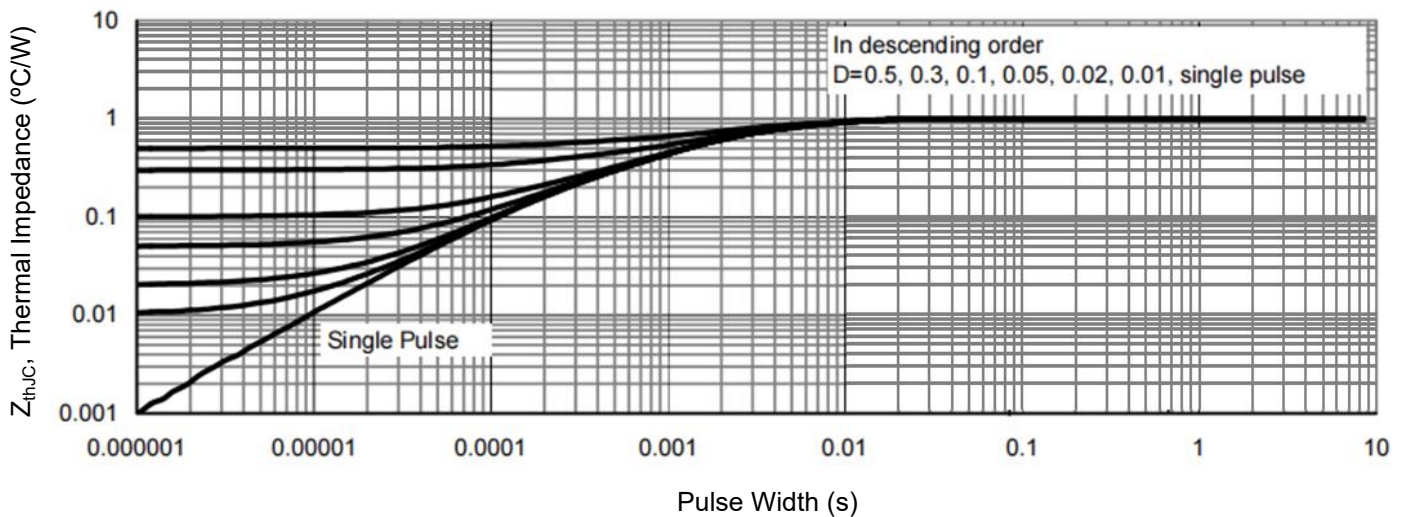
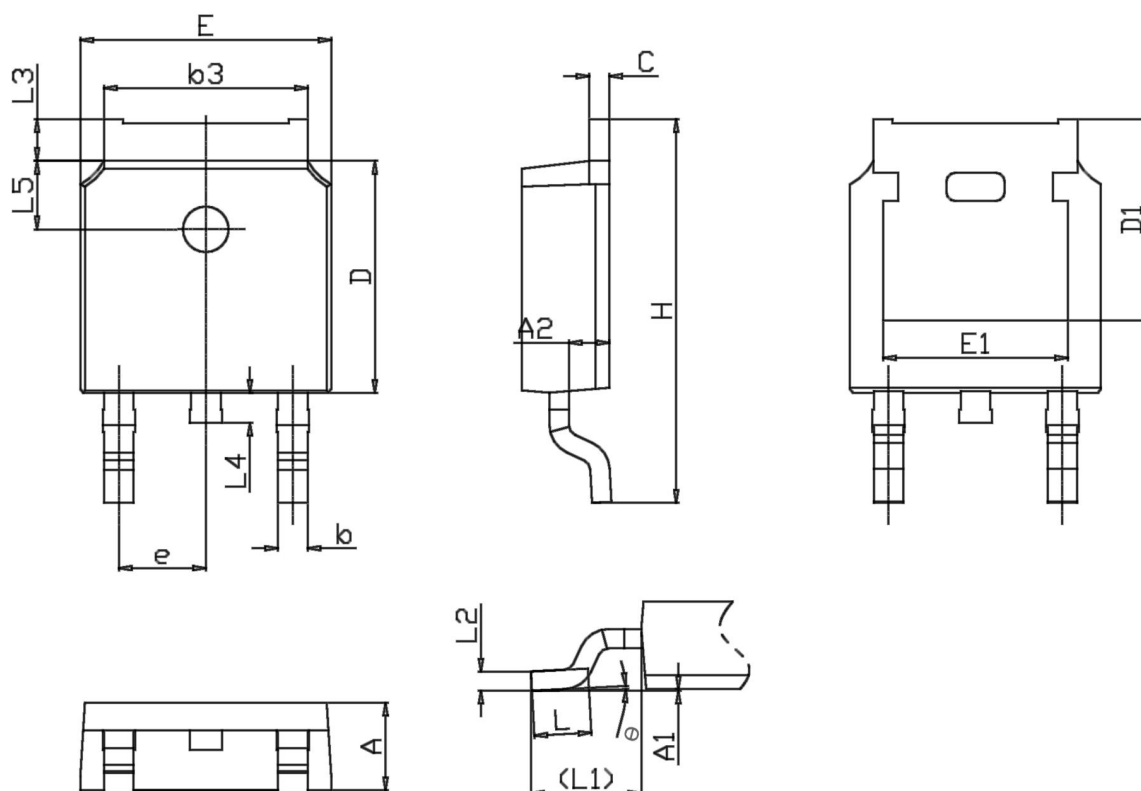


Figure 10. Normalized Maximum Transient Thermal Impedance



TO-252 Package Information



SYMBOL	mm		
	MIN	NOM	MAX
A	2.20	2.30	2.38
A1	0.00	-	0.12
A2	0.97	1.07	1.17
b	0.68	0.78	0.90
b3	5.20	5.33	5.46
c	0.43	0.53	0.61
D	5.98	6.10	6.22
D1	5.30REF		
E	6.40	6.60	6.73
E1	4.63	-	-
e	2.286BSC		
H	9.40	10.10	10.50
L	1.38	1.50	1.75
L1	2.90REF		
L2	0.51BSC		
L3	0.88	-	1.28
L4	0.50	-	1.00
L5	1.65	1.80	1.95
θ	0°	-	8°