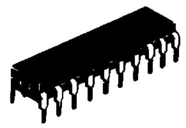
HA17012P, HA17012G ●12-bit Multiplying Digital-to-Analog Converter

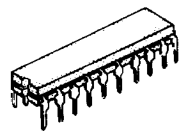
HA17012 is a monolithic high speed multiplying D/A converter which provides 12-bit resultion and current output. It is divided into two groups according to the accuracy of linearity and the differential error.

HA17012P



(DP-20)

HA17012G



(DG-20)

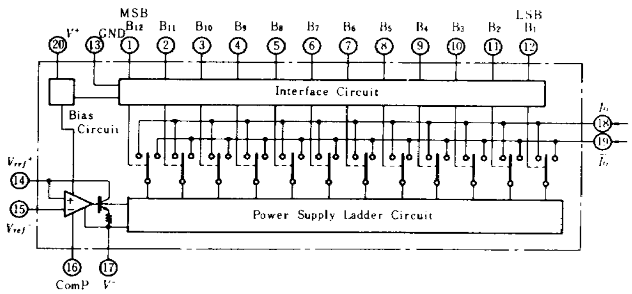
■ FEATURES

- With differential current attraction terminals (I_0, $\bar{I}_0$)
- 4mA full scale output is gained with 1mA reference input current.
- The settling time is short, 250ns (typ), and fast conversion is possible.
- Possible to connect a digital input to TTL and CMOS directly.
- Compatible with Am6012 of AMD Ltd.

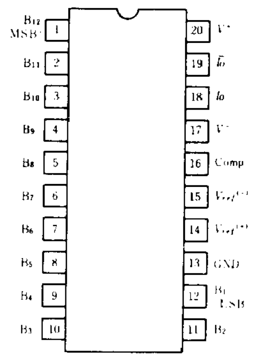
■ ACCURACY

Type No.	Linearity Accuracy		Differential Accuracy	
	Bit	LSB	Bit	LSB
HA17012B	11	±2	12	±1
HA17012C	10	±4	11	+2, −1

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS (Ta=250°C)

Item	Symbol	Rating	Unit
Supply Voltage	$V^{\cdot}$	±18	V
Logic Input Voltage	V_{LIN}	−5 to +15	V
Analog Output Voltage	V_{OUT}	−8 to +12	V
Reference Input Voltage	V_{ref}	V^- to V^+	V
Reference Input Current	I_{ref}	1.25	mA
Differential Reference Input Voltage Range	$V_{IN,dif}$	±18	V
Operating Temperature	T_{opr}	−20 to +75	℃
Storage Temperature *	T_{stg}	−65 to +150	℃

* In HA17012P: −55 to +125℃

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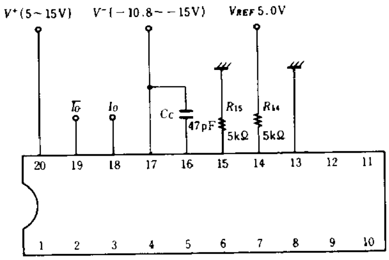
■ RECOMMENDED OPERATING CONDITIONS

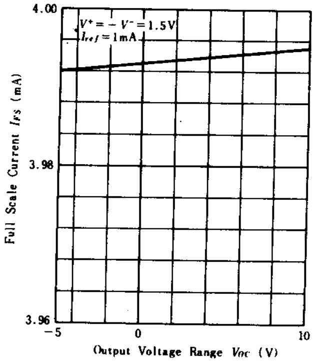
Item	Symbol	Recommended Value	Unit
Supply Voltage	V^+	5 to 15	V
	V^-	−15 to −10.8	V
Logic Input Voltage	V_I	0 to V^+	V
Reference Voltage	V_{REF}	5.0	V
Reference Current	I_{ref}	1.0	mA
Reference Input Resistance	R_{14}, R_{15}	5.0	kΩ
Phase Compen-sation Capacitance	C_C	47	pF
Output Voltage	V_{out}	0	V



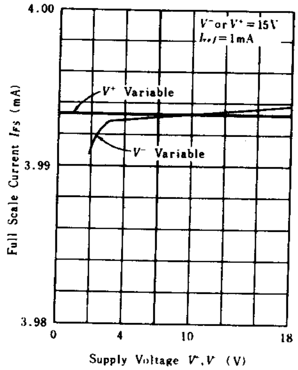
■ ELECTRICAL CHARACTERISTICS ($V^+ = -V^- = 15V$, $I_{ref} = 1mA$, $Ta = 25°C$)

Item	Symbol	Test Condition	HA17012B			HA17012C			Unit
			min	typ	max	min	typ	max	
Resolution			12	12	12	12	12	12	bits
Differential Error	DNL	$V_{out}=0V$	−0.025	−	+0.025	−0.025	−	+0.05	%FS
Non Linearity	NL	$V_{out}=0V$	−0.05	−	+0.05	−0.1	−	+0.1	%FS
Full Scale Current	I_{FS}	$V_{ref}=15V$, $R_{14}=R_{15}=15k\Omega$	3.935	3.999	4.063	3.871	3.999	4.127	mA
Full Scale Temperature Dependency	$\Delta I_{FS}/I_{FS}$		−	±10	−	−	±20	−	ppm/°C
Output Voltage Range	V_{oc}	$R_{out}>10M\Omega$	−5	−	+10	−5	−	+10	V
Full Scale Subtracted Current	I_{FSS}	$I_{FS}-\overline{I_{FS}}$	−2.0	±0.4	+2.0	−4.0	±0.8	+4.0	μA
Offset Current	I_{ZS}		−	−	0.1	−	−	0.4	μA
Settling Time	t_s	to $\pm\frac{LSB}{2}$ All bits ON.OFF	−	250	−	−	250	−	ns
Delay Time	t_{PLH}, t_{PHL}	50% to 50%	−	25	−	−	25	−	ns
Output Capacitance	C_{out}		−	20	−	−	20	−	pF
Logic Input Voltage	V_{IL}		−	−	0.8	−	−	0.8	V
	V_{IH}		2.0	−	−	2.0	−	−	V
Logic Input Current	I_{IN}	$-5V \leq V_{IN} \leq +15V$	−60	−	+20	−60	−	+20	μA
Ligic Input Voltage Range	V_{IS}	$-5V \leq V_{IN} \leq +15V$	−5	−	+15	−5	−	+15	V
Reference Current Range	I_{REF}		0.2	1.0	1.1	0.2	1.0	1.1	mA
Bias Current at Reference Terminal	I_{15}		−3	−	0	−3	−	0	μA
Supply Voltage Dependency	$PSS \cdot I_{FS}^+$	$13.5V \leq V^+ \leq 16.5V$	−10	−	+10	−10	−	+10	ppmFS/%V
	$PSS \cdot I_{FS}^-$	$-16.5 \leq V^- \leq -13.5V$	−10	−	+10	−10	−	+10	ppmFS/%V
Supply Voltage Range	V^+	$V_{out}=0V$	4.5	−	18	4.5	−	18	V
	V^-		−18	−	−10.8	−18	−	−10.8	V
Supply Current	I^+	$V^+=15V$	−	5.2	8.5	−	5.2	8.5	mA
	I^-	$V^-=-15V$	−23	−17.2	−	−23	−17.2	−	mA
Power Dissipation	P_T	$V^+=15V$ $V^-=-15V$	−	336	473	−	336	473	mW

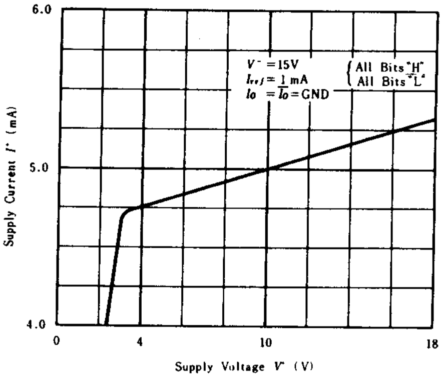
FULLSCALE CURRENT VS. OUTPUT VOLTAGE RANGE



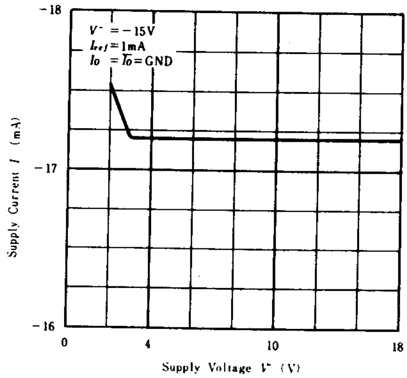
FULLSCALE CURRENT VS. SUPPLY VOLTAGE



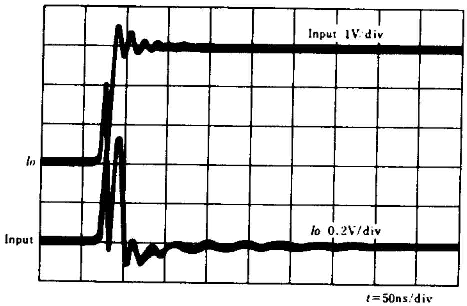
SUPPLY CURRENT VS. SUPPLY VOLTAGE(1)

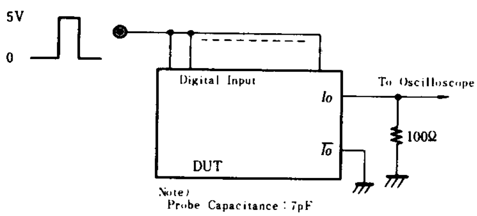


SUPPLY CURRENT VS. SUPPLY VOLTAGE(2)



SETTLING WAVEFORM(ALL BITS ON-OFF)



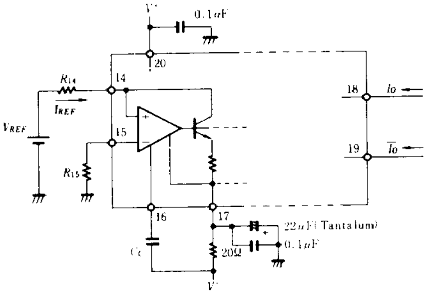


Test Circuit

■ APPLICATION NOTES

1. Method to Apply a Reference Input

● Positive Reference Voltage



The full scale output current ($I_0 + \overline{I_0}$) is four times as large as the reference input current (I_{REF}) on account of the internal circuit.

$$I_{FS} = I_0 + \overline{I_0} \fallingdotseq 4I_{REF}$$

V_{REF} is converted to the reference input current (I_{REF}) by R_{14}.

$$I_{REF} \fallingdotseq \frac{V_{REF}}{R_{14}}$$

To erase the input bias current error of the input operational amplifier, $R_{14} = R_{15}$.

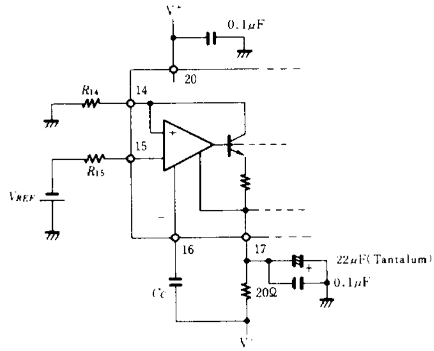
The phase correction capacitance C_C is 0.01μF generally and the minimum value can be found by;

$$C_C = 5 \times R_{14}\ (\text{k}\Omega)\ (\text{pF})$$

For example, when R_{14} 0 5kΩ, the minimum value of C_C is;

$$C_C = 5 \times 5 = 25\ (\text{pF})$$

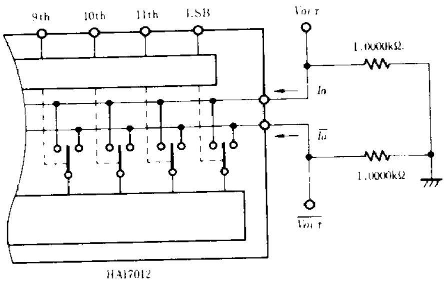
● Negative Reference Voltage



2. Method to Connect Output Circuit

(1) Resistor

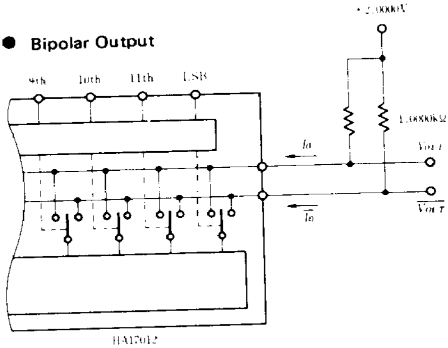
● Unipolar Negative Output Voltage



$I_{REF} = 1.0000$mA

Input Code MSB LSB	I_O (mA)	$\overline{I_O}$ (mA)	V_{OUT} (V)	$\overline{V_{OUT}}$ (V)
1 1 1 1 1 1 1 1 1 1 1 1	3.999	0.000	−3.999	0.000
1 1 1 1 1 1 1 1 1 1 1 0	3.998	0.001	−3.998	−0.001
1 0 0 0 0 0 0 0 0 0 0 0	2.000	1.999	−2.000	−1.999
0 0 0 0 0 0 0 0 0 0 0 1	0.001	3.998	−0.001	−3.998
0 0 0 0 0 0 0 0 0 0 0 0	0.000	3.999	0.000	−3.999

● Bipolar Output

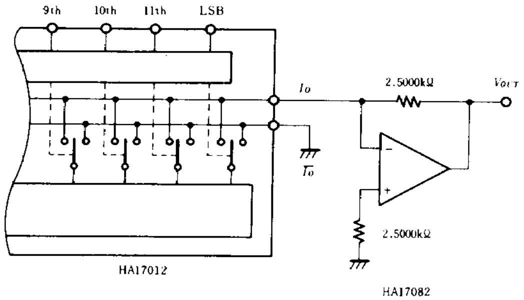


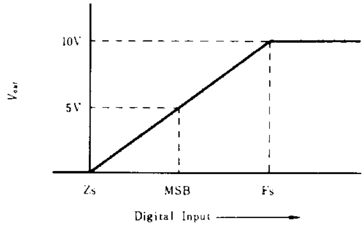
$I_{REF} = 1.0000$mA

Input Code MSB LSB	I_O (mA)	$\overline{I_O}$ (mA)	V_{OUT} (V)	$\overline{V_{OUT}}$ (V)
1 1 1 1 1 1 1 1 1 1 1 1	3.999	0.000	−1.999	+2.000
1 1 1 1 1 1 1 1 1 1 1 0	3.998	0.001	−1.998	+1.999
1 0 0 0 0 0 0 0 0 0 0 1	2.001	1.998	−0.001	+0.002
1 0 0 0 0 0 0 0 0 0 0 0	2.000	1.999	0.000	+0.001
0 1 1 1 1 1 1 1 1 1 1 1	1.999	2.000	+0.001	0.000
0 0 0 0 0 0 0 0 0 0 0 1	0.001	3.998	+1.999	−1.998
0 0 0 0 0 0 0 0 0 0 0 0	0.000	3.999	+2.000	−1.999

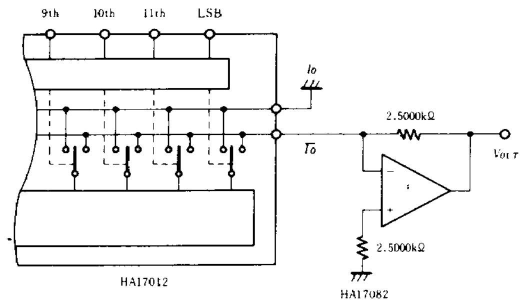
(2) Method to Connect Output Buffer and Amplifier

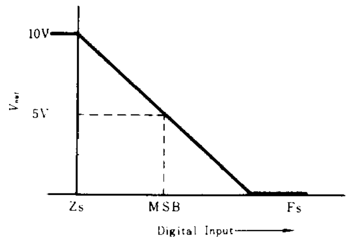
- **Unipolar Positive Output Voltage (Straight Binary)**



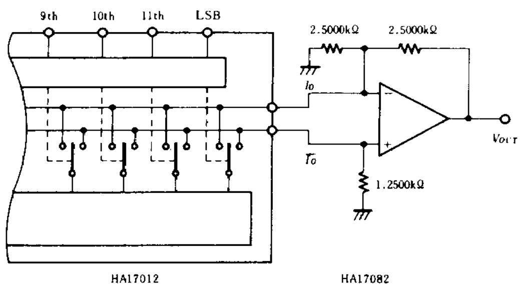


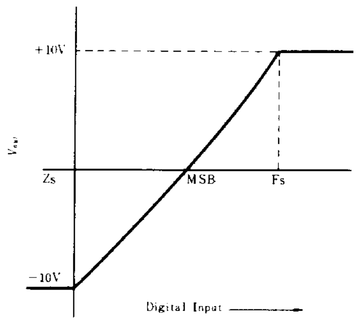
- **Unipolar Positive Output Voltage (Complementary Binary)**





- **Symmetrical Offset Output Voltage**





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