UMW IRLR120NTR

100V N-Channel MOSFET

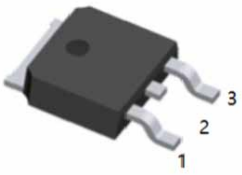
1.Features

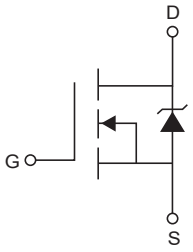
- $V_{DS\ (V)}$= 100V
- I_D=10A(V_{GS}=10V)
- $R_{DS(ON)}$<185mΩ(V_{GS}=10V)
- $R_{DS(ON)}$<225mΩ(V_{GS}=5V)
- $R_{DS(ON)}$<265mΩ(V_{GS}=4V)

2.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	DRAIN
3	S	SOURCE

TO-252(DPAK)
top view





3.Absolute Maximum Ratings

Parameter		Symbol	Rating	Units
Continuous Drain Current, V_{GS}=10V	T_C=25°C	I_D	10	A
Continuous Drain Current, V_{GS}=10V	T_C=100°C		7	A
Pulsed Drain Current ①⑥		I_{DM}	35	A
Power Dissipation	T_C=25°C	P_D	48	W
Linear Derating Factor			0.32	W/°C
Gate-to-Source Voltage		V_{GS}	±16	V
Single Pulse Avalanche Energy②⑥		E_{AS}	85	mJ
Avalanche Current①⑥		I_{AR}	6	A
Repetitive Avalanche Energy①⑥		E_{AR}	4.8	mJ
Peak Diode Recovery dv/dt ③		dv/dt	5	V/ns
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	°C
Soldering Temperature, for 10 seconds			300 (1.6mm from case)	°C

4.Thermal resistance rating

Parameter	Symbol	Typ	Max	Units
Junction-to-Case	$R_{\theta JC}$		3.1	°C/W
Junction-to-Ambient (PCB Mount) **	$R_{\theta JA}$		50	°C/W
Junction-to-Ambient	$R_{\theta JA}$		110	°C/W

5.Electrical Characteristics @ T_J= 25°C (unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=250μA, V_{GS}=0V	100			V
Breakdown Voltage Temp. Coefficient	$\Delta V_{(BR)DSS}/T_J$	I_D=1mA,Reference to 25°C		0.12		V/°C
Static Drain-to-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=6A ④			185	mΩ
		V_{GS}=5V, I_D=6A ④			225	
		V_{GS}=4V, I_D=5A ④			265	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1		2	V
Forward Transconductance	g_{FS}	V_{DS}=25V, I_D=6A ⑥	3.1			S
Drain-to-Source Leakage Current	I_{DSS}	V_{DS}=100V, V_{GS}=0V			25	μA
		V_{DS}=80V,V_{GS}=0V,T_J=150°C			250	
Gate-to-Source Forward Leakage	I_{GSS}	V_{GS}=16V			100	nA
Gate-to-Source Reverse Leakage		V_{GS}=-16V			-100	
Total Gate Charge	Q_g	I_D=6A			20	nC
Gate-to-Source Charge	Q_{gs}	V_{DS}=80V, V_{GS}=5V			4.6	
Gate-to-Drain ("Miller") Charge	Q_{gd}	See Fig. 6 and 13 ④⑥			10	
Turn-On Delay Time	$t_{D(on)}$	V_{DD}=50V, I_D=6A		4		ns
Rise Time	t_r	R_G=11Ω, V_{GS}=5V		35		ns
Turn-Off Delay Time	$t_{D(off)}$	R_D=8.2Ω,See Fig. 10 ④⑥		23		ns
Fall Time	t_f			22		ns
Internal Drain inductance	L_D	Between lead, 6mm (0.25in.) from package and center of die contact⑤		4.5		nH
Internal Source inductance	L_S			7.5		
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V f = 1.0MHz, See Fig. 5 ⑥		440		pF
Output Capacitance	C_{oss}			97		pF
Reverse Transfer Capacitance	C_{rss}			50		pF

Source-Drain Ratings and Characteristics						
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode.			10	A
Pulsed Source Current (Body Diode) ① ⑥	I_{SM}				35	A
Diode Forward Voltage	V_{SD}	T_J=25°C, I_S=6A, V_{GS}=0V ④			1.3	V
Reverse Recovery Time	t_{rr}	T_J=25°C, I_F=6A dI/dt=100A/μs ④ ⑥		110	160	ns
Reverse Recovery Charge	Q_{rr}			410	620	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② V_{DD}=25V, starting T_J=25°C, L=4.7mH R_G=25Ω, I_{AS}=6A. (See Figure 12)

③ I_{SD} ≤ 6.0A, di/dt ≤340A/μs, V_{DD} ≤ $V_{(BR)DSS}$,T_J ≤ 175°C

④ Pulse width ≤ 300μs; duty cycle ≤ 2%

⑤ Uses IRL530N data and test conditions.

⑥ This is applied for I-PAK, L_S of D-PAK is measured between lead and center of die contact.

6.1Typical Characterisitics

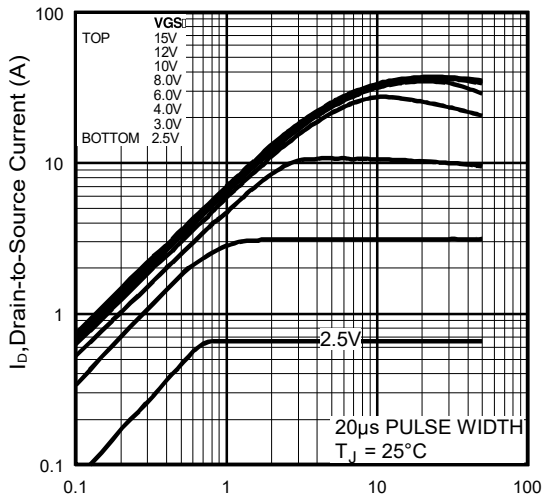


Figure 1: Typical Output Characteristics

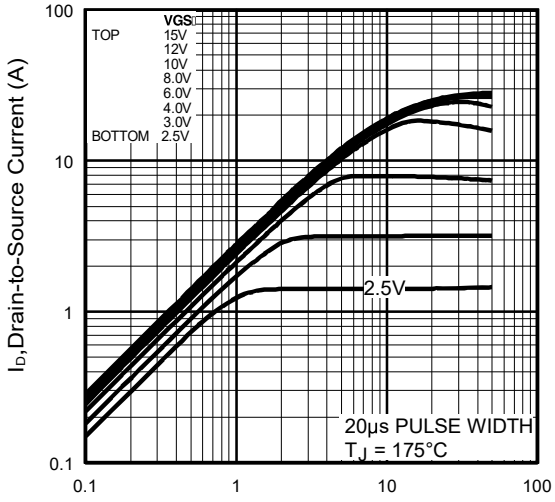


Figure 2: Typical Output Characteristics

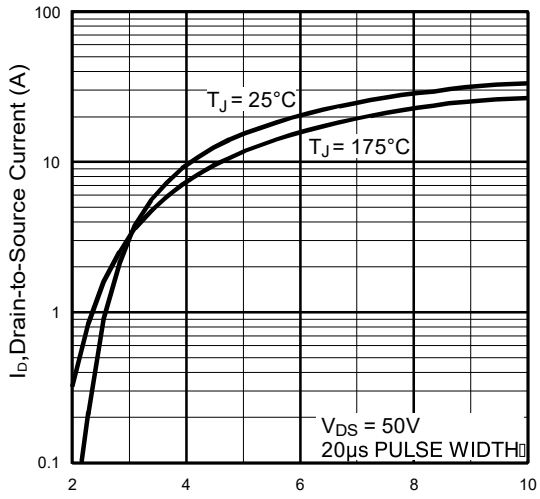


Figure 3: Typical Transfer Characteristics

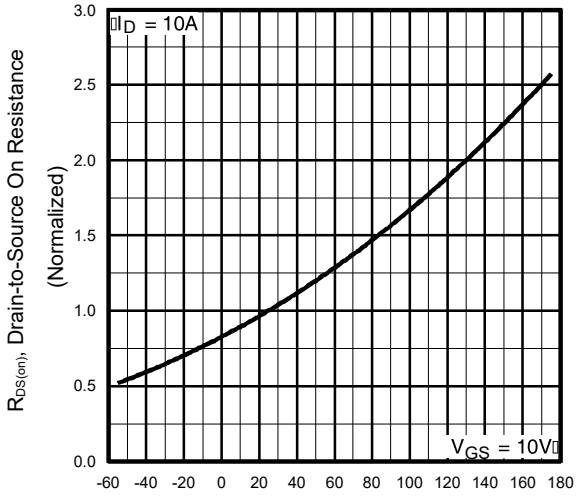
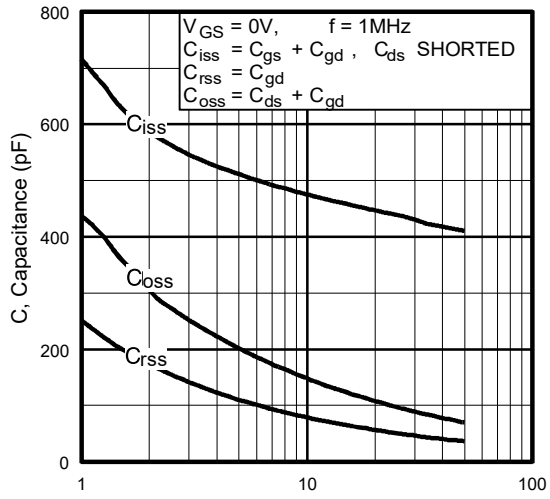


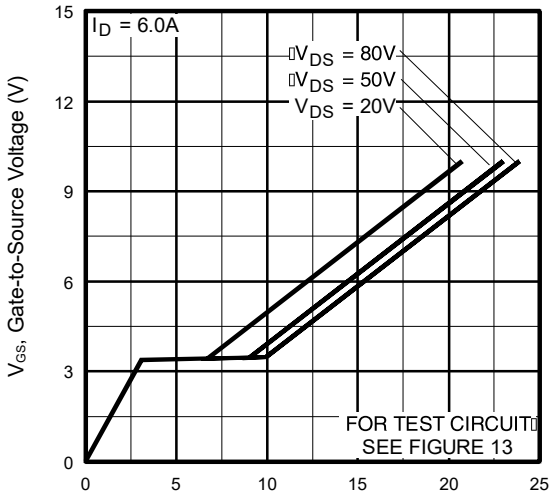
Figure 4: Nomalized On-ResistanceVs. Temperature

6.2Typical Characterisitics



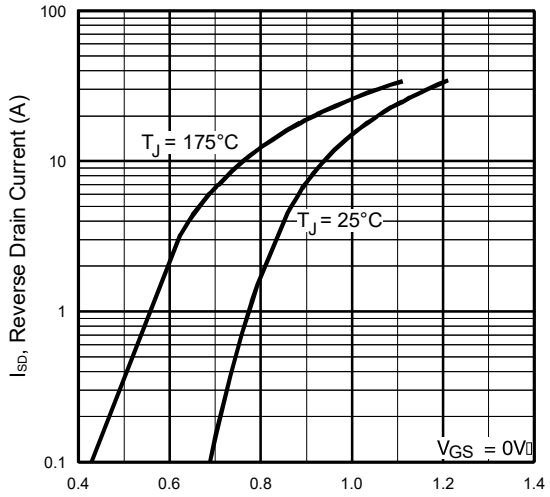
V_{DS} ,Drain-to-Source Voltage (V)

Figure 5: Typical Capacitance Vs. Drain-to-Source Voltage



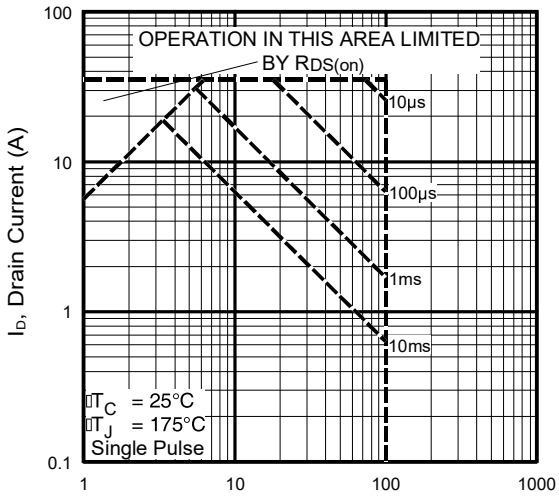
Q_G, Total Gate Charge (nC)

Figure 6: Typical Gate Charge Vs. Gate-to-Source Voltage



V_{SD}, Source-to-Drain Voltage (V)

Figure 7: Typical Source-Drain Diode Forward Voltage



V_{DS}, Drain-to-Source Voltage (V)

Figure 8: Maximum Safe Operating Area

6.3Typical Characterisitics

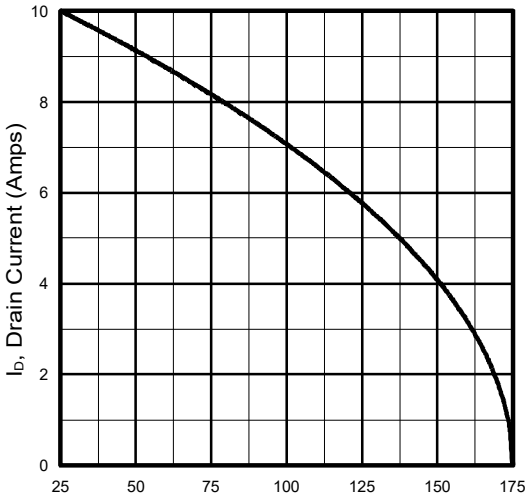


Figure 9: Maximum Drain Current Vs. Case Temperature

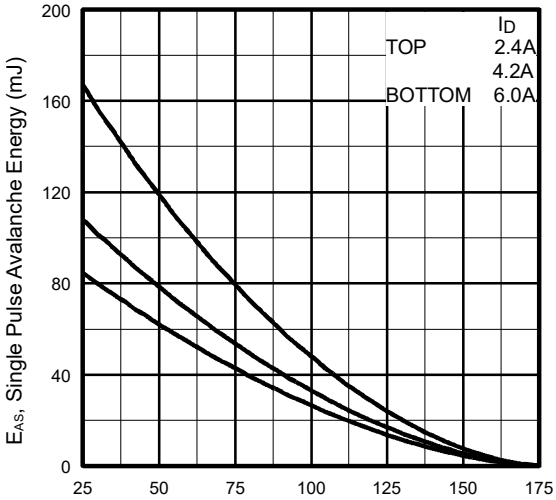


Figure 10: Maximum Avalanche Energy Vs. Drain Current

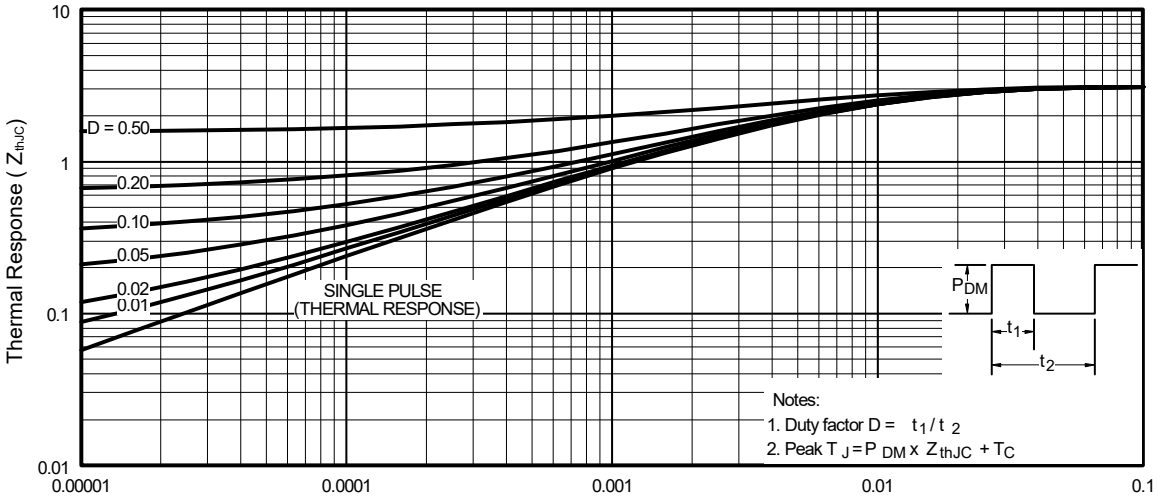


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

6.4Typical Characterisitics

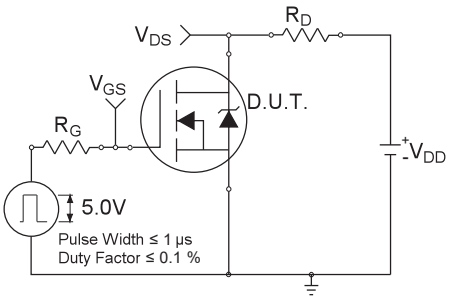


Figure 12a: Switching Time Test Circuit

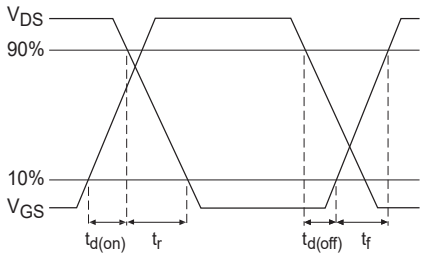


Figure 12b: Switching Time Waveforms

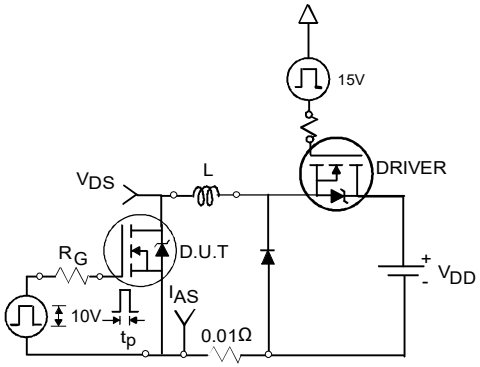


Figure 13a: Unclamped Inductive Test Circuit

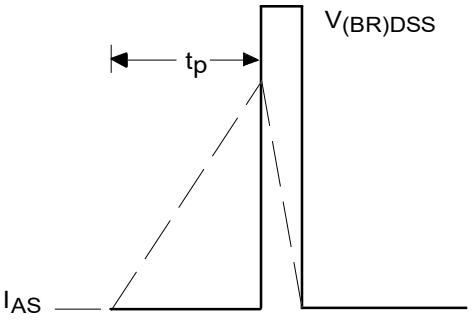


Figure 13b: Unclamped Inductive Waveforms

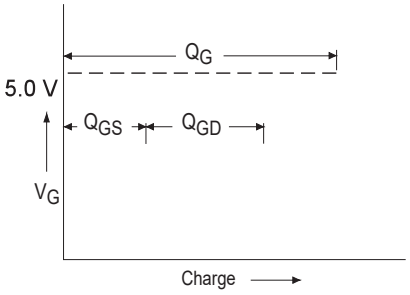


Figure 14a: Basic Gate Charge Waveform

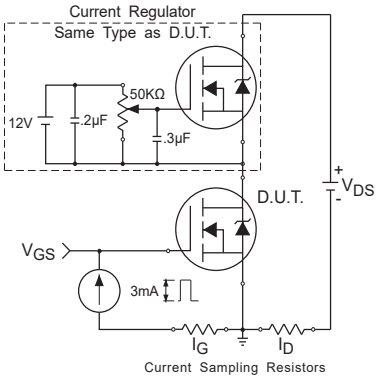
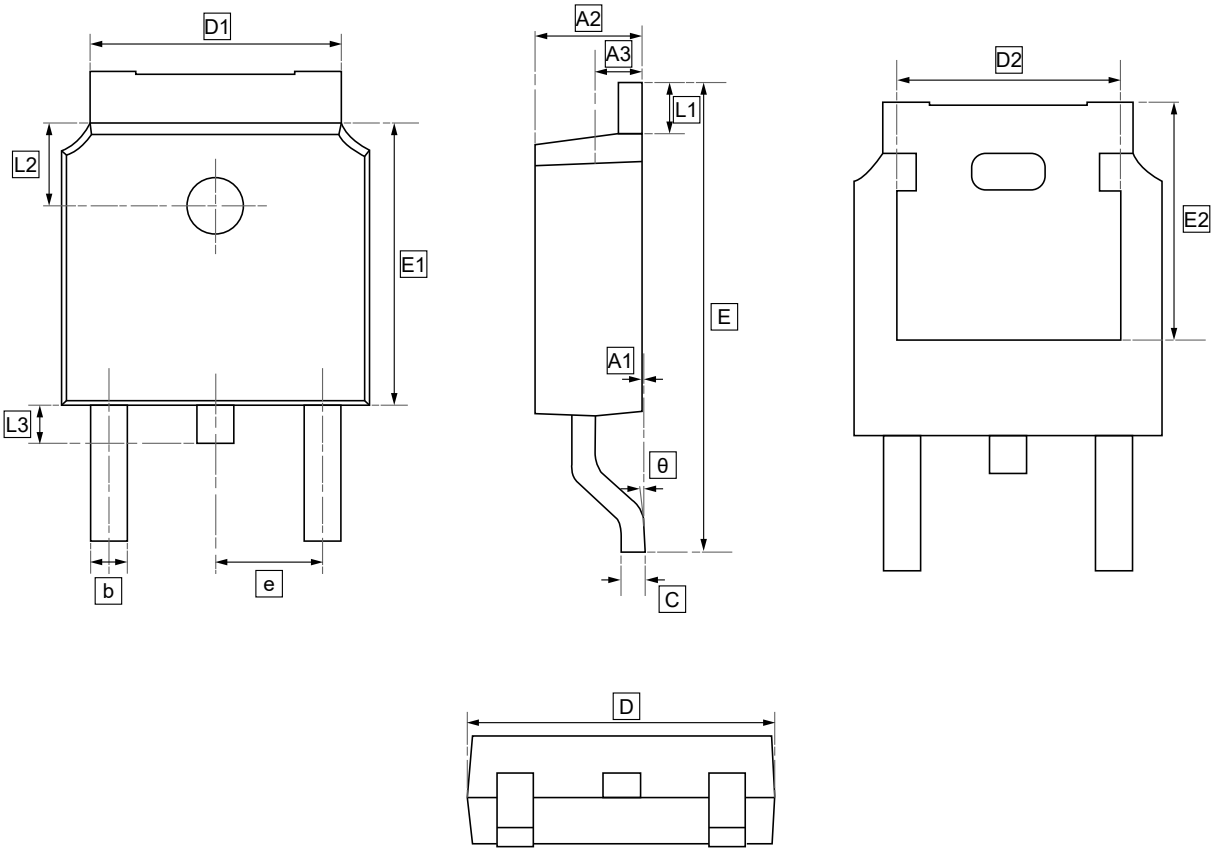


Figure 14b: Gate Charge Test Circuit

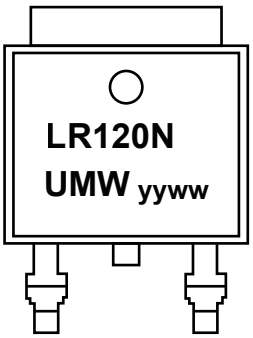
7.TO-252 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A1	A2	A3	b	c	D	D1	D2	E	E1	E2	e	L1	L2	L3	θ
Min	0.00	2.18	0.90	0.65	0.46	6.35	4.95	4.32	9.40	5.97	5.21	2.286	0.89	1.70	0.60	0.00
Max	0.13	2.39	1.10	0.85	0.61	6.73	5.46	4.90	10.41	6.22	5.38	BSC	1.27	1.90	1.00	8.00

8.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IRLR120NTR	TO-252	2500	Tape and reel

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