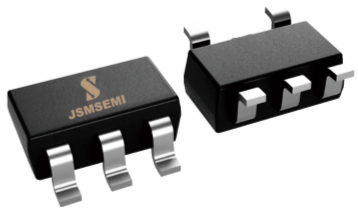
1 Description

The JSM27517 device is a low voltage power MOSFET and IGBT in phase gate driver. Proprietary latch-immune of CMOS technology enables single-chip integrated architectures with high robustness. The JSM27517 logic input level is compatible with CMOS or TTL logic output levels down to 3.3V. The output driver has Internal Undervoltage Lockout (UVLO) circuitry with hysteresis and buffer stage of output current . The JSM27517 is designed to operate over a wide VCC range of 5 V to 25 V and wide temperature range of –40°C to 125°C.



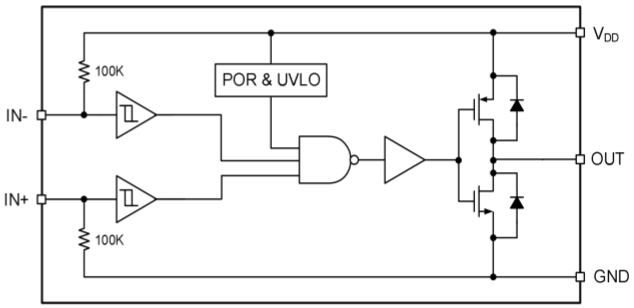
2 Features

- Dual Input Design (Choice of an Inverting (IN- pin) or Non-inverting (IN+ pin) Driver Configuration)
  – Unused Input Pin Can Be Used for Enable or Disable Function
- TTL and CMOS Compatible Input-Logic Threshold
- 5 to 25-V Single-Supply Range
- Operating Temperature Range of -40 to 125°C
- Undervoltage Lockout
  -- Undervoltage Lockout turn-on threshold 4.0V
  -- Undervoltage Lockout turn-off threshold 3.9V
- Turn on/Turn off Delays:
  -- Ton/Toff =30ns/30ns
- 4-A Peak Source and Sink-Drive Current
- SOT-23-5 Package

3 Applications

- Switch-Mode Power Supplies
- General Gate Driver
- Driving MOSFETs and IGBTs

Pin Configuration



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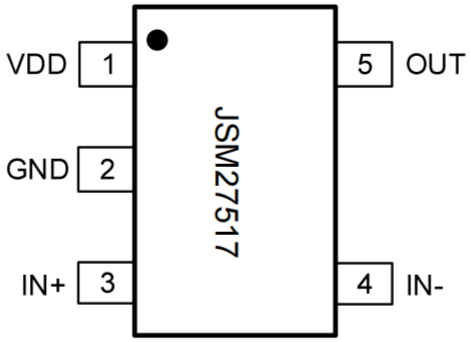
4 Pin Configuration and Functions



5-Pin SOT23-5 Package Top View

Pin Functions

PIN	NAME	DESCRIPTION
1	VDD	Bias supply input
2	GND	Ground: All signals are referenced to this pin.
3	IN+	Non-inverting Input: When the driver is used in inverting configuration, connect IN+ to VDD in order to enable output, OUT held LOW if IN+ is unbiased or floating.
4	IN-	Inverting Input: When the driver is used in non-inverting configuration, connect IN- to GND in order to enable output, OUT held LOW if IN- is unbiased or floating.
5	OUT	Sourcing/Sinking Current Output of Driver

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5 Specifications

5.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. All voltages are with respect to GND unless otherwise noted, Currents are positive into, negative out of the specified terminal, environment temperature is 25 ℃.

Symbol	Definition	MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.3	25	V
V_O	OUT voltage range	-0.3	V_{CC}+0.3	
V_{IN}	IN+, IN- voltage	-0.3	V_{CC}+0.3	

5.2 Thermal Information

Symbol	Definition	MIN	MAX	UNIT
R_{thJA}	thermal resistance	—	151	°C/W
T_S	Storage temperature	-55	+150	°C
T_J	Operating junction temperature	—	+150	
T_L	Lead temperature	—	300	

5.3 Recommended Operating Conditions

To properly operate, device should be used in the following recommended conditions. All voltages are with respect to GND unless otherwise noted, Currents are positive into, negative out of the specified terminal, environment temperature is 25 ℃.

Symbol	Definition	MIN	MAX	UNIT
V_{CC}	Supply voltage range	5.0	20	V
V_O	OUT voltage range	0	V_{CC}	
V_{IN}	IN+, IN- voltage	0	V_{CC}	
T_A	ambient temperature	-40	125	°C

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5.4 Electrical Characteristics

TA= 25℃, VCC=15V, CL=1nF(unless otherwise noted)

Symbol	Definition	MIN	TYP	MAX	UNIT
V_{IH}	Input signal high threshold	2.7	—	—	V
V_{IL}	Input signal low threshold	—	—	0.8	V
V_{CCUV+}	Undervoltage Lockout (UVLO) turn-on threshold VCC	—	4.0	—	V
V_{CCUV-}	Undervoltage Lockout (UVLO) turn-off threshold VCC	—	3.9	—	V
V_{CCUVHY}	UVLO threshold hysteresis VCC	—	0.1	—	V
I_{IN+}	Input current(IN+/IN-=HIGH)	—	50	100	μA
I_{IN-}	Input current(IN+/IN-= LOW)	—	—	5	μA
V_{OH}	High output voltage	—	—	0.35	V
V_{OL}	Low output voltage	—	—	0.35	V
I_Q	VCC quiescent supply current	—	180	400	μA
I_{O+}	Output high short-circuit pulse current	—	4	—	A
I_{O-}	Output low short-circuit pulse current	—	4	—	A
t_R	Rise time	—	10	15	ns
t_F	Fall time	—	10	15	ns
t_{ON}	Turn-on propagation delay	—	30	60	ns
t_{OFF}	Turn-off propagation delay	—	30	60	ns

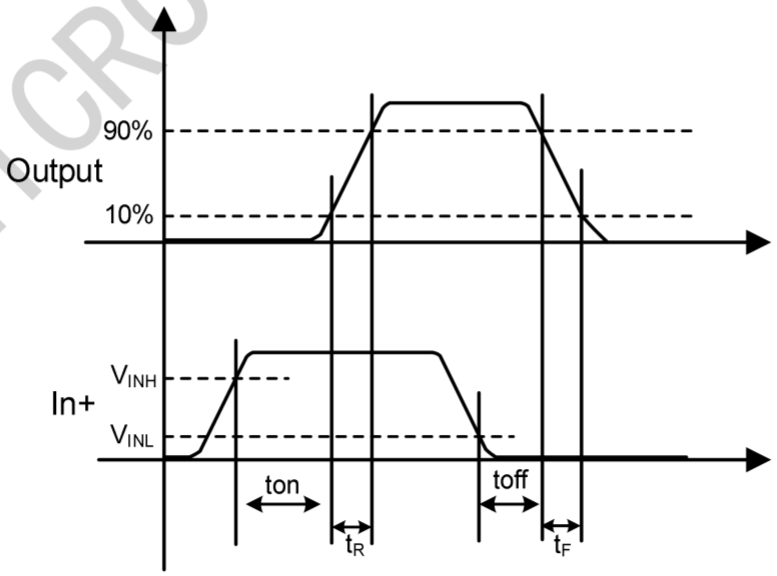

Figure 1 Input-Output waveform(non-inverting)

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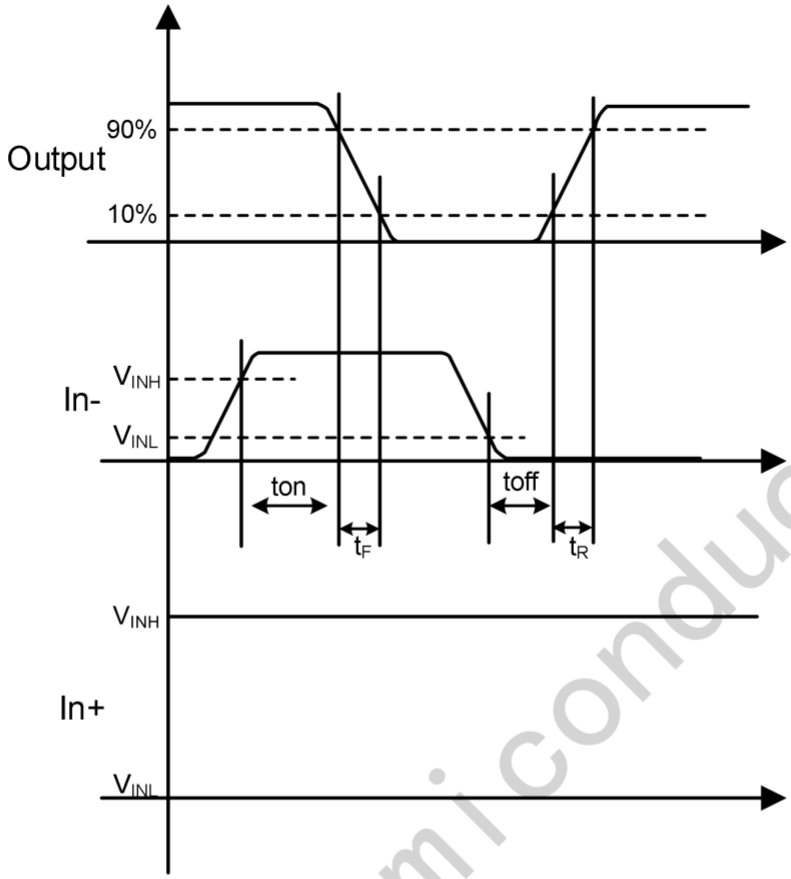

Figure 2 Input-Output waveform(inverting)

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5.5 Typical Characteristics

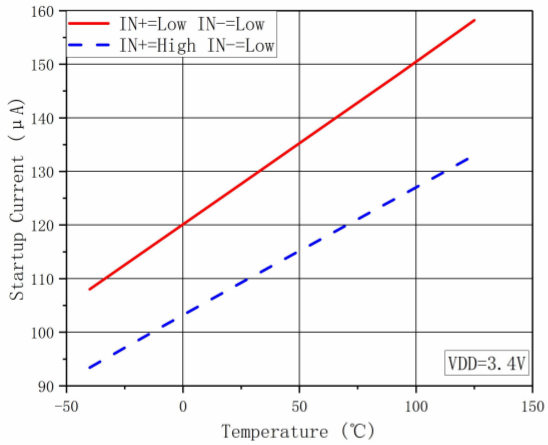


Figure 3. Start-Up Current vs Temperature

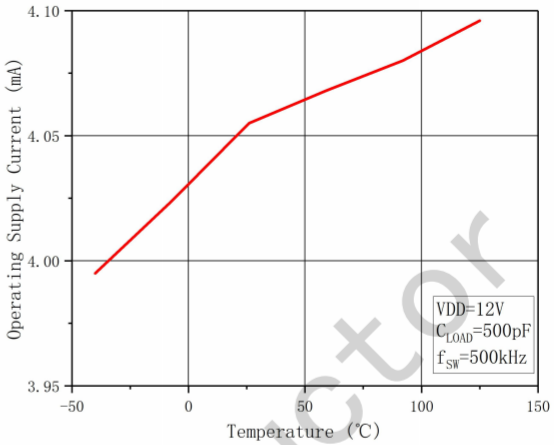
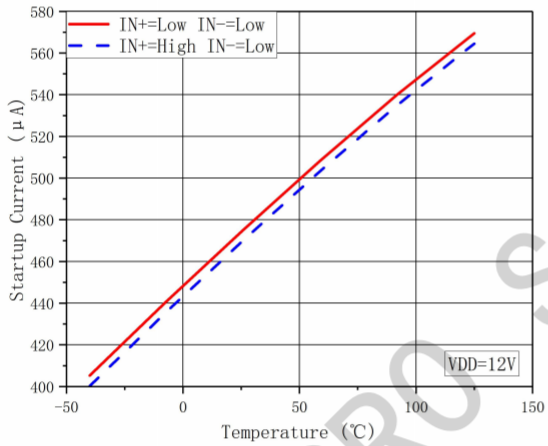


Figure 4. Operating Supply Current vs Temperature (Outputs Switching)



gure 5. Supply Current vs Temperature (Outputs In DC On/Off Condition)

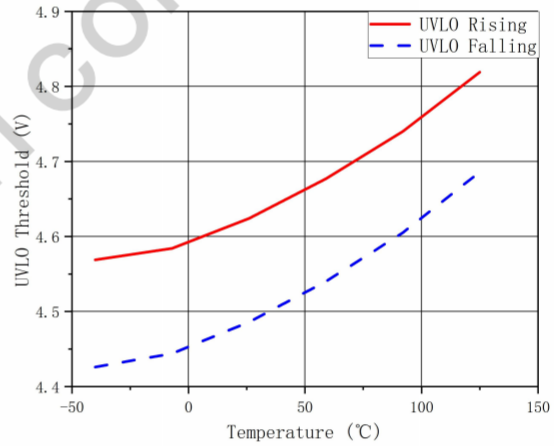


Figure 6. UVLO Threshold vs Temperature

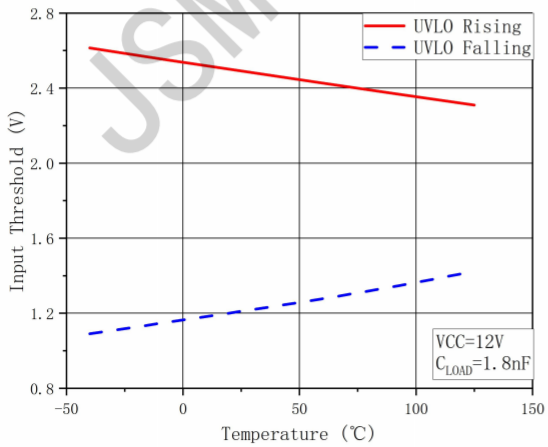


Figure 7. Input Threshold vs Temperature

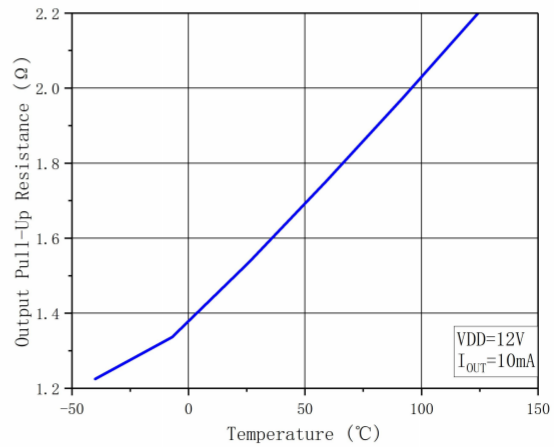


Figure 8. Output Pull-up Resistance vs Temperature

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Typical Characteristics(continued)

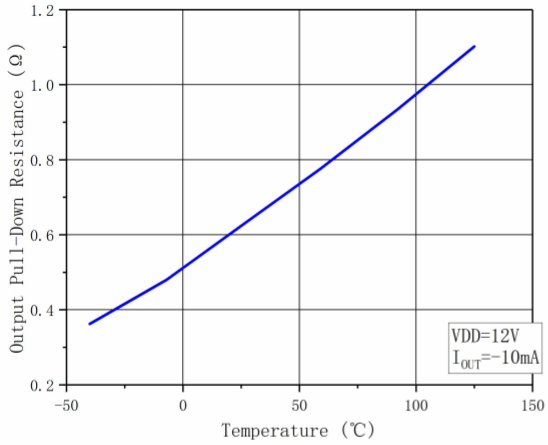

Figure 9. Output Pull-down Resistance vs Temperature

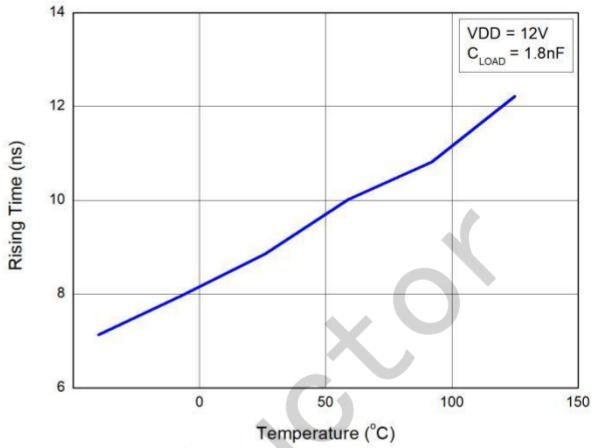

Figure 10. Rise Time vs Temperature

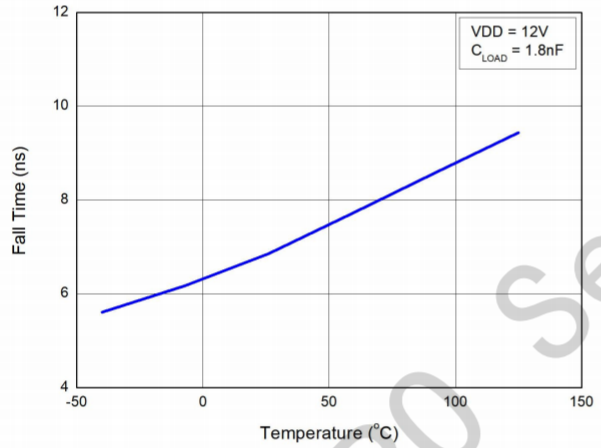

Figure 11. Fall Time vs Temperature

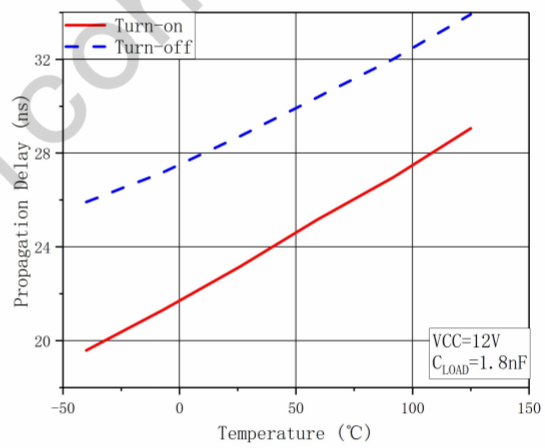

Figure 12. Input to Output Propagation Delay vs Temperature

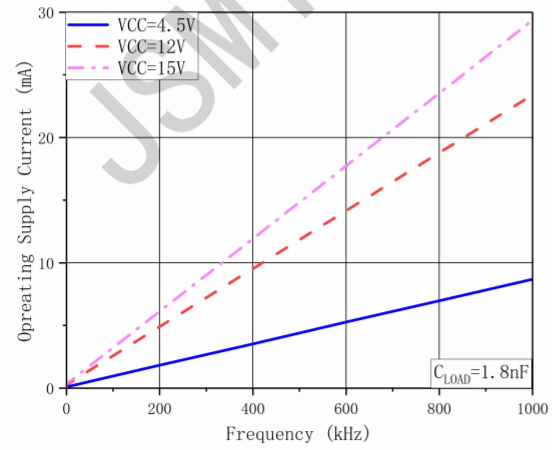

Figure 13. Operating Supply Current vs Frequency

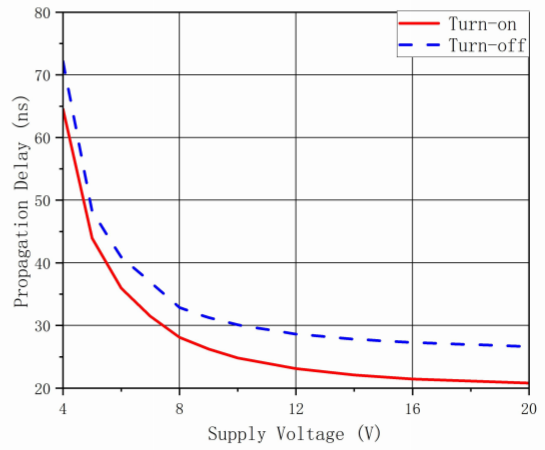

Figure 14. Propagation Delays vs Supply Voltage

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Typical Characteristics(continued)

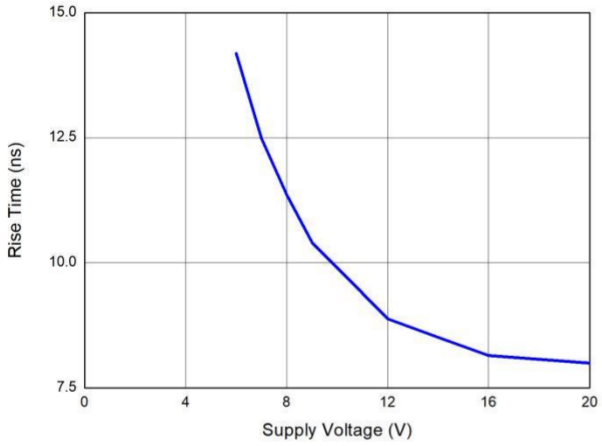

Figure 15. Rise Time vs Supply Voltage

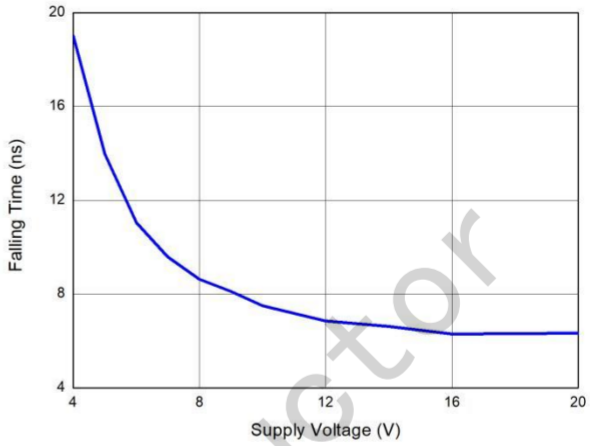

Figure 16. Fall Time vs Supply Voltage

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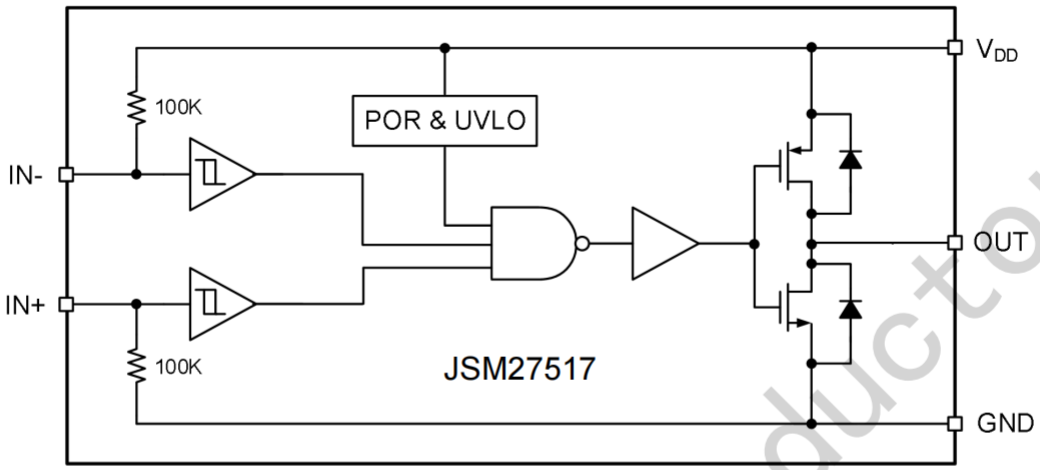
6 Detailed Description

6.1 Functional Block Diagram



6.2 Feature Description

6.2.1 VDD and Undervoltage Lockout

The JSM27517 devices have internal UVLO protection feature on the VDD-pin supply-circuit blocks. Whenever the driver is in UVLO condition (for example when VDD voltage is less than VCCUV+ during power up and when VDD voltage is less than VCCUV- during power down), this circuit holds all outputs LOW, regardless of the status of the inputs. The UVLO is typically 4.0 V with 100-mV typical hysteresis. This hysteresis helps prevent chatter when low VDD-supply voltages have noise from the power supply and also when there are droops in the VDD-bias voltage when the system commences switching and there is a sudden increase in IDD. The capability to operate at low voltage levels such as below 5 V, along with best-in-class switching characteristics, is especially suited for driving emerging GaN wide-bandgap power-semiconductor devices.

For example, at power up, the JSM27517 driver output remains LOW until the VDD voltage reaches the UVLO threshold. The magnitude of the OUT signal rises with VDD until steady-state VDD is reached. In the noninverting operation (PWM signal applied to IN+ pin) shown below, the output remains LOW until the UVLO threshold is reached, and then the output is in-phase with the input. In the inverting operation (PWM signal applied to IN- pin) shown below the output remains LOW until the UVLO threshold is reached, and then the output is out-phase with the input. In both cases, the unused input pin must be properly biased to enable the output. Note that in these devices the output turns to high-state only if IN+ pin is high and IN- pin is low after the UVLO threshold is reached..

Because the driver draws current from the VDD pin to bias all internal circuits, for the best high-speed circuit performance, two VDD bypass capacitors are recommended to prevent noise problems. The use of surfacemount components is highly recommended. A 0.1-μF ceramic capacitor should be located as close as possible to the VDD to GND pins of the gate driver. In addition, a larger capacitor (such as 1 μF) with relatively low ESR should be connected in parallel and close proximity, in order to help deliver the high-current peaks required by the load. The parallel combination of capacitors should present a low impedance characteristic for the expected current levels and switching frequencies in the application.

6.2.2 Operating Supply Current

The JSM27517 features very low quiescent I_{DD} currents. The total supply current is the sum of the quiescent I_{DD} current, the average I_{OUT} current due to switching and finally any current related to pull-up resistors on the unused input pin. For example when the inverting input pin is pulled low additional current is drawn from VDD supply through the pull-up resistors (refer to Functional Block Diagrams for the device Block Diagram). Knowing the operating frequency (f_{SW}) and the MOSFET gate (Q_G) charge at the drive voltage being used, the average I_{OUT} current can be calculated as product of Q_G and f_{SW}.

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6.2.3 Input Stage

The input pins of the JSM27517 devices are based on a TTL/CMOS compatible input-threshold logic that is independent of the VDD supply voltage. With typ high threshold = 2.7 V and typ low threshold = 0.8 V, the logic-level thresholds can be conveniently driven with PWM-control signals derived from 3.3-V and 5-V digital-power controllers. Wider hysteresis (typ 1 V) offers enhanced noise immunity compared to traditional TTLlogic implementations, where the hysteresis is typically less than 0.5 V. These devices also feature tight control of the input-pin threshold-voltage levels which eases system-design considerations and ensures stable operation across temperature. The very low input capacitance on these pins reduces loading and increases switching speed.

The device features an important safety function wherein, whenever any of the input pins are in a floating condition, the output of the respective channel is held in the low state. This is achieved using VDD-pullup resistors on all the inverting inputs (IN- pin) or GND-pulldown resistors on all the non-inverting input pins (IN+ pin), (refer to Functional Block Diagrams).

The device also features a dual-input configuration with two input pins available to control the state of the output. The user has the flexibility to drive the device using either a non-inverting input pin (IN+) or an inverting input pin (IN-). The state of the output pin is dependent on the bias on both the IN+ and IN- pins.

Once an input pin has been chosen for PWM drive, the other input pin (the unused input pin) must be properly biased in order to enable the output. As mentioned earlier, the unused input pin cannot remain in a floating condition because, whenever any input pin is left in a floating condition, the output is disabled for safety purposes. Alternatively, the unused input pin can effectively be used to implement an enable and disable function, as explained below.

• To drive the device in a non-inverting configuration, apply the PWM-control input signal to IN+ pin. In this case, the unused input pin, IN-, must be biased low (eg. tied to GND) in order to enable the output.

– Alternately, the IN- pin can be used to implement the enable/disable function using an external logic signal. OUT is disabled when IN- is biased high and OUT is enabled when IN- is biased low.

• To drive the device in an inverting configuration, apply the PWM-control input signal to IN- pin. In this case, the unused input pin, IN+, must be biased high (eg. tied to VDD) in order to enable the output.

– Alternately, the IN+ pin can be used to implement the enable/disable function using an external logic signal. OUT is disabled when IN+ is biased low and OUT is enabled when IN+ is biased high.

• Finally, note that the output pin is driven into a high state only when IN+ pin is biased high and IN- input is biased low.

The input stage of the driver should preferably be driven by a signal with a short rise or fall time. Caution must be exercised whenever the driver is used with slowly-varying input signals, especially in situations where the device is located in a mechanical socket or PCB layout is not optimal:

• High dI/dt current from the driver output coupled with board layout parasitics causes ground bounce. Because the device features just one GND pin, which may be referenced to the power ground, the differential voltage between input pins and GND is modified and triggers an unintended change of output state. Because of fast 13-ns propagation delay, high-frequency oscillations ultimately occur, which increases power dissipation and poses risk of damage.

• 1-V input-threshold hysteresis boosts noise immunity compared to most other industry-standard drivers.

• In the worst case, when a slow input signal is used and PCB layout is not optimal, adding a small capacitor (1nF) between input pin and ground very close to the driver device is necessary. This helps to convert the differential mode noise with respect to the input-logic circuitry into common-mode noise and avoid unintended change of output state.

If limiting the rise or fall times to the power device is the primary goal, then an external resistance is highly recommended between the output of the driver and the power device instead of adding delays on the input signal. This external resistor has the additional benefit of reducing part of the gate charge related power dissipation in the gate-driver device package and transferring the gate driver into the external resistor.

6.2.4 Enable Function

As mentioned earlier, an enable/disable function is easily implemented in the JSM27517 using the unused input pin. When IN+ is pulled down to GND or IN- is pulled down to VDD, the output is disabled. Thus IN+ pin is used like an enable pin that is based on active-high logic, while IN- can be used like an enable pin that is based on active-low logic.

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6.3 Device Functional Modes

Table 1 Device Logic Table

IN+	IN-	OUT
L	L	L
L	H	L
H	L	H
H	H	L
L	L	L
x(1)	Any	L
Any	x(1)	L

(1) Floating condition.

7 Applications and Implementation

7.1 Application Information

High-current gate-driver devices are required in switching power applications for a variety of reasons. In order to effect the fast switching of power devices and reduce associated switching-power losses, a powerful gate-driver device employs between the PWM output of control devices and the gates of the power semiconductor devices. Further, gate -driver devices are indispensable when it is not feasible for the PWM controller device to directly drive the gates of the switching devices. With the advent of digital power, this situation is often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal which is not capable of effectively turning on a power switch. A level-shifting circuitry is required to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) in order to fully turn on the power device and minimize conduction losses. Traditional buffer-drive circuits based on NPN/PNP bipolar transistors in a totem-pole arrangement, as emitter-follower configurations, prove inadequate with digital power because the traditional buffer-drive circuits lack level-shifting capability. Gate-driver devices effectively combine both the level-shifting and buffer-drive functions. Gate-driver devices also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controller devices by moving gate-charge power losses into the controller. Finally, emerging wide band-gap power-device technologies such as GaN based switches, which are capable of supporting very high switching frequency operation, are driving special requirements in terms of gate-drive capability. These requirements include operation at low VCC voltages (5 V or lower), low propagation delays, tight delay matching and availability in compact, low-inductance packages with good thermal capability. In summary, gate-driver devices are an extremely important component in switching power combining benefits of high-performance, low-cost, component-count, board-space reduction, and simplified system design.

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7.2 Typical Application

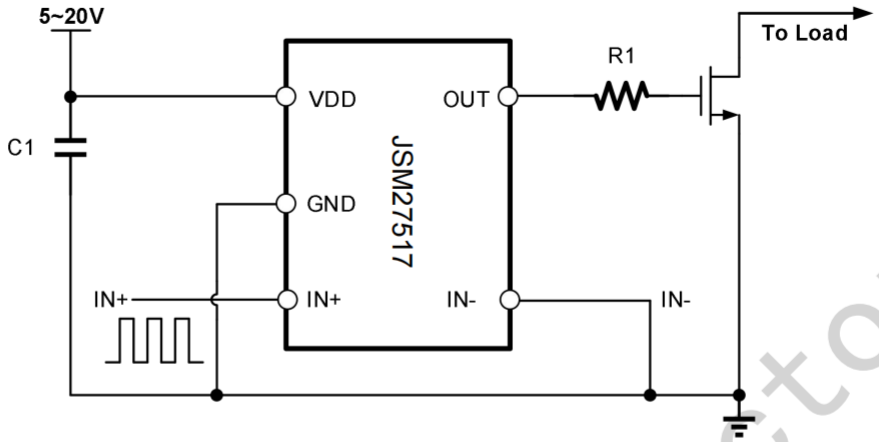

Figure 17 Non-inverting Typical Application Diagram of JSM27517

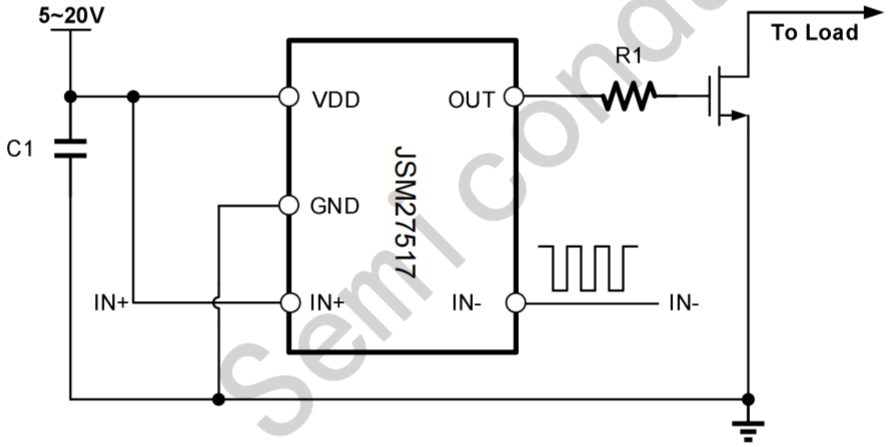

Figure 18 Inverting Typical Application Diagram of JSM27517

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7.2.1 Detailed Design Procedure

7.2.1.1 Input-to-Output Logic

The design should specify which type of input-to-output configuration should be used. If turning on the power MOSFET or IGBT when the input signal is in high state is preferred, then the non-inverting configuration must be selected. If turning off the power MOSFET or IGBT when the input signal is in high state is preferred, the inverting configuration must be chosen. The JSM27517 devices can be configured in either an inverting or non-inverting input-to-output configuration, using the IN– or IN+ pins, respectively. To configure the device for use in inverting mode, tie the IN+ pin to VDD and apply the input signal to the IN– pin. For the non inverting configuration, tie the IN– pin to GND and apply the input signal to the IN+ pin.

7.2.2.2 Input Threshold Type

The type of input voltage threshold determines the type of controller used with the gate driver device. The JSM27517 devices feature a TTL and CMOS-compatible input threshold logic, with wide hysteresis. The threshold voltage levels are low voltage and independent of the VDD supply voltage, which allows compatibility with both logic-level input signals from microcontrollers, as well as higher-voltage input signals from analog controllers. See Electrical Characteristics for the actual input threshold voltage levels and hysteresis specifications for the JSM27517 devices.

7.2.2.3 VDD Bias Supply Voltage

The bias supply voltage to be applied to the VDD pin of the device should never exceed the values listed in the Recommended Operating Conditions table. However, different power switches demand different voltage levels to be applied at the gate terminals for effective turnon and turnoff. With certain power switches, a positive gate voltage may be required for turnon and a negative gate voltage may be required for turnoff, in which case the VDD bias supply equals the voltage differential. With a wide operating range from 5.0 V to 20 V, the JSM27517 devices can be used to drive a variety of power switches, such as Si MOSFETs (for example, VGS = 4.5 V, 10 V, 12 V), IGBTs (VGE = 15 V, 18 V), and wide-band gap power semiconductors (such as GaN, certain types of which allow no higher than 6 V to be applied to the gate terminals).

7.2.2.4 Peak Source and Sink Currents

Generally, the switching speed of the power switch during turn-on and turn-off should be as fast as possible, to minimize switching power losses. The gate driver device must be able to provide the required peak current for achieving the targeted switching speeds for the targeted power MOSFET.

If the parasitic trace inductance limits the dI/dt, then a situation may occur in which the full peak current capability of the gate driver is not fully achieved in the time required to deliver the Q_G required for the power MOSFET switching. In other words, the time parameter in the equation would dominate and the I_{PEAK} value of the current pulse would be much less than the true peak current capability of the device, while the required Q_G is still delivered. Because of this, the desired switching speed may not be realized, even when theoretical calculations indicate the gate driver is capable of achieving the targeted switching speed. Thus, placing the gate driver device very close to the power MOSFET and designing a tight gate drive-loop with minimal PCB trace inductance is important to realize the full peak-current capability of the gate driver.

7.2.2.5 Enable and Disable Function

Certain applications demand independent control of the output state of the driver, without involving the input signal. A pin offering an enable and disable function achieves this requirement. The JSM27517 devices offer two input pins, IN+ and IN–, both of which control the state of the output as listed in table 1. Based on whether an inverting or non inverting input signal is provided to the driver, the appropriate input pin can be selected as the primary input for controlling the gate driver. The other unused input pin can be used for the enable and disable functionality. If the design does not require an enable function, the unused input pin can be tied to either the VDD pin (in case IN+ is the unused pin), or GND (in case IN– is unused pin) to ensure it does not affect the output status.

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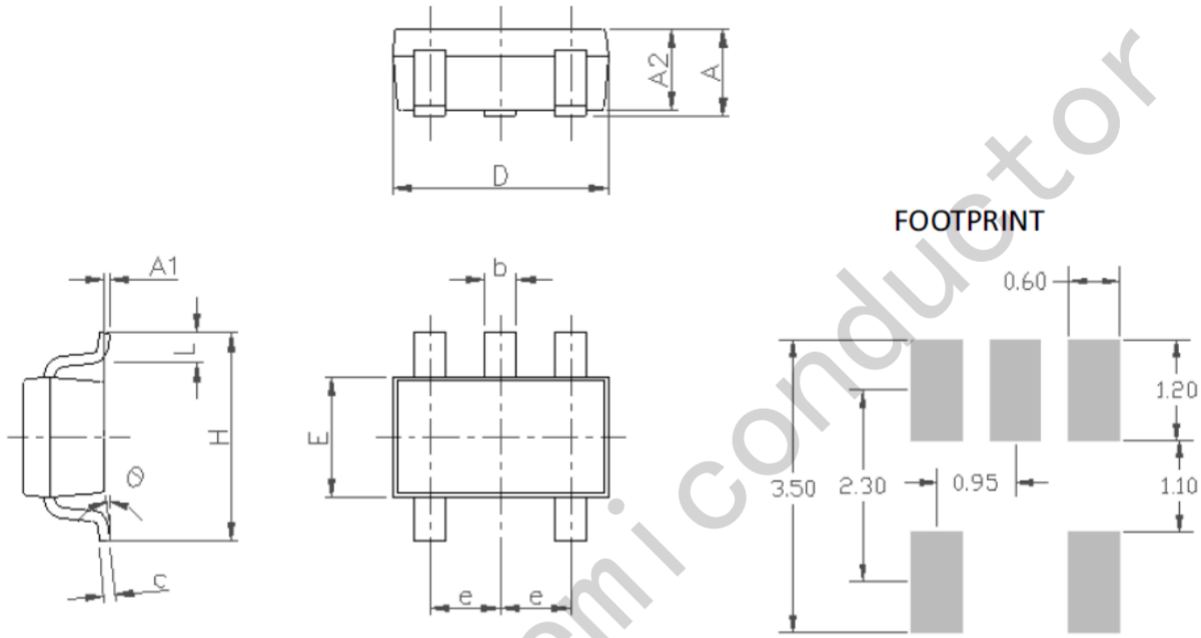
8 PACKAGING INFORMATION

SOT23-5 Package Outlines



SOT23-5 Package Dimensions

Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)	Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)
A	0.9	-	1.45	E	1.50	-	1.75
A1	0.00	-	0.15	e	-	0.95	-
A2	0.90	-	1.30	H	2.60	-	3.00
b	0.30	-	0.50	L	0.30	-	0.60
c	0.09	-	0.20	θ	0.00	-	10.00
D	2.80	-	3.05				

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