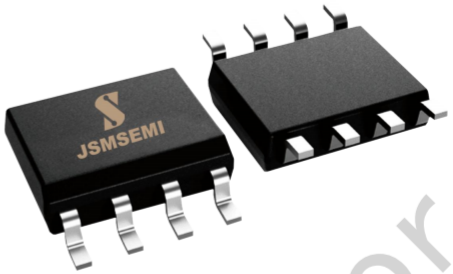
1 Description

The JSM2101S is a high voltage, high speed power MOSFET drivers with dependent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET in the high-side configuration which operates up to 700V.



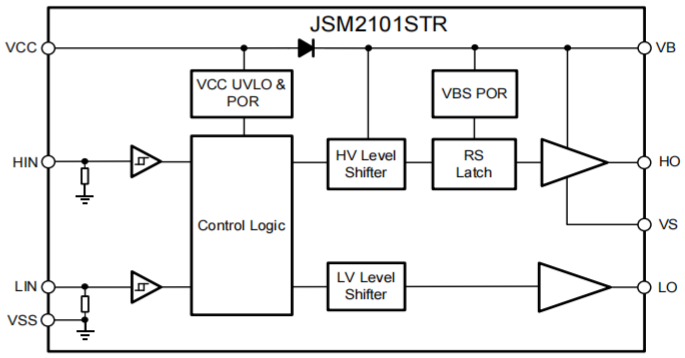
2 Features and Benefits

- Floating channel designed for bootstrap operation
- Fully operational to +700V
- 3.3V, 5V and 15V input logic compatible
- dV/dt noise Immunity ±50 V/nsec
- Allowable negative Vs capability: -9V
- Gate drive supply range from 10V to 20V
- Undervoltage lockout for both channels
  --UVLO forward 8.9V
  --UVLO reverse 8.2V
- Propagation delay
  --Ton/Toff =130ns/130ns
  --Matching delay time 50ns
- Wide operating temperature range -40°C ~125°C
- Typically output Source/Sink current capability: 300mA/600mA
- Integrated Bootstrap diode
- RoSH compatible

3 Application

- Motor Control
- Air Conditioners/ Washing Machines
- General Purpose Inverters
- Micro/Mini Inverter Drives
- Home Appliance

Functional Block Diagram



4 Function Pin Description

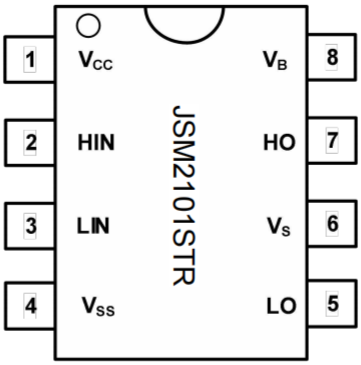


Table4-1 Lead Definitions

Number	Symbol	Description
1	V_{CC}	Low side and logic fixed supply
2	HIN	Logic input for high side gate driver output (HO), in phase
3	LIN	Logic input for low side gate driver output (LO), in phase
4	V_{SS}	Low side return
5	LO	Low side gate drive output
6	V_S	High side floating supply return
7	HO	High side gate drive output
8	V_B	High side floating supply

5 Product specifications

5.1 Absolute Maximum Ratings

Exceeding the limit maximum rating may cause permanent damage to the device. All voltage parameters are rated with reference to VSS and an ambient temperature of 25°C.

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply	-0.3	725	V
V_S	High side floating supply return	V_B - 25	V_B + 0.3	
V_{HO}	High side gate drive output	V_S -0.3	V_B + 0.3	
V_{CC}	Low side and main power supply	-0.3	25	
V_{LO}	Low side gate drive output	-0.3	V_{CC} + 0.3	
V_{IN}	Logic input of HIN & LIN	-0.3	V_{CC} + 0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient	—	50	V/ns

5.2 ESD rating

Symbol	Definition	MIN.	MAX.	Units
ESD	HBM Model	1500	—	V
	Machine Model	500	—	V

5.3 Rated power

Symbol	Definition	MIN.	MAX.	Units
P_D	Package Power Dissipation @ TA ≤25°C	—	625	mW

5.4 Thermal information

Symbol	Definition	MIN.	MAX.	Units
Rth_{JA}	Thermal Resistance, Junction to Ambient	--	200	°C/W
T_J	Junction Temperature	—	150	°C
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

5.5 Recommended Operating Conditions

For proper operation, the device should be used under the following recommended conditions. The bias ratings of VS and VSS are measured at a supply voltage of 15V, and unless otherwise specified, the ratings of all voltage parameters are referenced to VSS and the ambient temperature is 25°C.

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply	VS + 10	VS + 20	V
V_S	High side floating supply return	-9	700	
V_{HO}	High side gate drive output	V_S	V_B	
V_{CC}	Low side and main power supply	10	20	
V_{LO}	Low side gate drive output	0	V_{CC}	
V_{IN}	Logic input of HIN & LIN	0	V_{CC}	
T_A	Ambient temperature	-40	125	°C

Note1：Transient negative VS can be used for VSS-50V with a pulse width of 50ns, guaranteed by design..

Note2：When the input pulse width is less than 1us, the input pulse cannot be transmitted normally .

5.6 Electrical Characteristics

Valid for temperature range at T_A= 25°C, V_{CC}=V_B= 15V, C_L=1nF, unless otherwise specified

5.6.1 Dynamical electrical characteristics

Symbol	Definition	MIN.	TYP.	MAX.	Units	Test Condition
t_{ON}	Turn-on propagation delay	—	130	220	ns	V_S=0/700V
t_{OFF}	Turn-off propagation delay	—	130	220	ns	V_S=0V
t_R	Turn-on rise time	—	75	170	ns	
t_F	Turn-off fall time	—	35	70	ns	
MT	Matching delay ON and OFF	—	—	50	ns	

5.6.2 Static electrical characteristics

Valid for temperature range at T_A= 25°C, V_{CC}=V_B= 15V, C_L=1nF, unless otherwise specified.

Symbol	Definition	MIN.	TYP.	MAX.	Units	Test Condition
V_{CCUV+}	VCC supply UVLO threshold	8	8.9	9.8	V	
V_{CCUV-}		7.4	8.2	9.0	V	
$V_{CCUVHYS}$	hysteresis of V_{CC} UVLO	—	0.7	—	V	
I_{LK}	High-side floating supply leakage current	—	—	50	μA	V_B=V_S=700V
I_{QBS}	Quiescent VB supply current	—	50	100	μA	V_{IN}=0V or 5V
I_{QCC}	Quiescent VCC supply current	—	120	240	μA	V_{IN}=0V or 5V
V_{IH}	Logic “1”(HIN&LIN) input voltage	2.5	—	—	V	VCC=10Vto 20V
V_{IL}	Logic “0” (HIN&LIN) input voltage	—	—	0.8	V	VCC=10Vto 20V
V_{OH}	High level output voltage, VBIAS - VO	—	—	0.1	V	I_O=0A
V_{OL}	Low level output voltage, VO	—	—	0.1	V	I_O=0A
I_{IN+}	Logic “1” Input bias current	—	5	10	μA	IN=5V, SD=5V
I_{IN-}	Logic “0” Input bias current	—	—	2	μA	IN=0V, SD=0V
I_{O+}	Output high short circuit pulsed current	200	300	—	mA	V_O=0V PW≤10us
I_{O-}	Output low short circuit pulsed current	400	600	—	mA	V_O=15V PW≤10us

6 Function Description

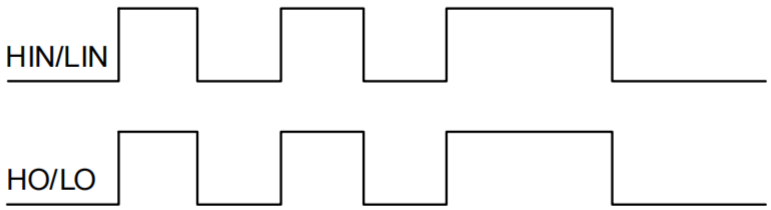


Figure 5. JSM2101S Input and output timing waveform

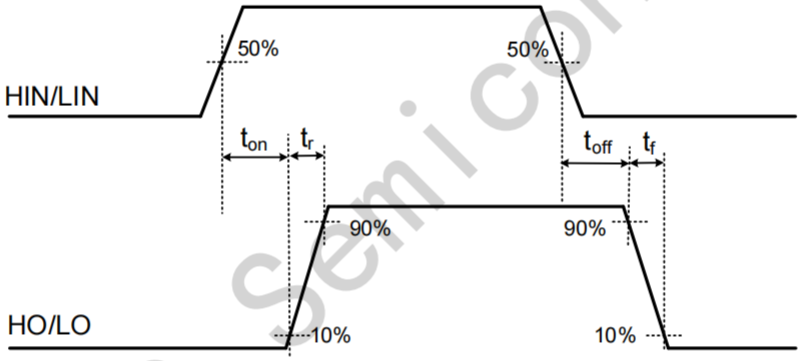


Figure 6. Propagation Time Waveform Definition

7 JSM2101STR Description

7.1 Function Block Diagram

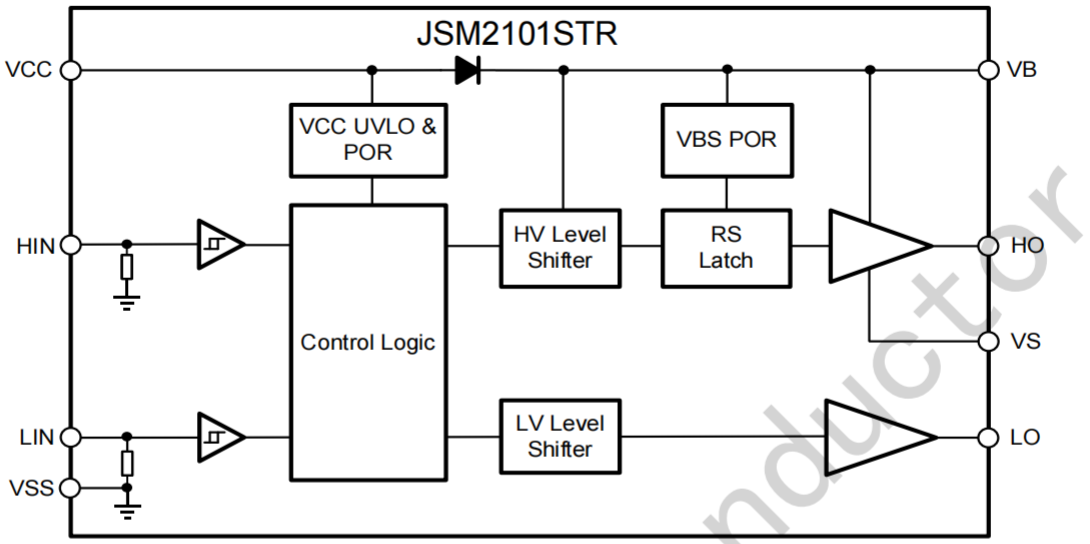


Figure7-1 Function Block Diagram of JSM2101S

7.2 Application message

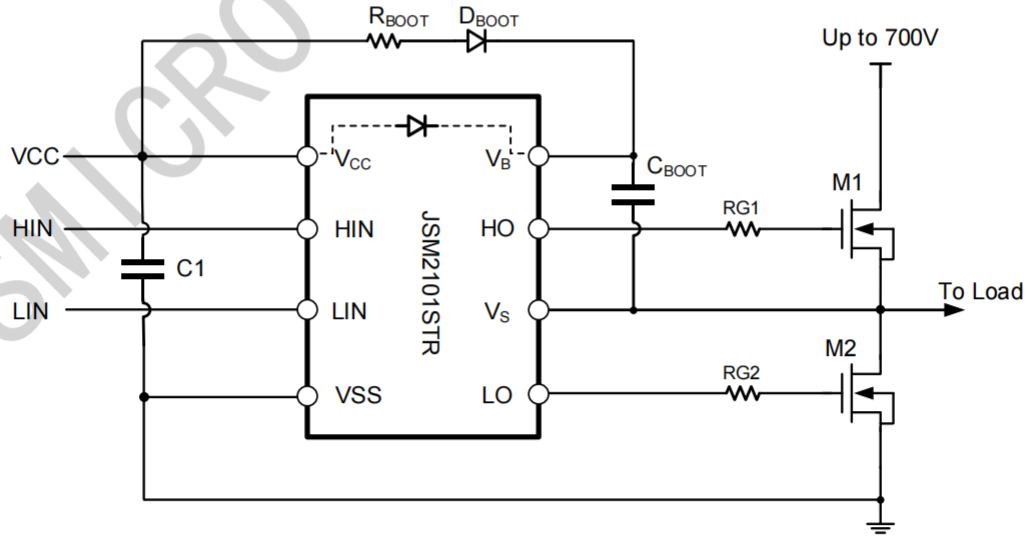


Figure7-2 Typical application circuit of JSM2101STR

7.2 Guide for bootstrap circuit design

The structure in the general half-bridge circuit is shown in Figure Figure 7-2, including three parts: bootstrapping resistance, bootstrap diode and bootstrap capacitance. This scheme is the most commonly used and the most cost-effective scheme in the current motor drive.

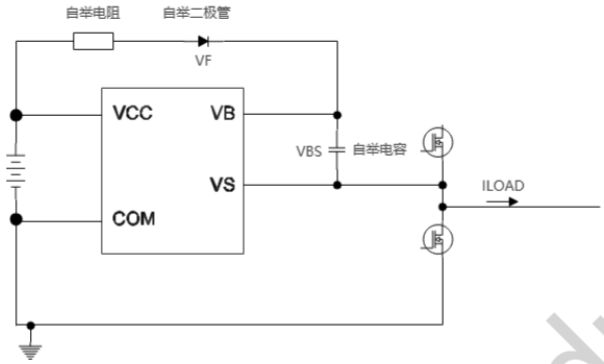


Figure 7-2 Basic structure of the bootstrap circuit

Selection of capacitance for bootstrap circuits

To determine the size of the bootstrap capacitor, we first need to evaluate the following points:

-The gate charge Qg required for MOS activation;

-GS leakage ILK_GS of MOS;

-The static working current IQBS of the drive;

-Leakage ILK-DIODE of bootstrap diode;

-Self bootstrap capacitor leakage ILK-CAP;

-Upper bridge setting high time THON

When the bootstrap capacitor uses an electrolytic capacitor, ILK-CAP will be included in the calculation value, and other types of capacitors do not need to be considered. It is recommended to use at least one low ESR ceramic capacitor here. Parallel electrolytic capacitors and low ESR ceramic capacitors can achieve better circuit operating characteristics.

By calculation, we can obtain the capacitance value required for a single opening:

$$Q_{TOT} = Q_G + (I_{LK\_GS} + I_{QBS} + I_{LK\_DIODE} + I_{LK\_CAP}) \times T_{HON}$$

During the bootstrapping process, the range of VBS descent $\triangle V_{BS}$

$$\Delta V_{BS} \leq V_{CC} - V_F - V_{GSmin} - V_{DSon}$$

During this process, it is necessary to ensure that:

$$V_{GSmin} > V_{BSUV-}$$

V_F Reverse diode voltage drop of MOS

V_{GEmin} maintains the minimum gate voltage for MOSFET conduction

V_{DSon} Conduction voltage drop of VDSon bridge MOS

Based on the above results, it can be calculated that:

$$C_{BOOTmin} = \frac{Q_{TOT}}{\triangle V_{BS}}$$

Note: In the process of calculating the bootstrap capacitor here, only the amount of charge required for one pulse process was calculated, without considering issues such as PWM duty cycle and frequency. If the signal is

bootstrap capacitance size through a certain equivalent conversion.

Precautions for bootstrap circuits

A. Bootstrap resistor

Bootstrap resistors are used in some bootstrap circuits and are not mandatory components. During startup, HO and LO may experience abnormal jumps. Increasing the bootstrap resistor will limit the current passing through the bootstrap diode during the bootstrap circuit startup, effectively suppressing some adverse signals and protecting the circuit.

B. Bootstrap capacitor

In the circuit design where the upper bridge arm is opened for a long time, the use of electrolytic capacitors as bootstrap capacitors must consider ESR. Long term opening of the upper bridge arm requires a bootstrap capacitor with a larger capacitance value, and electrolytic capacitors are generally used more often. However, electrolytic capacitors have a certain internal resistance, which can reduce the voltage division of the bootstrap resistor and prevent them from achieving their functions. Parallel connection of a low ESR ceramic capacitor can effectively prevent this situation from occurring.

C. Bootstrap diode

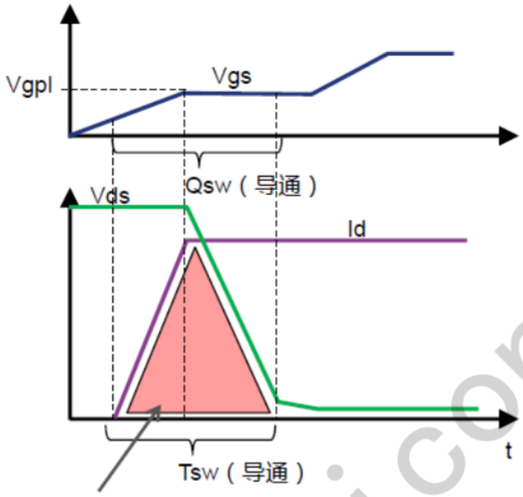
Bootstrap diodes are used to maintain voltage stability in bootstrap circuits. It is necessary to ensure that the reverse withstand voltage of the diode is greater than the driving power voltage, and on this basis, fast recovery diodes such as Schottky diodes should be selected as much as possible.

7.3 Bootstrap Circuit Design Guidelines

The gate resistor is used to control the switching speed and the slope of the rising and falling edges of the driven MOS, which can affect multiple performance factors in applications such as loss and reliability. This section will describe how to choose a driving resistor and discuss the impact it brings. The selection of gate resistance is closely related to the driving chip, MOSFET, and even circuit design used, and needs to be re selected according to the actual situation in different environments.

The common operating frequency of industrial brushless motors is about 2kHz -10kHz. Based on this, gate resistors with a resistance value of 20 Ω -120 Ω are usually chosen. This is determined by the following two points:

(1) The switching loss of MOS. The loss of MOS is partly due to switching loss and partly due to conduction loss. The gate resistance mainly affects the loss of the switching process. The larger the resistance value, the slower the switching process, and the larger the overlap area of voltage and current, the greater the loss. The most direct impact of excessive loss is that it will cause the chip temperature to rapidly rise, and under conditions above 150 , it will put the device at risk of failure.



$$Psw(on) = \frac{1}{2} \times Id \times Vds \times Tsw(on)$$

Figure 7-3 MOS switch losses under resistive load conditions

(2) Reliability. Contrary to losses, the smaller the resistance of the gate resistance, the faster the switching speed of MOSFETs. In practical applications, the power terminal current is relatively large and sensitive to parasitic parameters. Excessive switching speed can increase signal instability, ranging from excessive EMI of the motor to circuit damage. The most common ones are:

1) The gate signal rings, causing MOS damage (as shown in Figure 7-4);

2) The dv/dt is too fast, causing the VS port to withstand high or low voltage signals, resulting in drive damage.

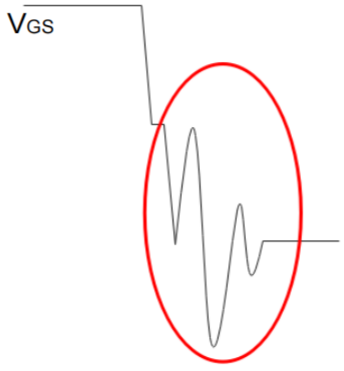


Figure 7-4 Gate Ringing Phenomenon

7.4 PCB Layout Guidelines

To achieve excellent performance of the half bridge gate driver chip, the following printed circuit board (PCB) layout and wiring guidelines should be followed.• Low ESR/ESL capacitors should be placed between the VCC and COM pins near the driver chip, as well as between the VB and VS pins, to provide the peak current of the VCC and VB pins.

• To prevent large voltage transients in the high side MOSFET drain, it is necessary to connect a low ESR electrolytic capacitor and a ceramic capacitor between the high side MOSFET drain and ground (COM).

• To avoid excessive voltage negative transients on the switch node (VS) pins, it is necessary to minimize the parasitic inductance between the high side MOSFET source and the low side MOSFET (synchronous rectifier) source as much as possible.

• Efforts should be made to avoid overlapping between the VS layer and the ground (COM) layer, in order to minimize the coupling of switch noise from the VS layer to the ground layer to a greater extent.

• The heat dissipation pads of the driver chip should be connected to a large area of thick copper layer to improve the heat dissipation performance of the driver chip. Heat dissipation pads are usually connected to a ground plane that is equipotential with the chip COM. It is recommended to only connect this heat dissipation pad to the COM pins.

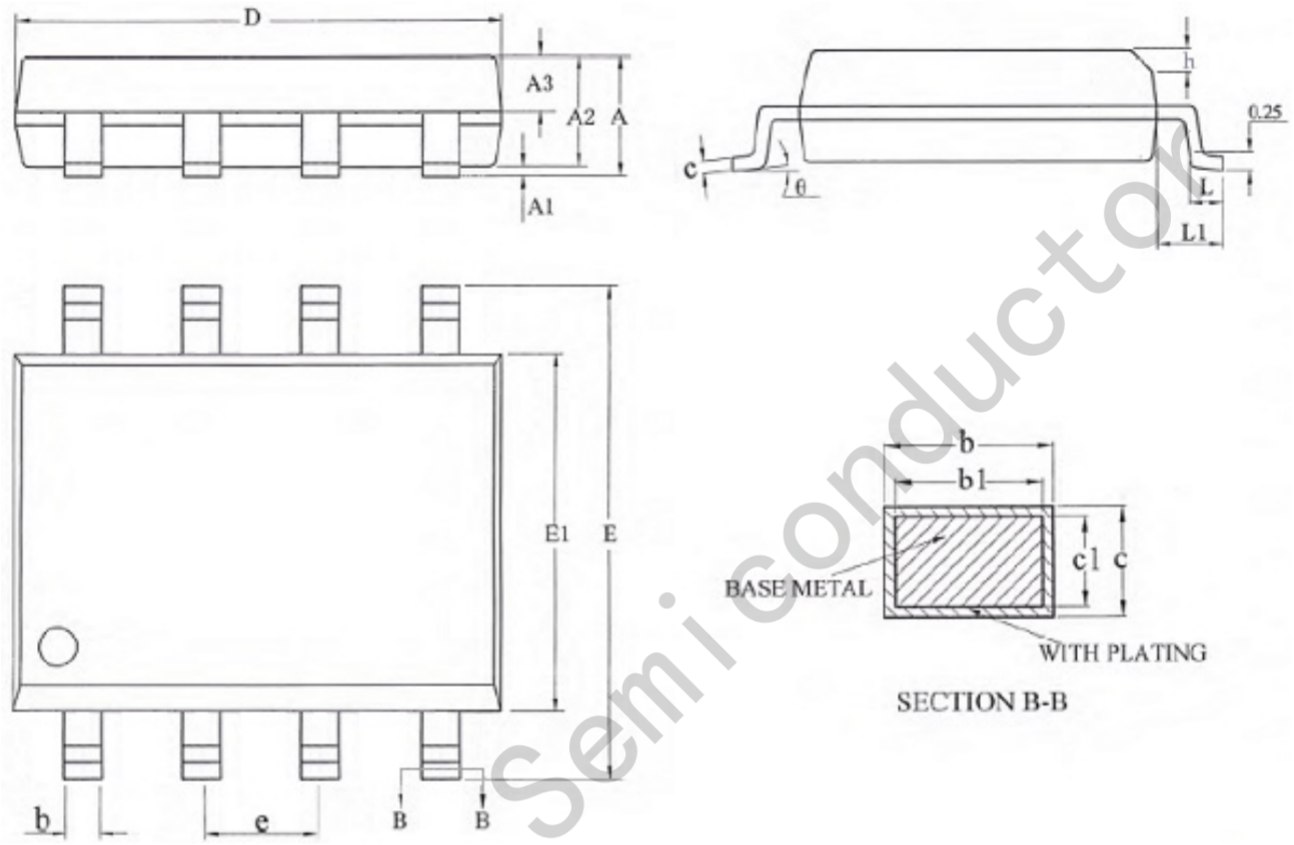
• Grounding precautions:

The primary goal of designing grounding connections is to limit the MOSFET gate charge discharge circuit to the smallest possible loop area. This method reduces the loop inductance and effectively avoids noise issues on the MOSFET gate. Meanwhile, the gate driver chip should be as close as possible to the MOSFET.

The second consideration is to ensure the rationality of the charging path for the bootstrap capacitor, which includes VCC bypass capacitors based on ground (COM), bootstrap diodes, bootstrap capacitors, and low side MOSFET body diodes. Due to the VCC bypass capacitor charging the bootstrap capacitor cycle by cycle through the bootstrap diode, and each charging occurs in a very short time, the charging path will pass through the peak current. Minimizing the loop length and area of the bootstrap circuit on the PCB as much as possible can ensure that the bootstrap circuit operates in a stable state, which is crucial for ensuring the reliable operation of the driver chip.

8 Package Information

SOIC-8 Package Outlines



SOIC-8 Package Dimensions

Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)	Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)
A	-	-	1.75	D	4.70	4.90	5.10
A1	0.10	-	0.225	E	5.80	6.00	6.20
A2	1.30	1.40	1.50	E1	3.70	3.90	4.10
A3	0.60	0.65	0.70	e		1.27BSC	
b	0.39	-	0.48	h	0.25	-	0.50
b1	0.38	0.41	0.43	L		0.50	
c	0.21	-	0.26	L1	1.05BSC		
c1	0.19	0.20	0.21	θ	0	-	8°