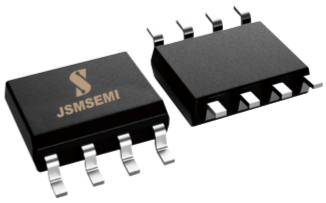
1 Description

The JSM5108G is a high voltage，high speed power MOSFET drivers with dependent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET in the high-side configuration which operates up to 200 V.



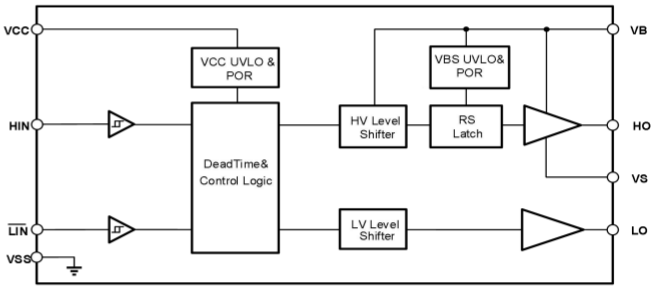
2 Features and Benefits

- Floating channel designed for bootstrap operation
- Fully operational to +250 V
- 3.3V, 5V and 15V input logic compatible
- dV/dt noise Immunity ±50 V/nsec
- Allowable negative Vs capability: -9V
- Gate drive supply range from 6 V to 20V
- Cross-conduction prevention logic
- -- Deadtime:200ns
- Matched propagation delay for both channels
- Wide operating temperature range -40°C ~125°C
- Typically output Source/Sink current capability: 1.2A/1.5A
- RoSH compatible

3 Application

- Motor Control
- Air Conditioners/ Washing Machines
- General Purpose Inverters
- Micro/Mini Inverter Drives

Functional Block Diagram



4 Function Pin Description

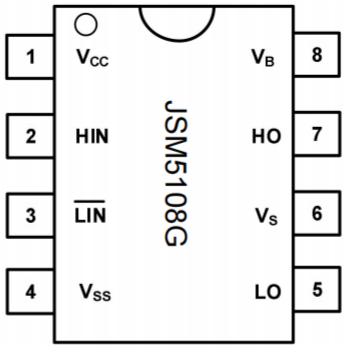


Figure4-1 8-Pin SOIC8 Top view

Table 4-1 Lead Definitions

Number	Symbol	Description
1	V_{CC}	Low side and logic fixed supply
2	HIN	Logic input for high side gate driver output (HO), in phase
3	$\overline{LIN}$	Logic input for low side gate driver output (LO), out of phase
4	V_{SS}	Low side return
5	LO	Low side gate drive output
6	V_S	High side floating supply return
7	HO	High side gate drive output
8	V_B	High side floating supply

5 Product specifications

5.1 Absolute Maximum Ratings

Exceeding the limit maximum rating may cause permanent damage to the device. All voltage parameters are rated with reference to VSS and an ambient temperature of 25°C.

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply	-0.3	275	V
V_S	High side floating supply return	V_B – 25	V_B + 0.3	
V_{HO}	High side gate drive output	V_S -0.3	V_B + 0.3	
V_{CC}	Low side and main power supply	-0.3	25	
V_{LO}	Low side gate drive output	-0.3	V_{CC} + 0.3	
V_{IN}	Logic input of HIN & $\overline{LIN}$	-0.3	V_{CC} + 0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient	—	50	V/ns

5.2 ESD rating

Symbol	Definition	MIN.	MAX.	Units
ESD	HBM Model	1500	—	V
	Machine Model	500	—	V

5.3 Rated power

Symbol	Definition	MIN.	MAX.	Units
P_D	Package Power Dissipation @ TA ≤25°C	—	625	mW

5.4 Thermal information

Symbol	Definition	MIN.	MAX.	Units
Rth_{JA}	Thermal Resistance, Junction to Ambient	--	200	°C/W
T_J	Junction Temperature	—	150	°C
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

5.5 Recommended Operating Conditions

For proper operation, the device should be used under the following recommended conditions. The bias ratings of VS and VSS are measured at a supply voltage of 15V, and unless otherwise specified, the ratings of all voltage parameters are referenced to VSS and the ambient temperature is 25°C.

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply	VS + 6	VS + 20	V
V_S	High side floating supply return	-9	250	
V_{HO}	High side gate drive output	V_S	V_B	
V_{CC}	Low side and main power supply	6	20	
V_{LO}	Low side gate drive output	0	V_{CC}	
V_{IN}	Logic input of HIN & $\overline{LIN}$	0	V_{CC}	
T_A	Ambient temperature	-40	125	°C

Note1：Transient negative VS can be used for VSS-50V with a pulse width of 50ns, guaranteed by design..

Note2：When the input pulse width is less than 1us, the input pulse cannot be transmitted normally .

5. 6 Electrical Characteristics

Valid for temperature range at T_A= 25ºC, V_{CC}=V_B= 15V, C_L=1nF, unless otherwise specified

5.6.1 Dynamical electrical characteristics

Symbol	Definition	MIN.	TYP.	MAX.	Units	Test Condition
t_{ON}	Turn-on propagation delay	—	150	250	ns	V_S=0V
t_{OFF}	Turn-off propagation delay	—	140	250	ns	V_S=250V
t_R	Turn-on rise time	—	50	100	ns	
t_F	Turn-off fall time	—	40	100	ns	
DT	Deadtime	—	200	--	ns	
MT	Matching delay ON and OFF	—	—	50	ns	

5.6.2 Static electrical characteristics

Valid for temperature range at T_A= 25ºC, V_{CC}=V_B= 15V, C_L=1nF, unless otherwise specified.

Symbol	Definition	MIN.	TYP.	MAX.	Units	Test Condition
V_{CCUV+}	VCC supply UVLO threshold	—	5.5	—	V	
V_{CCUV-}		—	5.0	—	V	
I_{LK}	High-side floating supply leakage current	—	—	50	μA	V_B=V_S=250V
I_{QBS}	Quiescent VB supply current	—	40	120	μA	V_{IN}=0V or 5V
I_{QCC}	Quiescent VCC supply current	—	160	280	μA	V_{IN}=0V or 5V
V_{IH}	Logic “1”(HIN&$\overline{LIN}$) input voltage	2.5	—	—	V	
V_{IL}	Logic “0” (HIN&$\overline{LIN}$) input voltage	—	—	0.8	V	
V_{OH}	High level output voltage, VBIAS - VO	—	—	0.2	V	I_O=0A
V_{OL}	Low level output voltage, VO	—	—	0.1	V	I_O=0A
I_{IN+}	Logic “1” Input bias current	—	10	20	μA	HIN=5V, $\overline{LIN}$=0V
I_{IN-}	Logic “0” Input bias current	—	15	30	μA	HIN=0V, $\overline{LIN}$=5V
I_{O+}	Output high short circuit pulsed current	—	1.2	—	A	V_O=0V PW≤10us
I_{O-}	Output low short circuit pulsed current	—	1.5	—	A	V_O=15V PW≤10us

6 Function Description

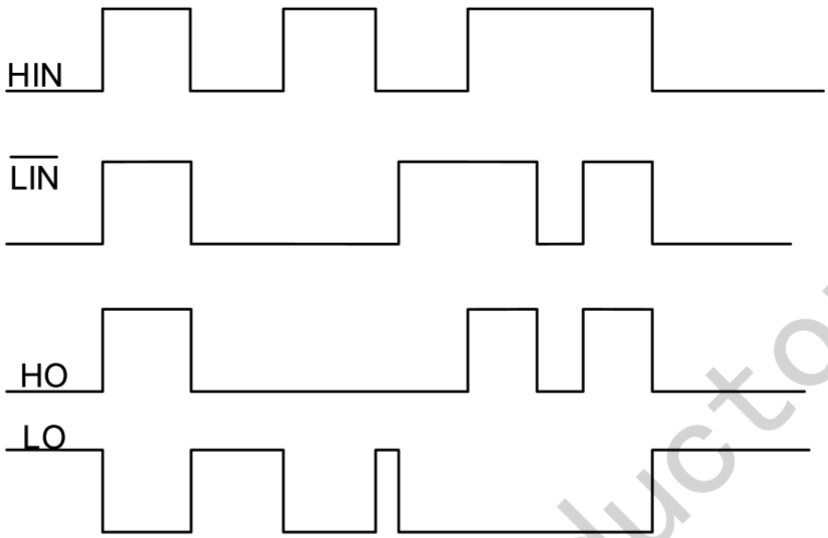


Figure 6-1 JSM5108GInput and output timing waveform

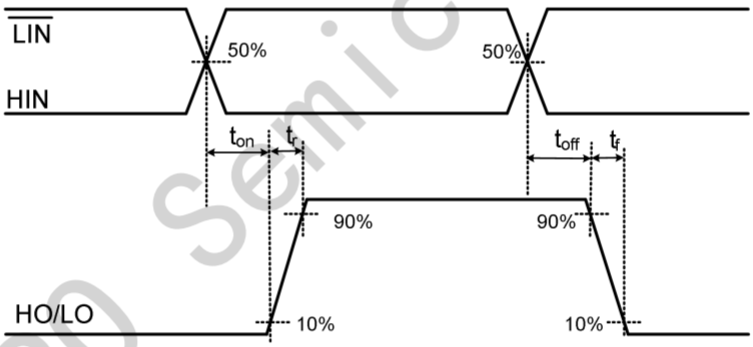


Figure 6-2 Propagation Time Waveform Definition

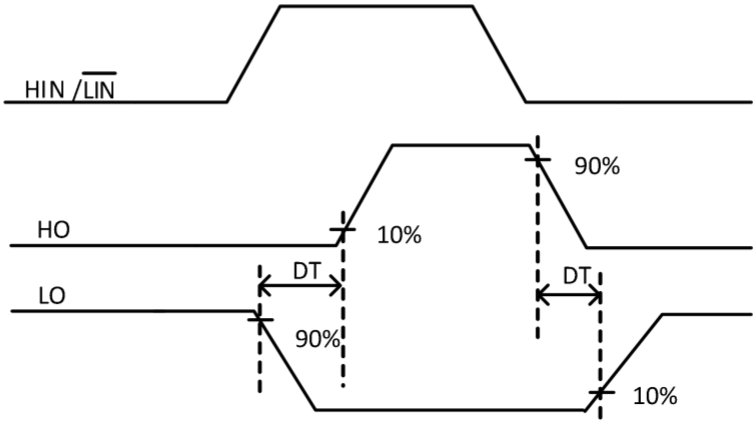


Figure 6-3 Cross Conduction Prevention Delay Time Waveform Definition

7 JSM5108G Description

7.1 Function Block Diagram

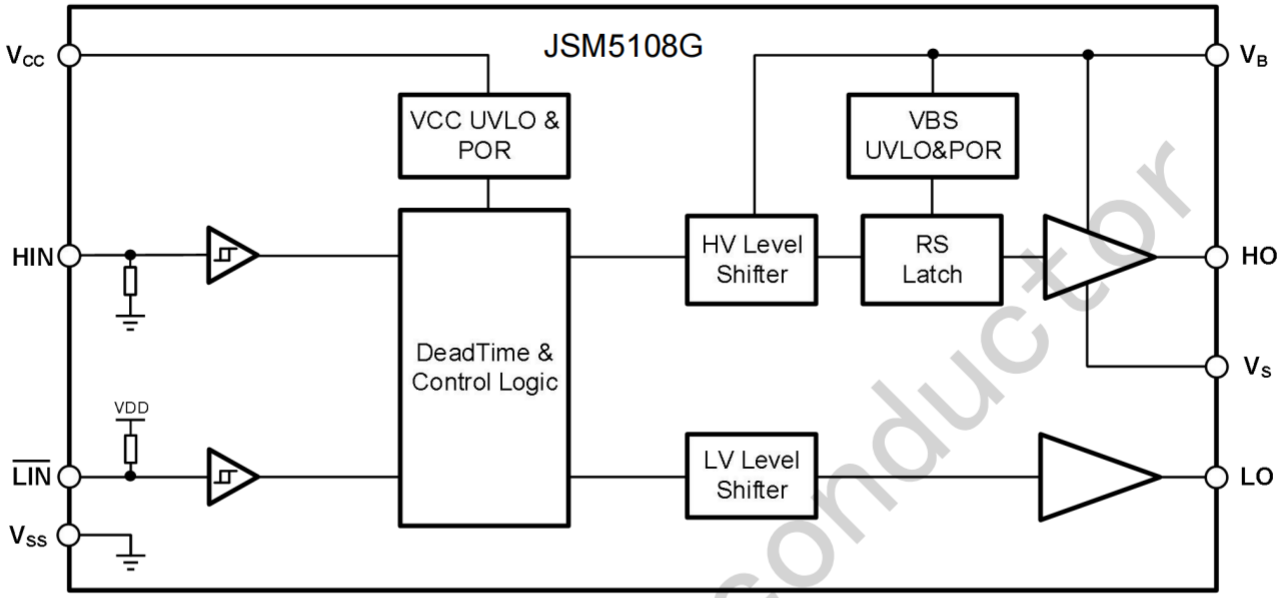


Figure 7-1 Function Block Diagram of JSM5108G

7.2 Chip operating logic

Table 7-1 I/O logical table

INPUT		OUTPUT	
HIN	LIN/	HO	LO
L	L	L	H
L	H	L	L
H	L	L	L
H	H	H	L
Note: H stands for high level; L stands for low level			

8 Application message

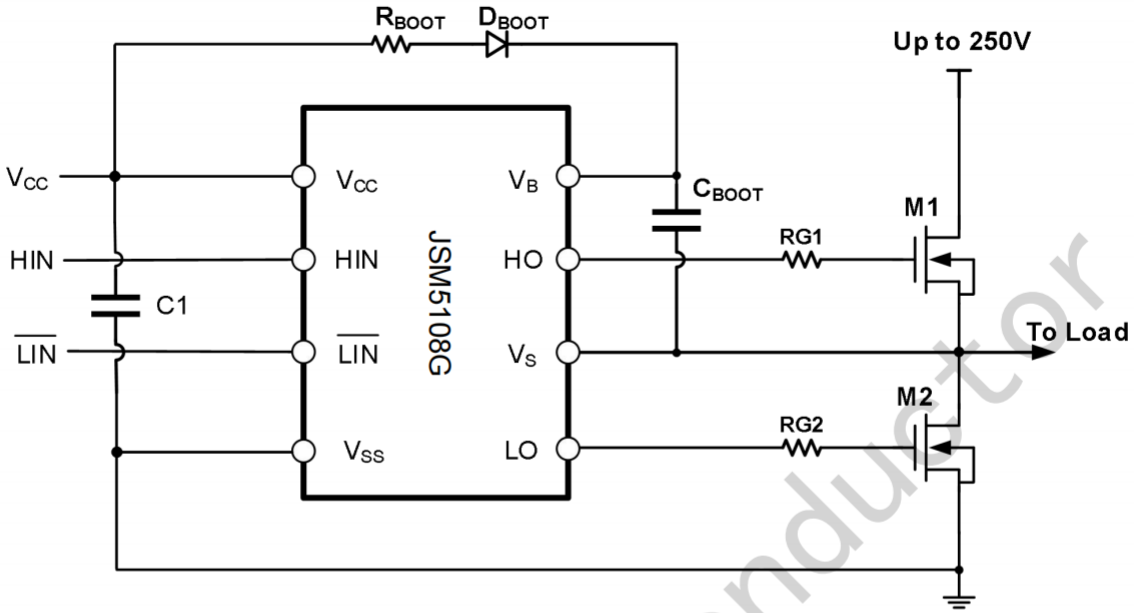
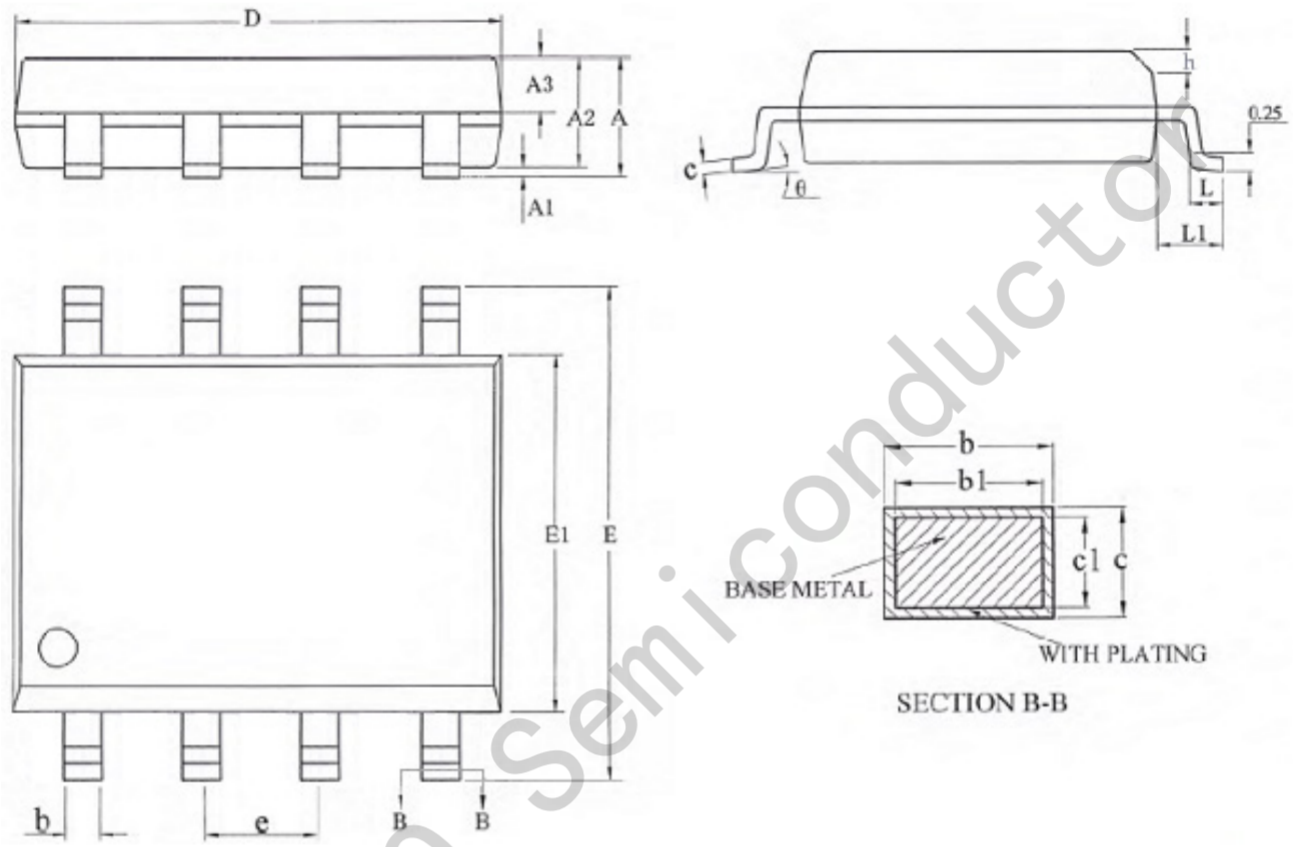


Figure 8-1 Typical application circuit of JSM5108G

SOIC-8 Package Outlines



SOIC-8 Package Dimensions

Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)	Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)
A	-	-	1.75	D	4.70	4.90	5.10
A1	0.10	-	0.225	E	5.80	6.00	6.20
A2	1.30	1.40	1.50	E1	3.70	3.90	4.10
A3	0.60	0.65	0.70	e		1.27BSC	
b	0.39	-	0.48	h	0.25	-	0.50
b1	0.38	0.41	0.43	L		0.50	
c	0.21	-	0.26	L1	1.05BSC		
c1	0.19	0.20	0.21	θ	0	-	8°