

P-Channel Enhancement Mode Power MOSFET

<p>Description</p> <p>The G100P04D5 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.</p> <p>General Features</p> <ul style="list-style-type: none"> ● V_{DS} -40V ● I_D (at $V_{GS} = -10V$) -55A ● $R_{DS(ON)}$ (at $V_{GS} = -10V$) < 10mΩ ● $R_{DS(ON)}$ (at $V_{GS} = -4.5V$) < 16mΩ ● 100% Avalanche Tested ● RoHS Compliant <p>Application</p> <ul style="list-style-type: none"> ● Power switch ● DC/DC converters 	<p>Schematic diagram</p> <p>pin assignment</p> <p>DFN5X6-8L</p>
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Ordering Information

Device	Package	Marking	Packaging
G100P04D5	DFN5X6-8L	G100P04	5000pcs/Reel

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-40	V
Continuous Drain Current	I_D	$T_C = 25^\circ\text{C}$	-55
		$T_C = 100^\circ\text{C}$	-35
Pulsed Drain Current (note1)	I_{DM}	-220	A
Gate-Source Voltage	V_{GS}	± 20	V
Power Dissipation	P_D	58	W
Single pulse avalanche energy (note2)	E_{AS}	132	mJ
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	$^\circ\text{C}$

Thermal Resistance

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient	R_{thJA}	50	$^\circ\text{C/W}$
Maximum Junction-to-Case	R_{thJC}	2.14	$^\circ\text{C/W}$

Specifications $T_J = 25^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-40	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -40V, V_{GS} = 0V$	--	--	-1	μA
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20V$	--	--	± 100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1.2	-1.7	-2.5	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -20A$	--	8.8	10	m Ω
		$V_{GS} = -4.5V, I_D = -20A$	--	13	16	
Forward Transconductance	g_{FS}	$V_{DS} = -5V, I_D = -20A$	--	41	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{GS} = 0V,$ $V_{DS} = -20V,$ $f = 1.0\text{MHz}$	--	2500	--	pF
Output Capacitance	C_{oss}		--	335	--	
Reverse Transfer Capacitance	C_{rss}		--	292	--	
Total Gate Charge	Q_g	$V_{DD} = -20V,$ $I_D = -20A,$ $V_{GS} = -10V$	--	58	--	nC
Gate-Source Charge	Q_{gs}		--	7	--	
Gate-Drain Charge	Q_{gd}		--	14	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = -20V,$ $I_D = -20A,$ $R_G = 3\Omega$	--	9	--	ns
Turn-on Rise Time	t_r		--	7	--	
Turn-off Delay Time	$t_{d(off)}$		--	19	--	
Turn-off Fall Time	t_f		--	9	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	$T_C = 25^\circ\text{C}$	--	--	-55	A
Body Diode Voltage	V_{SD}	$T_J = 25^\circ\text{C}, I_{SD} = -20A, V_{GS} = 0V$	--	--	-1.2	V
Reverse Recovery Charge	Q_{rr}	$I_F = -20A, V_{GS} = 0V$ $di/dt = -100A/\mu s$	--	36	--	nC
Reverse Recovery Time	T_{rr}		--	21	--	ns

Notes

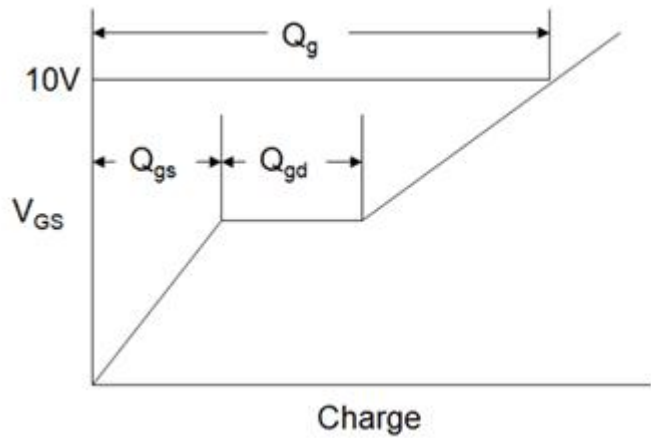
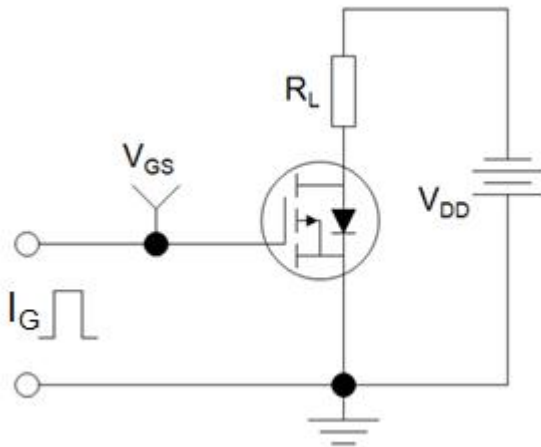
1. Repetitive Rating: Pulse width limited by maximum junction temperature

2. EAS condition : $T_J = 25^\circ\text{C}, V_{DD} = -40V, V_{GS} = -10V, L = 0.5\text{mH}, R_G = 25\Omega$

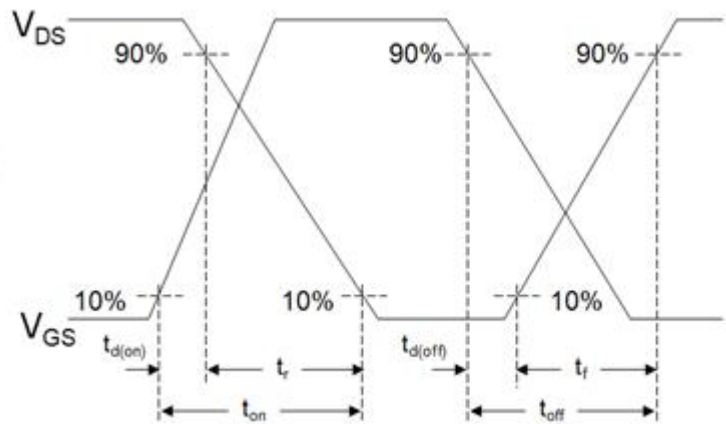
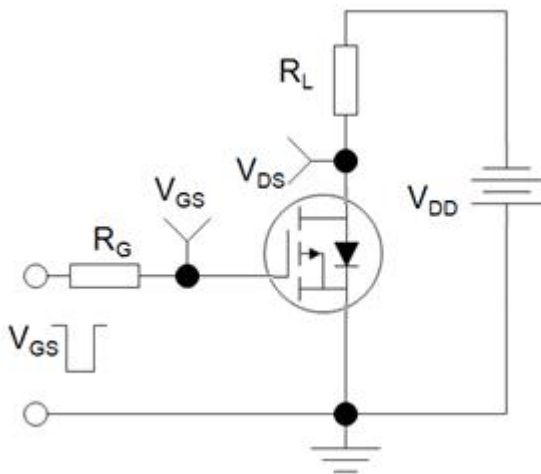
The table shows the minimum avalanche energy, which is 360mJ when the device is tested until failure

3. Identical low side and high side switch with identical R_G

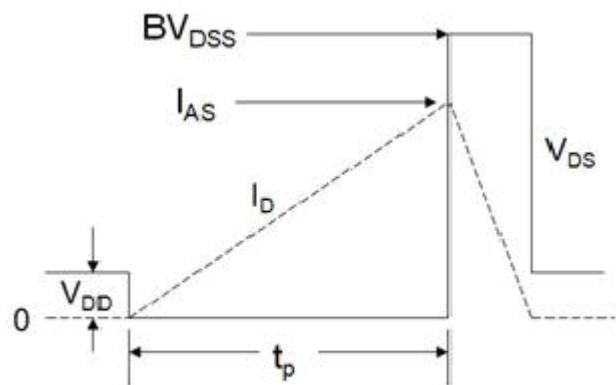
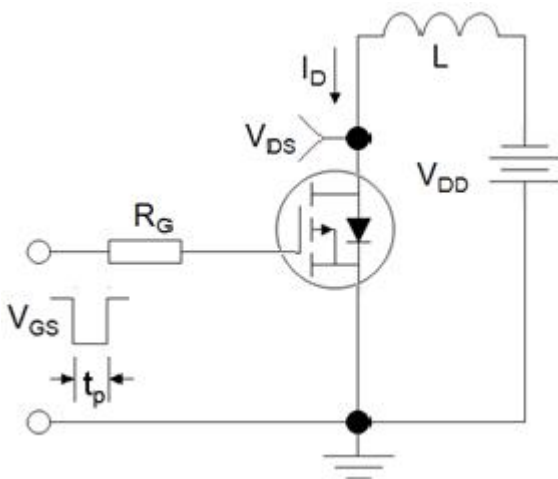
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 1. Output Characteristics

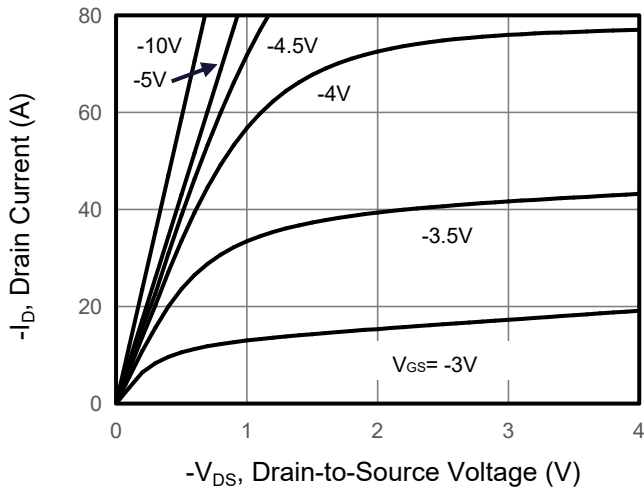


Figure 2. Transfer Characteristics

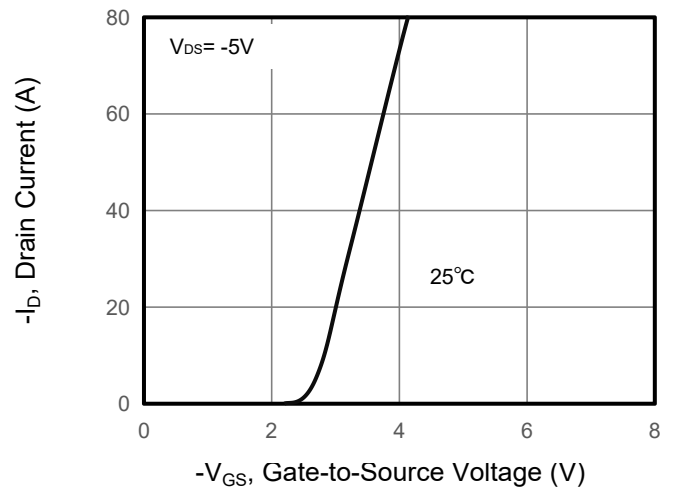


Figure 3. Drain Source On Resistance

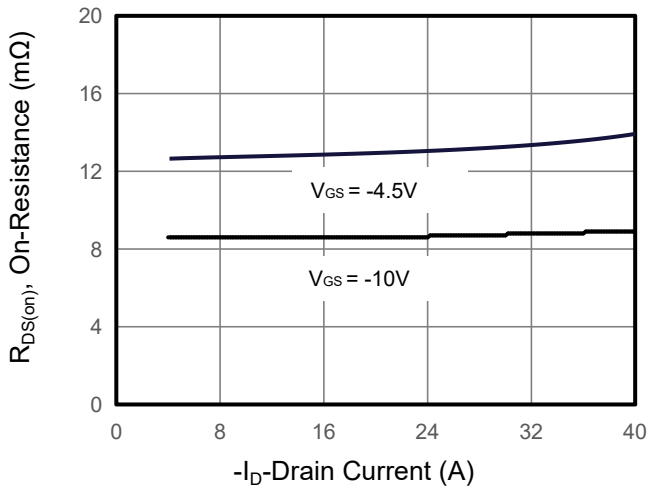


Figure 4. Gate Charge

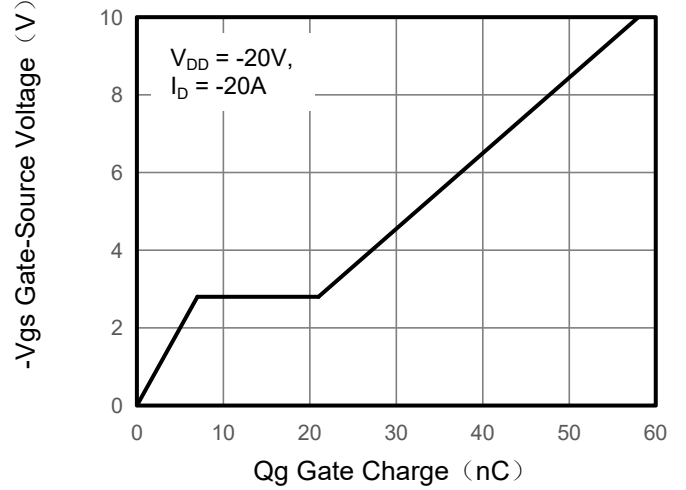


Figure 5. Capacitance

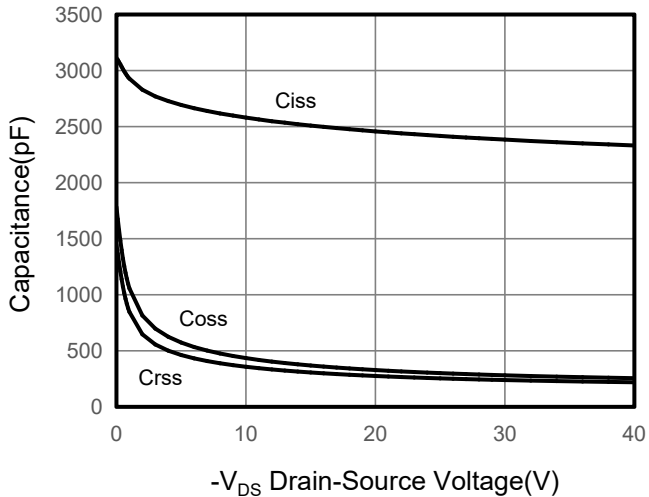
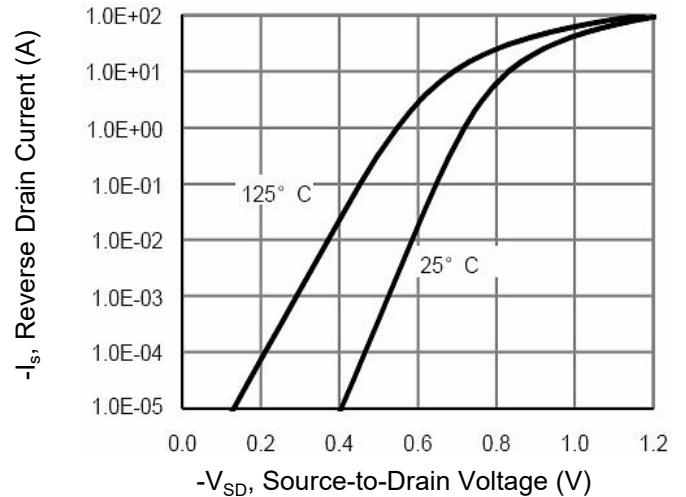


Figure 6. Source-Drain Diode Forward



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 7. Drain-Source On-Resistance

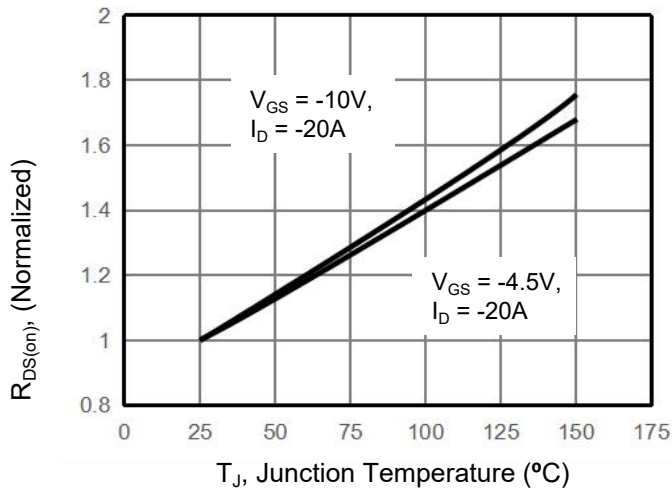


Figure 8. Safe Operation Area

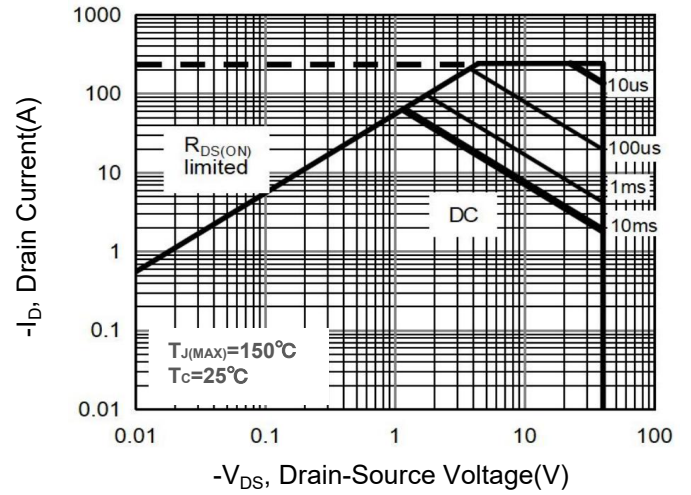


Figure 9. Maximum Continuous Drain Current vs Case Temperature

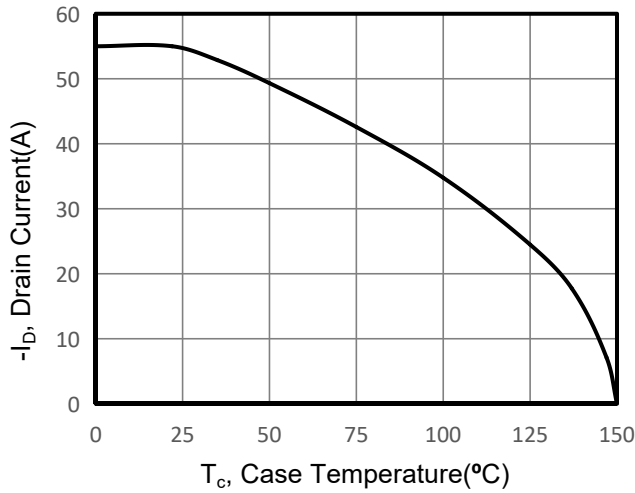
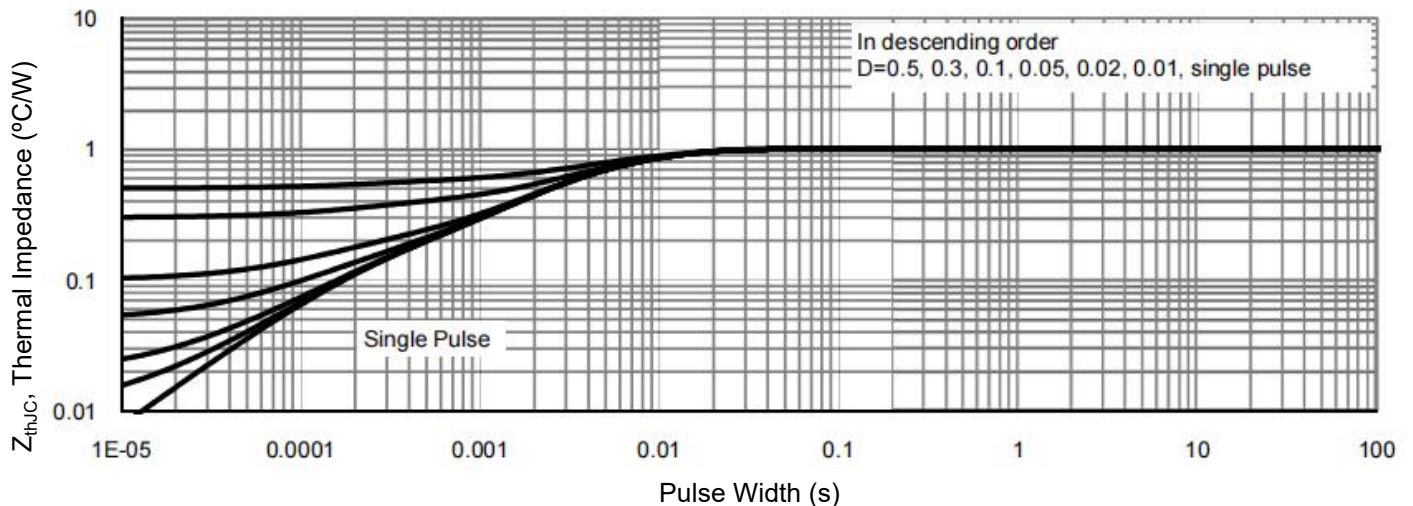
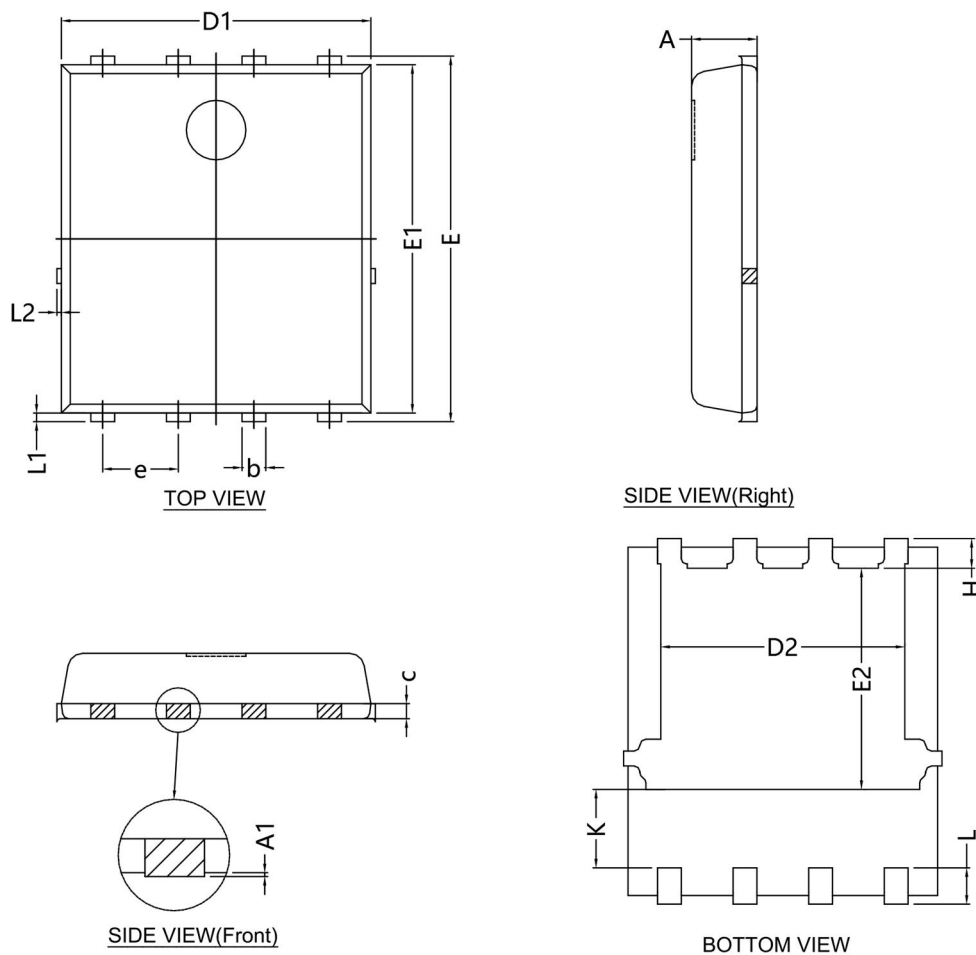


Figure 10. Normalized Maximum Transient Thermal Impedance



DFN5X6-8L Package Information



DIM. SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A	1.00	1.10	1.20
A1	0	---	0.05
b	0.30	0.40	0.50
c	0.20	0.25	0.30
D1	5.10	5.20	5.30
D2	3.90	4.10	4.25
E	6.00	6.15	6.30
E1	5.76	5.86	5.96
E2	3.52	3.72	3.92
e	1.27 BSC		
H	0.40	0.50	0.60
L	0.50	0.61	0.71
L1	0.05	0.15	0.25
L2	0.02	0.08	0.15
K	1.10	---	---