

FDMS8320LDC-VB Datasheet

N-Channel 40 V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^{a, e}	Q_g (Typ.)
40	0.0050 at $V_{GS} = 10$ V	70	67 nC
	0.0060 at $V_{GS} = 4.5$ V	65	

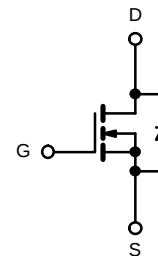
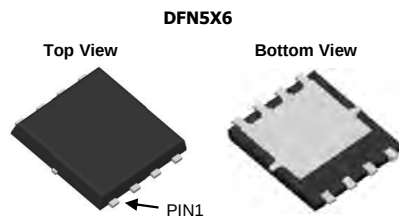
FEATURES

- Trench Power MOSFET
- 100 % R_g and UIS Tested



APPLICATIONS

- Notebook PC Core
- VRM/POL



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ($T_J = 175$ °C)	$T_C = 25$ °C	I_D	70 ^{a, e}	A
	$T_C = 70$ °C		60 ^e	
	$T_A = 25$ °C		19 ^{b, c}	
	$T_A = 70$ °C		18.6 ^{b, c}	
Pulsed Drain Current		I_{DM}	120	mJ
Avalanche Current Pulse		I_{AS}	21	
Single Pulse Avalanche Energy		E_{AS}	47.2	
Continuous Source-Drain Diode Current	$T_C = 25$ °C	I_S	70 ^{a, e}	A
	$T_A = 25$ °C		2.36 ^{b, c}	
Maximum Power Dissipation	$T_C = 25$ °C	P_D	100 ^a	W
	$T_C = 70$ °C		55	
	$T_A = 25$ °C		6.15 ^{b, c}	
	$T_A = 70$ °C		3.07 ^{b, c}	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	$t \leq 10$ s	R_{thJA}	47	56	°C/W
Maximum Junction-to-Case	Steady State	R_{thJC}	0.8	1.1	

Notes:

a. Based on $T_C = 25$ °C.

b. Surface mounted on 1" x 1" FR4 board.

c. $t = 10$ s.

d. Maximum under steady state conditions is 90 °C/W.

e. Calculated based on maximum junction temperature. Package limitation current is 80 A.

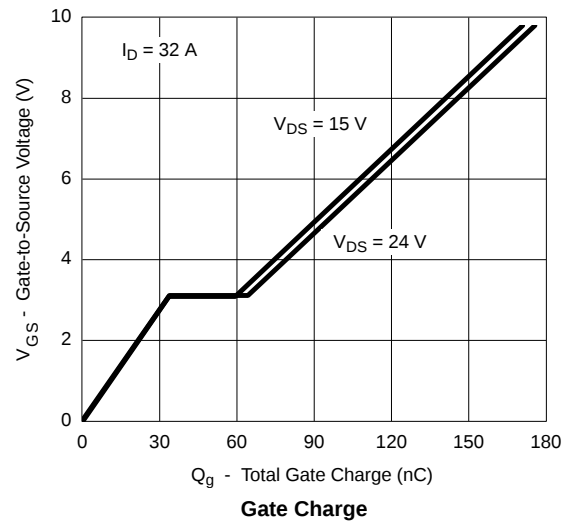
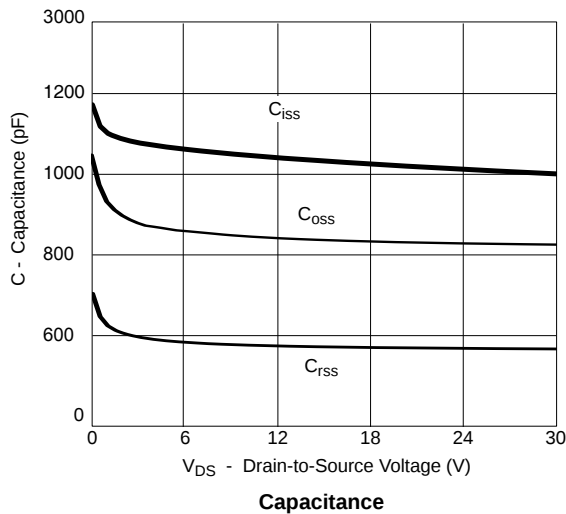
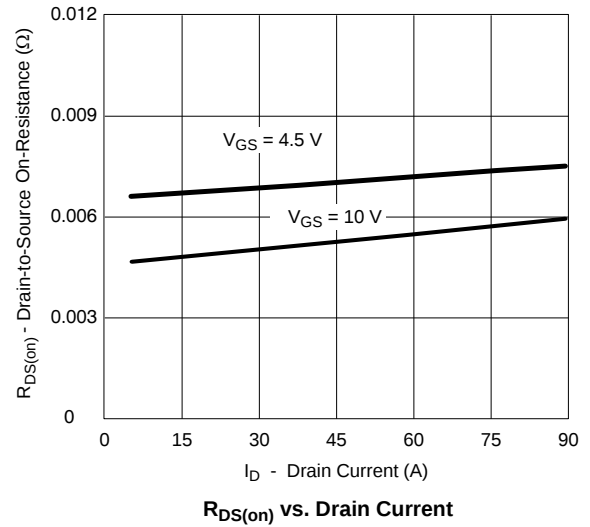
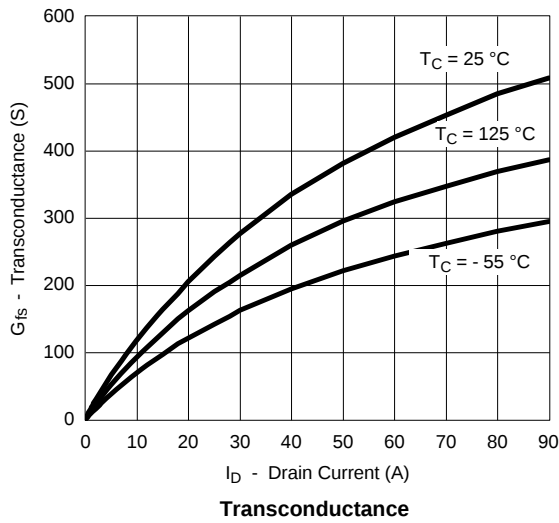
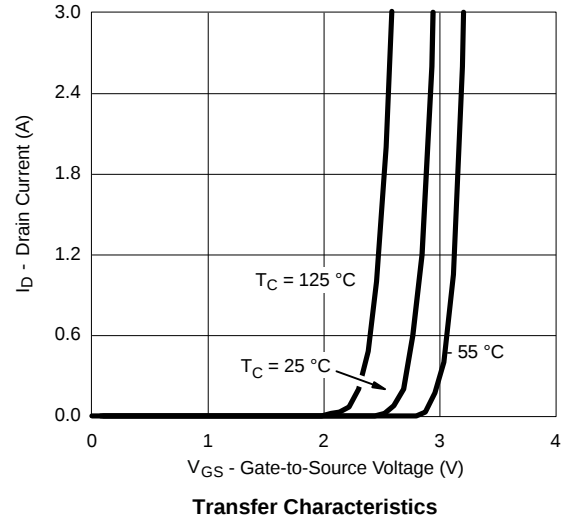
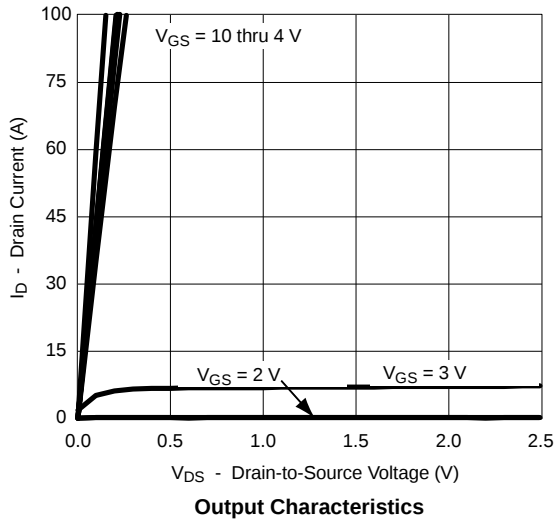
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
Parameter	Symbol	Test Conditions	Min .	Typ.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	40			V	
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		35		mV/°C	
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			- 5.5			
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.2		2.5	V	
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V			1	μA	
		V _{DS} = 40 V, V _{GS} = 0 V, T _J = 55 °C			10		
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	70			A	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 32 A		0.005		Ω	
		V _{GS} = 4.5 V, I _D = 29 A		0.006			
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 32 A		110		S	
Dynamic ^b							
Input Capacitance	C _{iss}	V _{DS} = 12.5 V, V _{GS} = 0 V, f = 1 MHz		1195		pF	
Output Capacitance	C _{oss}			975			
Reverse Transfer Capacitance	C _{rss}			670			
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 32 A		67		nC	
Gate-Source Charge	Q _{gs}	V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 29 A		57.3			
Gate-Drain Charge	Q _{gd}			31			
Gate Resistance	R _g			25			
Turn-On Delay Time	t _{d(on)}	f = 1 MHz		1.4	2.1	Ω	
Rise Time	t _r			18	27		
Turn-Off Delay Time	t _{d(off)}		V _{DD} = 15 V, R _L = 0.555 Ω I _D ≅ 27 A, V _{GEN} = 10 V, R _g = 1 Ω		11		17
Fall Time	t _f				70		105
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 0.625 Ω I _D ≅ 24 A, V _{GEN} = 4.5 V, R _g = 1 Ω			10	15	
Rise Time	t _r				55	83	
Turn-Off Delay Time	t _{d(off)}			180	270		
Fall Time	t _f			55	83		
				12	18		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			70	A	
Pulse Diode Forward Current ^a	I _{SM}				100		
Body Diode Voltage	V _{SD}	I _S = 22 A		0.8	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}	I _F = 20 A, di/dt = 100 A/μs, T _J = 25 °C		52	78	ns	
Body Diode Reverse Recovery Charge	Q _{rr}			70.2	105	nC	
Reverse Recovery Fall Time	t _a			27		ns	
Reverse Recovery Rise Time	t _b			25			

Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

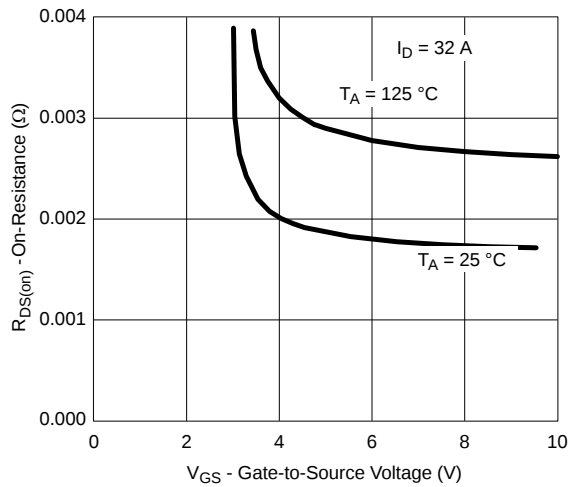
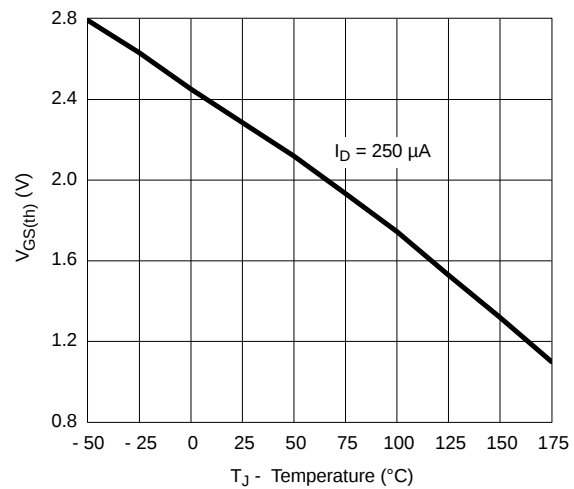
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


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On-Resistance vs. Junction Temperature

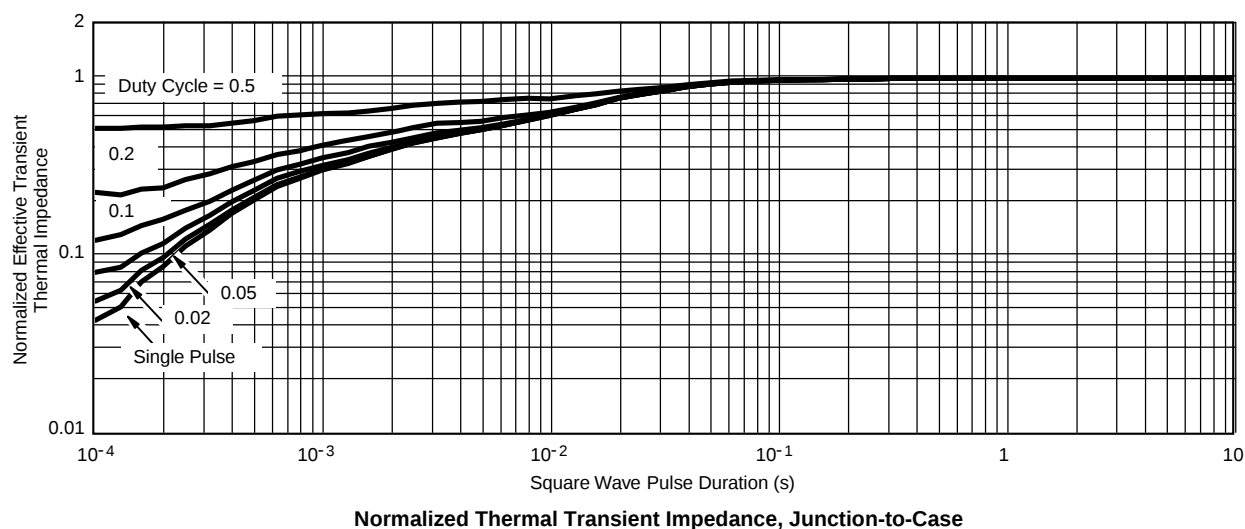
Forward Diode Voltage vs. Temperature

 $R_{DS(on)}$ vs. V_{GS} vs. Temperature

Threshold Voltage


* $V_{GS} >$ minimum V_{GS} at which $r_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


* The power dissipation P_D is based on $T_{J(max)} = 175$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



DFN5x6_8L_EP1_P PACKAGE OUTLIN



RECOMMENDED LAND PATTERN



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.85	0.95	1.00	0.033	0.037	0.039
A1	0.00	---	0.05	0.000	---	0.002
b	0.30	0.40	0.50	0.012	0.016	0.020
c	0.15	0.20	0.25	0.006	0.008	0.010
D	5.10	5.20	5.30	0.201	0.205	0.209
D1	4.25	4.35	4.45	0.167	0.171	0.175
E	5.45	5.55	5.65	0.215	0.219	0.222
E1	5.95	6.05	6.15	0.234	0.238	0.242
E2	3.525	3.625	3.725	0.139	0.143	0.147
E3	1.175	1.275	1.375	0.046	0.050	0.054
e	1.27 BSC			0.050 BSC		
L	0.45	0.55	0.65	0.018	0.022	0.026
L1	0	---	0.15	0	---	0.006
L2	0.68 REF			0.027 REF		
θ	0°	---	10°	0°	---	10°

NOTE

UNIT: mm

- PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MILS EACH.
- CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

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