

## Precision 24 MHz CMOS Rail-to-Rail Input/Output Operational Amplifiers

### Features

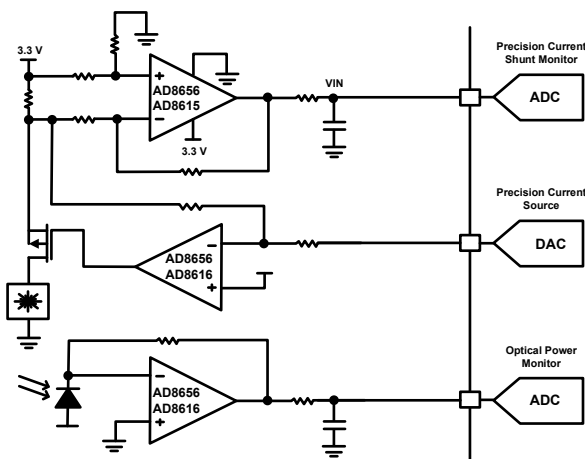
- Continuous Time Amplifier, No Chopper or Auto-zero Glitch
- Low Offset Voltage: 50  $\mu\text{V}$  max
- Low Offset Voltage Drift: 0.2  $\mu\text{V}/^\circ\text{C}$   
1  $\mu\text{V}/^\circ\text{C}$  max
- Low Input Bias Current: 0.6 pA  
3 pA max
- Low Noise: 6  $\text{nV}/\sqrt{\text{Hz}}$  @1 kHz  
4  $\text{nV}/\sqrt{\text{Hz}}$  @10 kHz  
0.1 Hz to 10 Hz 1.4  $\mu\text{V}_{\text{P-P}}$
- High Unit Gain Bandwidth: 24 MHz
- High Slew Rate: 6.8  $\text{V}/\mu\text{s}$
- Fast Settling Time: 0.5  $\mu\text{s}$  to 0.01%
- Supply Current: 1.8 mA per amplifier
- Wide Supply Voltage: 2.7 V to 5.5 V;  $\pm 1.35$  V to  $\pm 2.75$  V
- Rail-to-rail Input and Output
- Drive Large Capacitive Load Up to 10 nF
- Large Output Current:  $\pm 150$  mA
- Wide Temperature Range:  $-40$   $^\circ\text{C}$  to  $+125$   $^\circ\text{C}$

### Applications

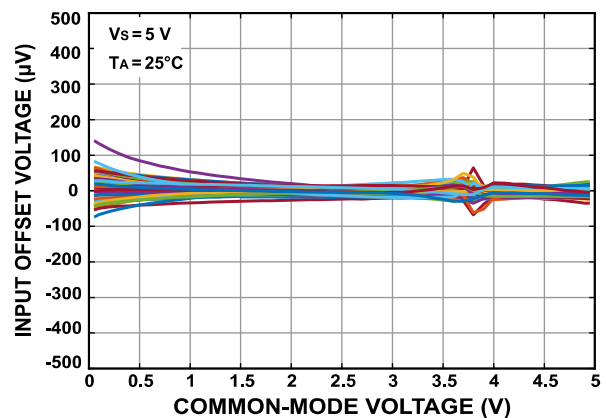
- Multi-parameter Patient Monitor
- Chemistry and Gas Analyzer
- Multi-pole Filters
- Sensor Analog Front End
- ASIC Input or Output Amplifiers
- ADC Input Driver and DAC Output Buffer
- Photodiode Trans-impedance Amplifier

Model	Channels	Package
AD8616	1	SOT23-5
AD8656	1	SOT23-5
	2	SOIC-8/MSOP-8
	4	SOIC-14/TSSOP-14

### Typical Application



### Typical Characteristics



## Pin Configurations and Function

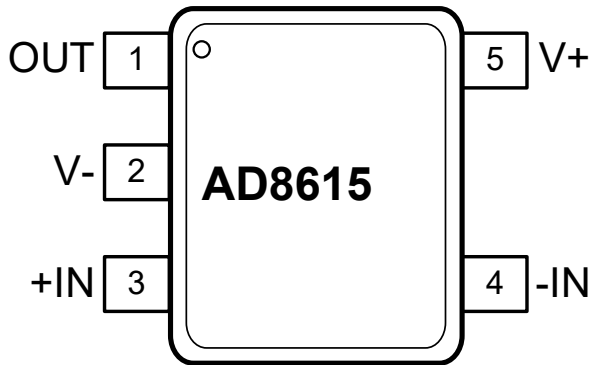


Figure 1. AD8615 Pin Configuration (5-lead SOT23)

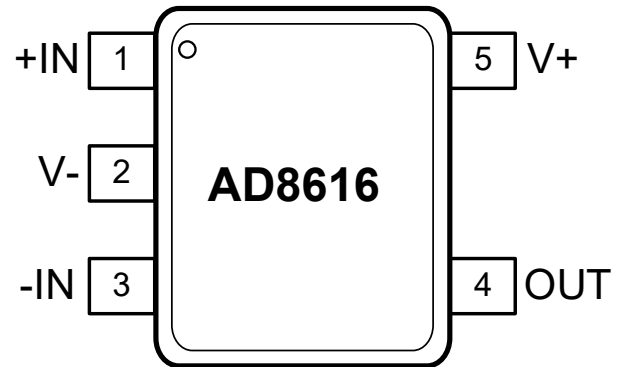


Figure 2. AD8616 Pin Configuration (5-lead SOT23)

Mnemonic	Pin No.	I/O	Description
OUT	1	AO	Amplifier output
V-	2	P	Negative power supply
+IN	3	AI	Amplifier non-inverting input
-IN	4	AI	Amplifier inverting input
V+	5	P	Positive power supply

Mnemonic	Pin No.	I/O	Description
+IN	1	AI	Amplifier non-inverting input
V-	2	P	Negative power supply
-IN	3	AI	Amplifier inverting input
OUT	4	AO	Amplifier output
V+	5	P	Positive power supply

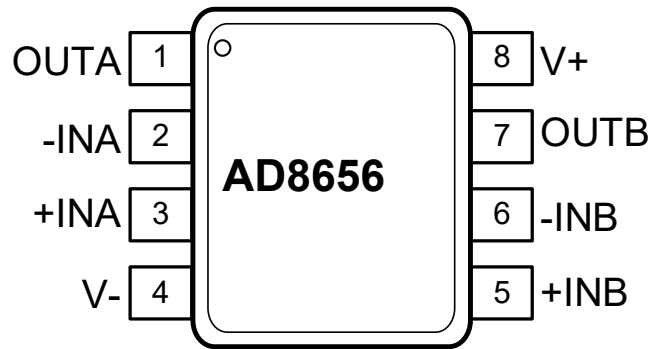


Figure 3. AD8656 Pin Configuration (8-lead SOIC and MSOP)

Mnemonic	Pin No.	I/O <sup>1</sup>	Description
OUTA	1	AO	Channel A output
-INA	2	AI	Channel A inverting input
+INA	3	AI	Channel A Non-inverting input
V-	4	P	Negative power supply
+INB	5	AI	Channel B Non-inverting input
-INB	6	AI	Channel B inverting input
OUTB	7	AO	Channel B output
V+	8	P	Positive power supply

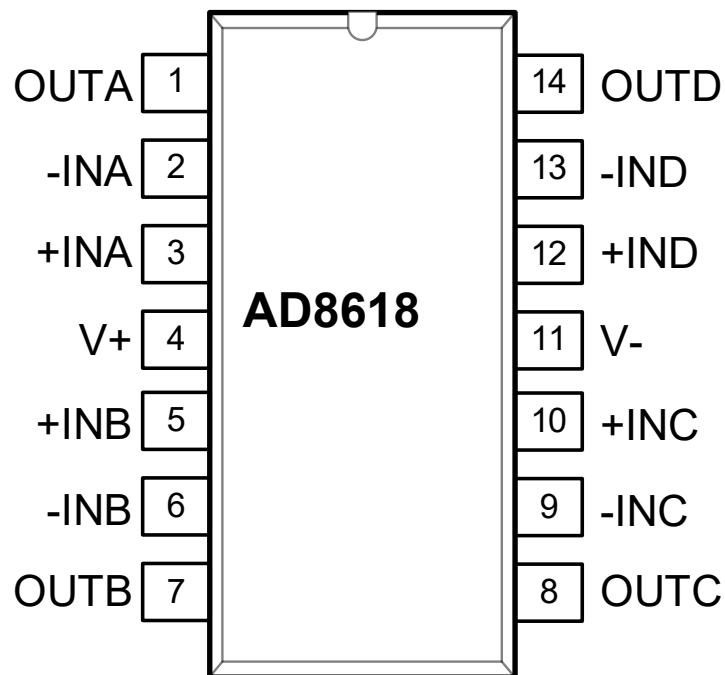


Figure 4. AD8616 Pin Configuration (14-lead SOIC and TSSOP)

Mnemonic	Pin No.	I/O <sup>1</sup>	Description
OUTA	1	AO	Channel A output
-INA	2	AI	Channel A inverting input
+INA	3	AI	Channel A non-inverting input
V+	4	P-	Positive power supply
+INB	5	AI	Channel B non-inverting input
-INB	6	AI	Channel B inverting input
OUTB	7	AO	Channel B output
OUTC	8	AO	Channel C output
-INC	9	AI	Channel C inverting input
+INC	10	AI	Channel C non-inverting input
V-	11	P	Negative power supply
+IND	12	AI	Channel D non-inverting input
-IND	13	AI	Channel D inverting input
OUTD	14	AO	Channel D output

## Absolute Maximum Ratings

Parameter	Rating
Supply Voltage	6 V
Input Voltage	V- to V+
Output Short-Circuit Duration to GND	Indefinite
Operating Temperature Range	-40 °C to 125 °C
Storage Temperature Range	-65 °C to 150 °C
Junction Temperature Range	-65 °C to 150 °C
Lead Temperature, Soldering (10 sec)	300 °C
ESD Rating (ESD)	
Human Body Model (HBM)	6 kV
Charge Device Model (CDM)	2 kV

## Thermal Resistance

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
5-lead SOT23	230	76	°C/W
8-lead SOIC	158	43	°C/W
8-lead MSOP	190	44	°C/W
14-lead SOIC	120	36	°C/W
14-lead TSSOP	240	43	°C/W

## Specifications

The ● denotes the specification which apply over the full operating temperature range, otherwise specifications are at  $V_S = 5\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $T_A = 25\text{ °C}$ , unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$V_{CM} = 2.5\text{ V}$ and $4.5\text{ V}$	●	10 70	50 150	$\mu\text{V}$ $\mu\text{V}$
		$V_{CM} = 0\text{ V}$ to $5\text{ V}$	●		500	$\mu\text{V}$
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40\text{ °C} < T_A < +125\text{ °C}$	●	0.2	1	$\mu\text{V}/\text{°C}$
Input Bias Current	$I_B$		●	0.6	3 1000	$\text{pA}$ $\text{pA}$
		$-40\text{ °C} < T_A < +85\text{ °C}$			80	$\text{pA}$
Input Offset Current	$I_{OS}$		●		5 400	$\text{pA}$ $\text{pA}$
		$-40\text{ °C} < T_A < +85\text{ °C}$			20	$\text{pA}$
Input Capacitance	$C_{DIFF}$	Differential		3.2		$\text{pF}$
	$C_{CM}$	Common-Mode		7.4		$\text{pF}$
Input Voltage Range	IVR		0		5	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V}$ to $4.5\text{ V}$	80	105		dB
Large Signal Voltage Gain	$A_{VO}$	$R_L = 2\text{ k}\Omega$ , $V_O = 0.5\text{ V}$ to $4.5\text{ V}$	110	140		dB
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$I_L = 1\text{ mA}$	●	4.98 4.97	4.988	V V
		$I_L = 10\text{ mA}$	●	4.85 4.80	4.895	V V
Output Voltage Low	$V_{OL}$	$I_L = 1\text{ mA}$	●		12 30	$\text{mV}$ $\text{mV}$
		$I_L = 10\text{ mA}$	●		105 200	$\text{mV}$ $\text{mV}$
Output Current	$I_{OUT}$			$\pm 150$		mA
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 1\text{ MHz}$ , $A_V = 1$		5.6		$\Omega$
<b>POWER SUPPLY</b>						
Supply Current Per Amplifier	$I_S$	$I_{OUT} = 0\text{ mA}$	●	1.8	2 2.1	mA mA
Power Supply Rejection Ratio	PSRR	$V_S = 2.7\text{ V}$ to $5.5\text{ V}$		80	103	dB
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$			6.8	$\text{V}/\mu\text{s}$
Unit Gain Bandwidth	UGB				24	MHz
Settling Time		To 0.01%			0.5	$\mu\text{s}$
THD + Noise	THD + N				0.0004	%
Phase Margin	$\phi_M$				49	Degree
Channel Separation	$C_S$	$f = 10\text{ kHz}$			-115	dB
		$f = 100\text{ kHz}$			-110	dB
<b>NOISE PERFORMANCE</b>						
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$			6	$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$			4.2	$\text{nV}/\sqrt{\text{Hz}}$
Peak-to-Peak Voltage Noise	$e_{n\text{-P-P}}$	0.1 Hz to 10 Hz			1.4	$\mu\text{V}_{\text{P-P}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$			0.4	$\text{fA}/\sqrt{\text{Hz}}$

The ● denotes the specification which apply over the full operating temperature range, otherwise specifications are at  $V_S = 2.7\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $T_A = 25\text{ °C}$ , unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$V_S = 3.5\text{ V}$ , $V_{CM} = 1.75\text{ V}$ and $3.0\text{ V}$		40	160	$\mu\text{V}$
		$V_S = 2.7\text{ V}$ , $V_{CM} = 0\text{ V}$ to $2.7\text{ V}$	●		500	$\mu\text{V}$
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40\text{ °C} < T_A < +125\text{ °C}$	●	0.2	1	$\mu\text{V}/\text{°C}$
Input Bias Current	$I_B$		●	0.6	3	$\text{pA}$
		$-40\text{ °C} < T_A < +85\text{ °C}$			1000	$\text{pA}$
Input Offset Current	$I_{OS}$		●		5	$\text{pA}$
		$-40\text{ °C} < T_A < +85\text{ °C}$			400	$\text{pA}$
Input Capacitance	$C_{DIFF}$	Differential		3.2		$\text{pF}$
	$C_{CM}$	Common-Mode		7.4		$\text{pF}$
Input Voltage Range	IVR		0		2.7	$\text{V}$
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V}$ to $2.2\text{ V}$	70	95		$\text{dB}$
Large Signal Voltage Gain	$A_{VO}$	$R_L = 2\text{ k}\Omega$ , $V_O = 0.5\text{ V}$ to $2.2\text{ V}$	100	135		$\text{dB}$
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$I_L = 1\text{ mA}$	●	2.65	2.683	$\text{V}$
				2.65		$\text{V}$
Output Voltage Low	$V_{OL}$	$I_L = 1\text{ mA}$	●		17	$\text{mV}$
					50	$\text{mV}$
Output Current	$I_{OUT}$			$\pm 50$		$\text{mA}$
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 1\text{ MHz}$ , $A_V = 1$		5.6		$\Omega$
<b>POWER SUPPLY</b>						
Supply Current Per Amplifier	$I_S$	$I_{OUT} = 0\text{ mA}$	●	1.8	2	$\text{mA}$
Power Supply Rejection Ratio	PSRR	$V_S = 2.7\text{ V}$ to $5.5\text{ V}$		80	103	$\text{dB}$
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$		6.8		$\text{V}/\mu\text{s}$
Unit Gain Bandwidth	UGB			24		$\text{MHz}$
Settling Time		To 0.01%		0.5		$\mu\text{s}$
THD + Noise	THD + N			0.0004		%
Phase Margin	$\phi_M$			43		Degree
Channel Separation	$C_S$	$f = 10\text{ kHz}$		-115		$\text{dB}$
		$f = 100\text{ kHz}$		-110		$\text{dB}$
<b>NOISE PERFORMANCE</b>						
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		6		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$		4.2		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		0.4		$\text{fA}/\sqrt{\text{Hz}}$
Peak-to-Peak Voltage Noise	$e_{n\text{P-P}}$	0.1 Hz to 10 Hz		1.4		$\mu\text{V}_{\text{P-P}}$

## Typical Performance Characteristics

Unless otherwise stated,  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_L = 2\text{ k}\Omega$ .

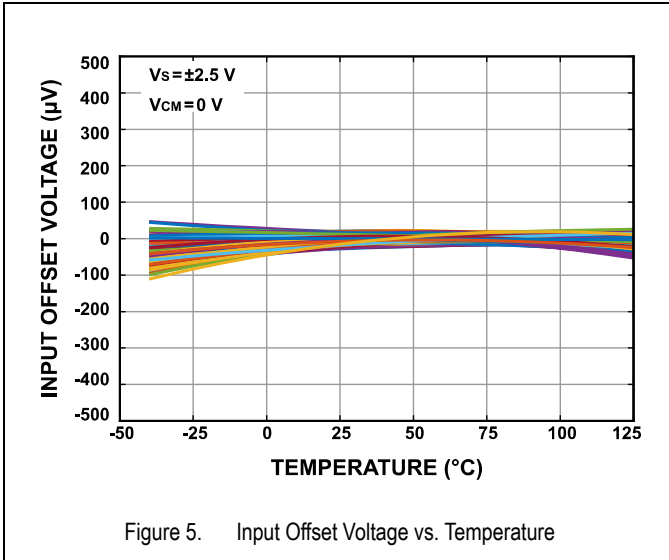


Figure 5. Input Offset Voltage vs. Temperature

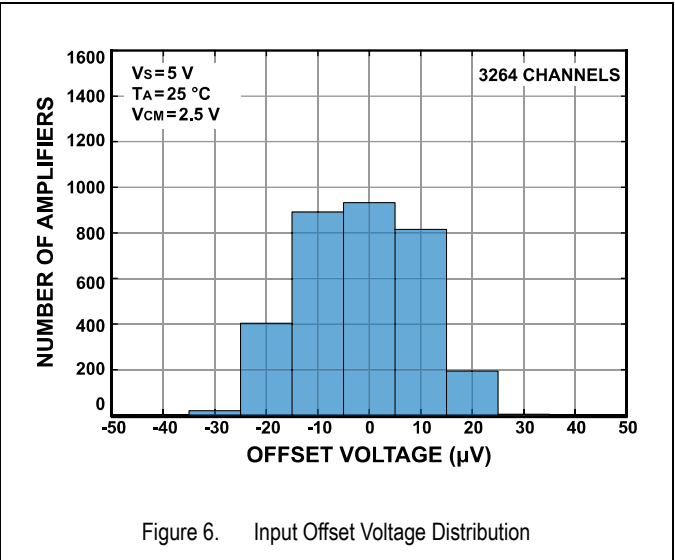


Figure 6. Input Offset Voltage Distribution

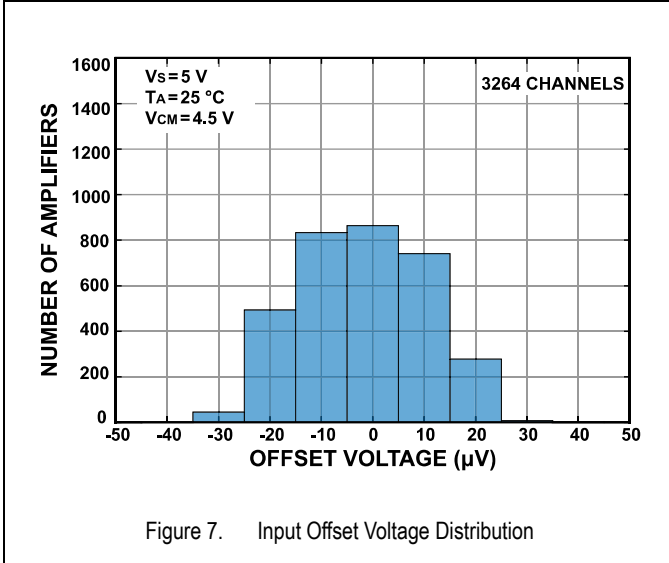


Figure 7. Input Offset Voltage Distribution

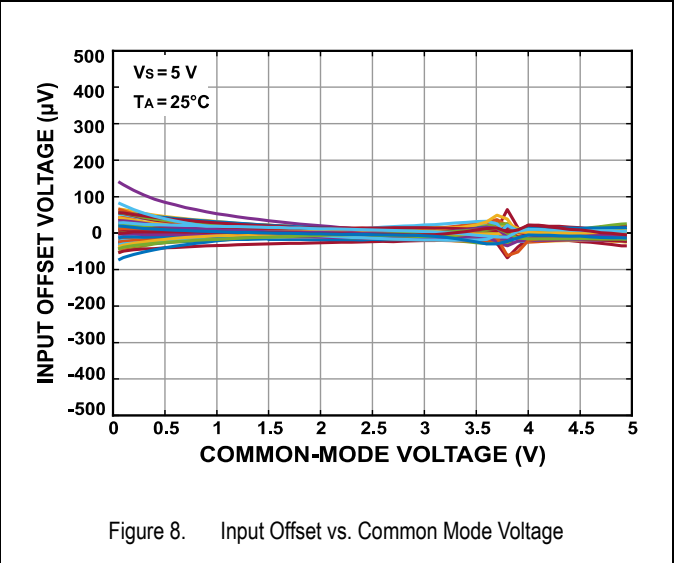


Figure 8. Input Offset vs. Common Mode Voltage

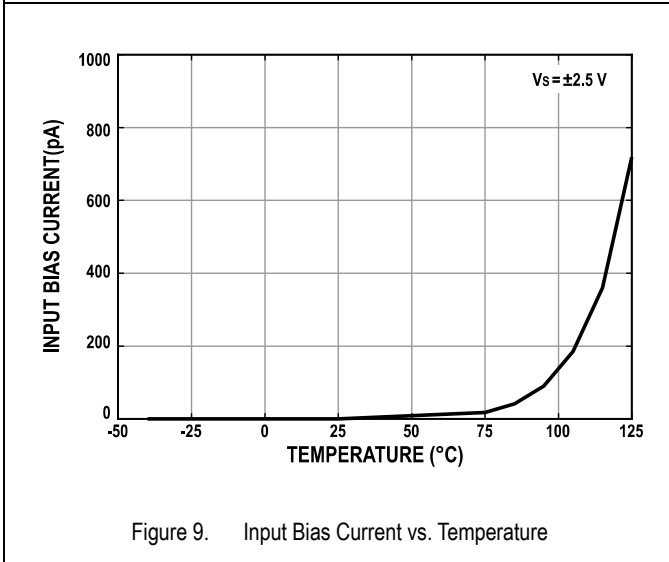


Figure 9. Input Bias Current vs. Temperature

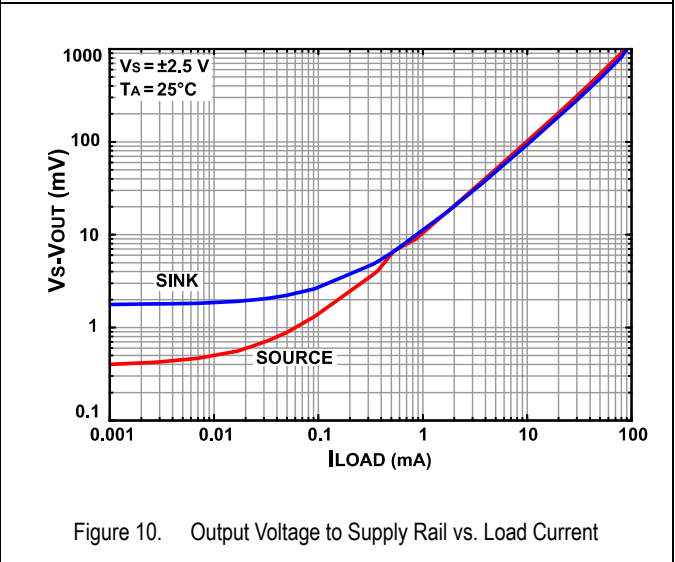
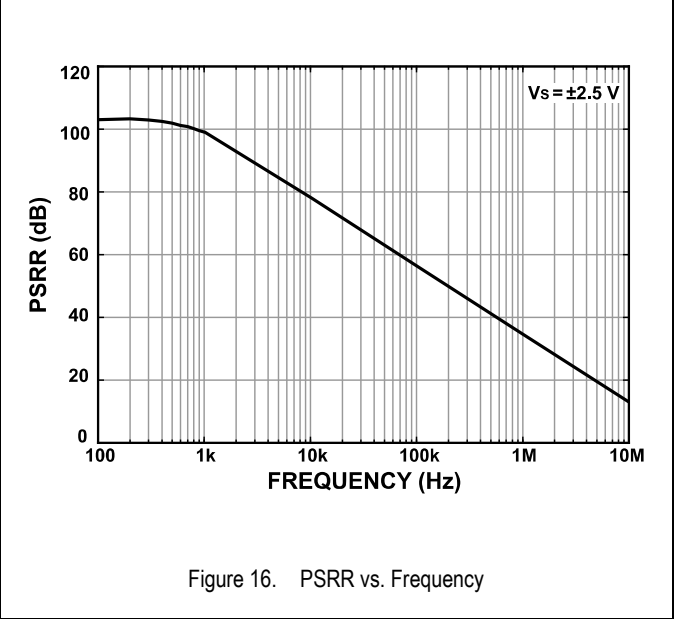
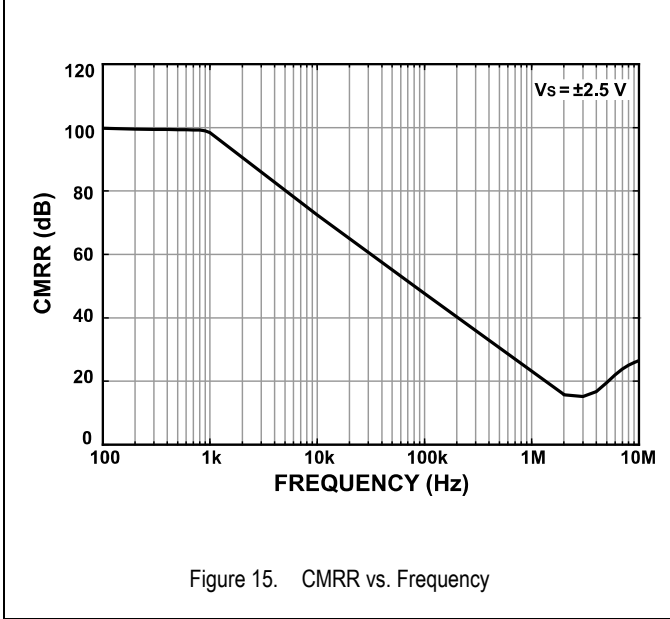
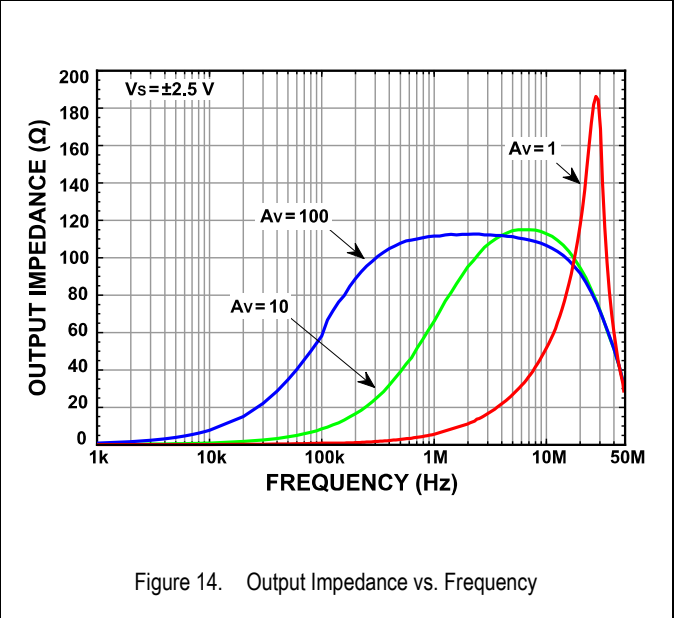
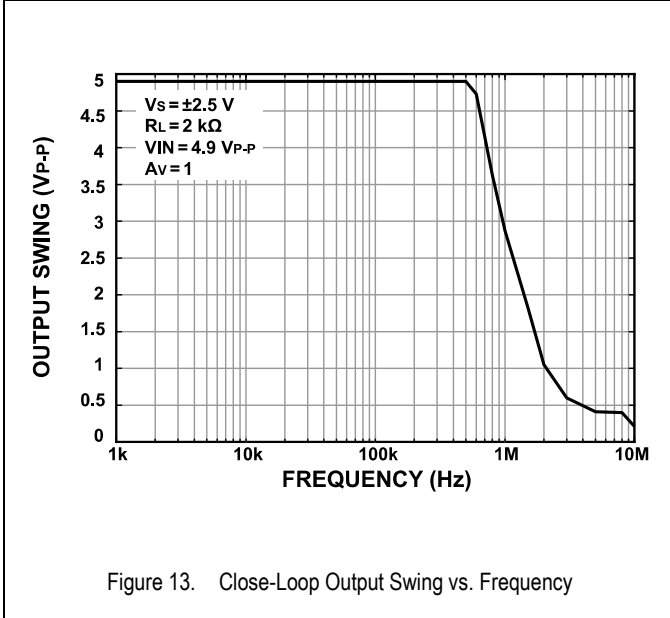
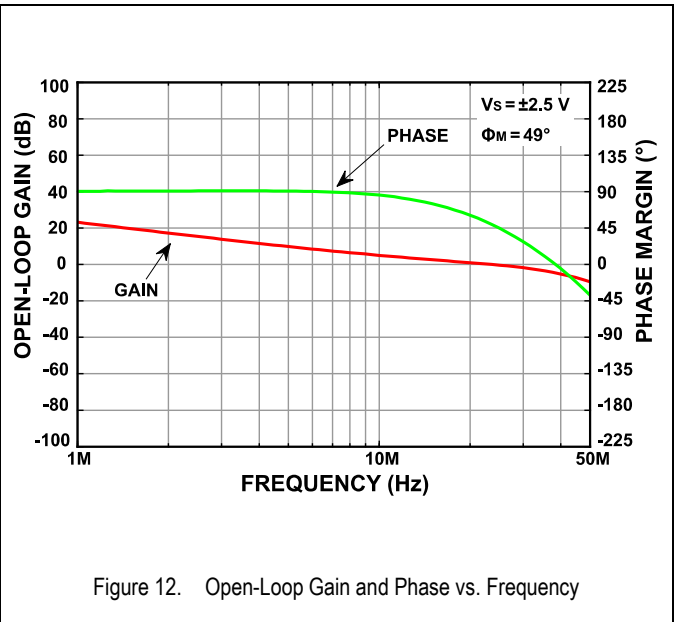
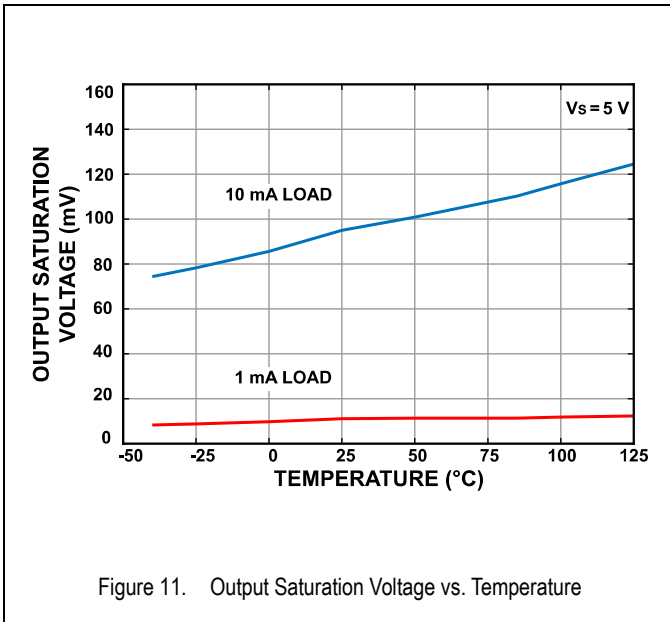
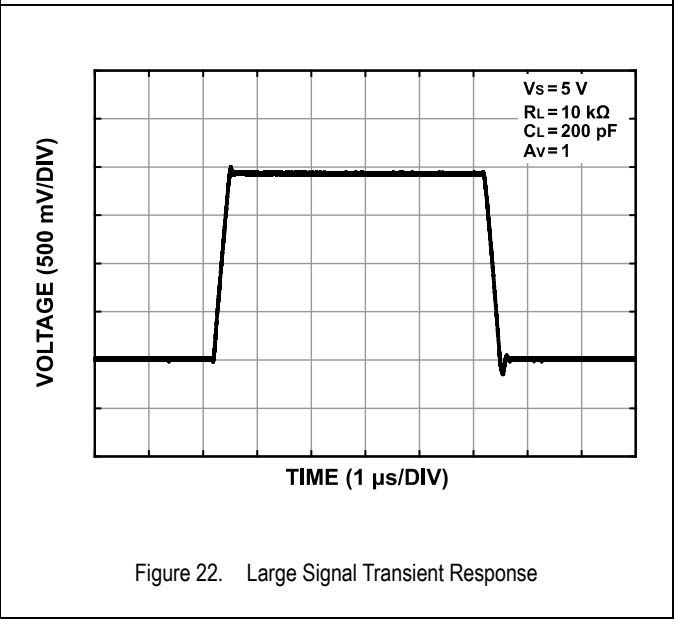
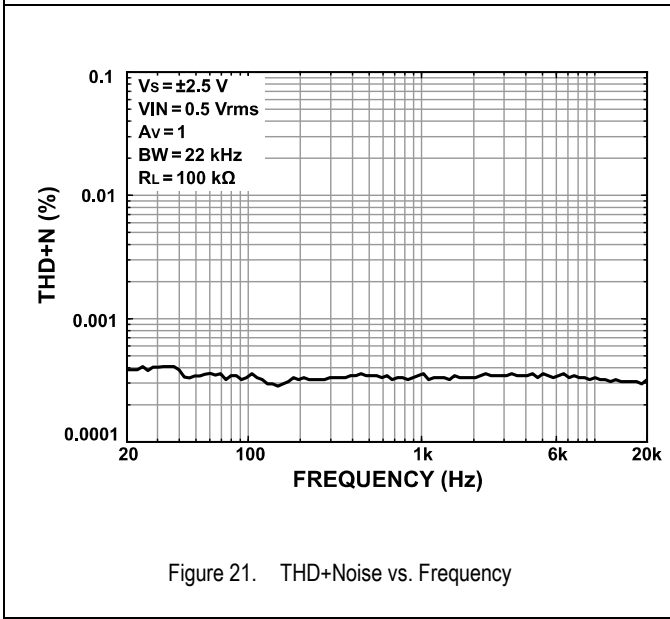
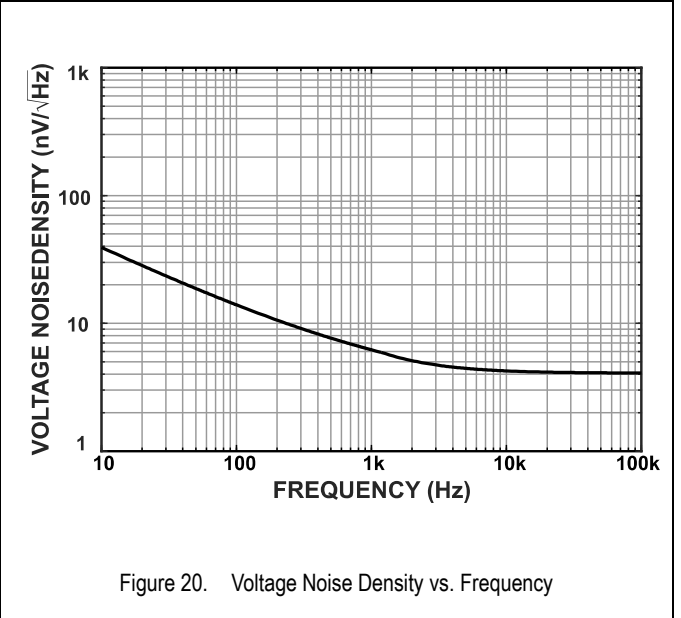
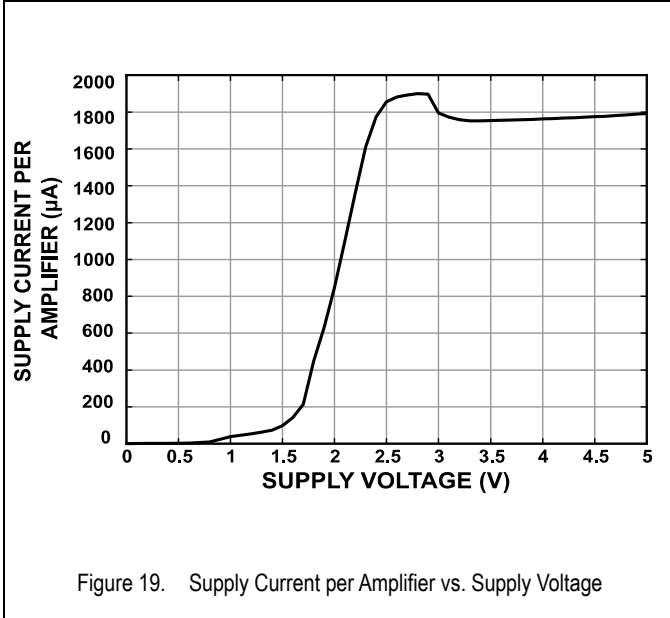
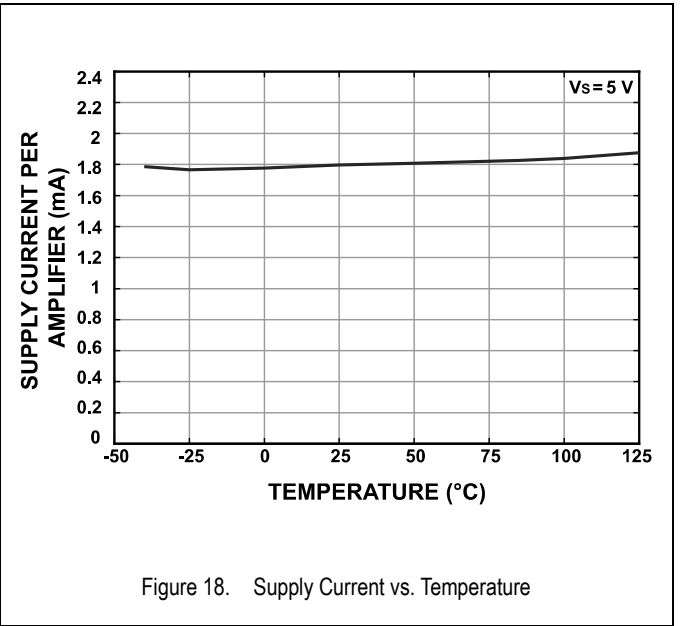
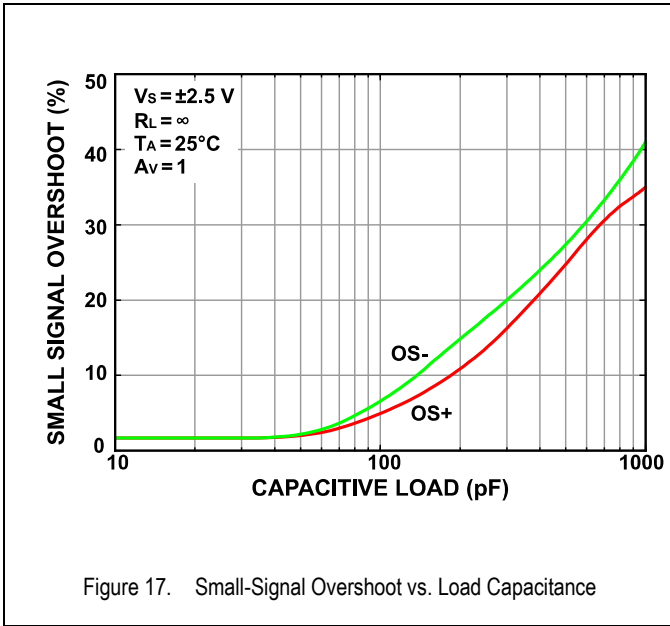
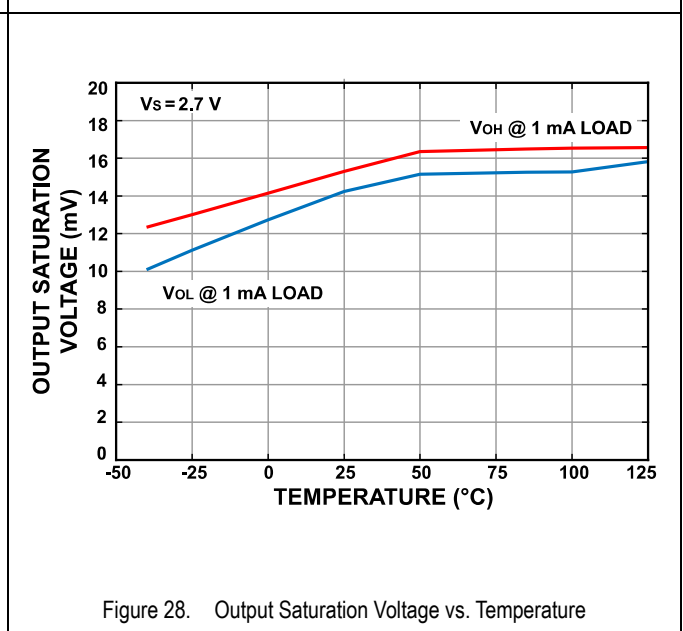
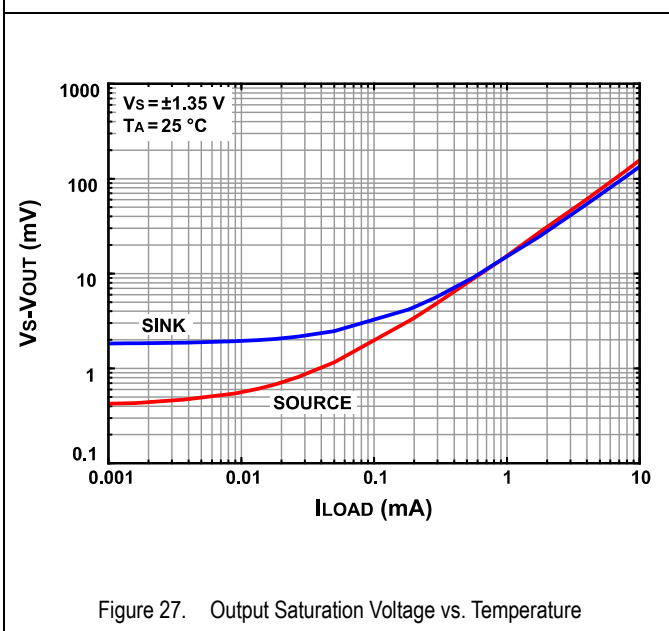
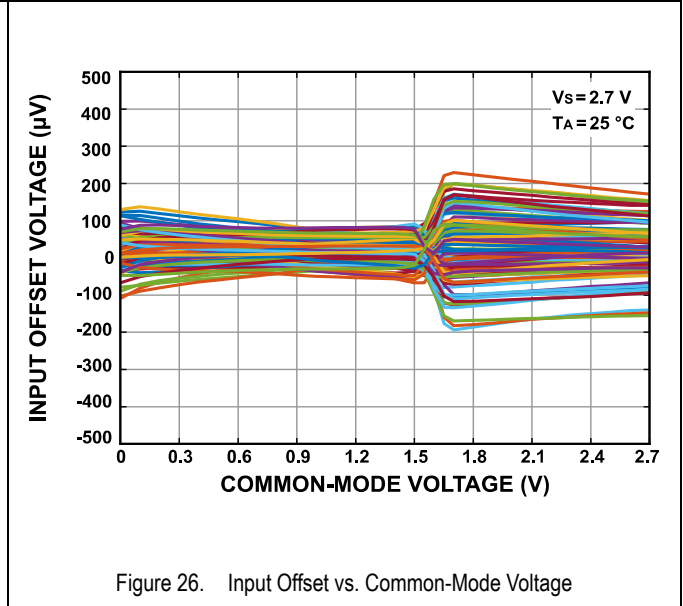
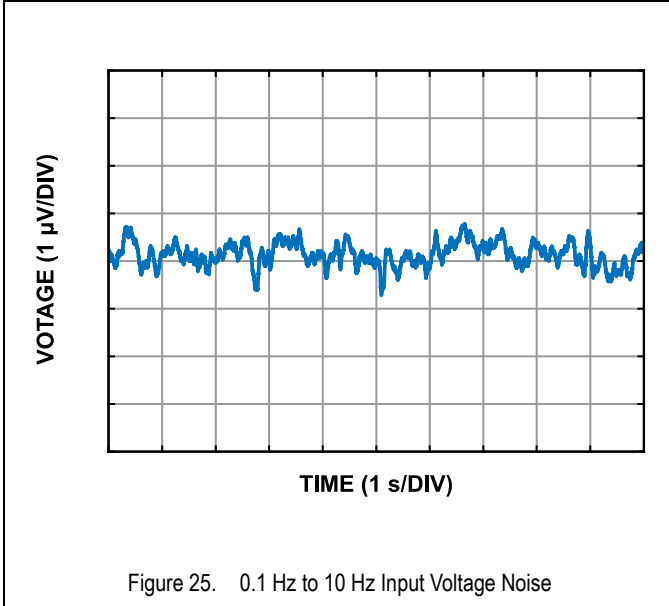
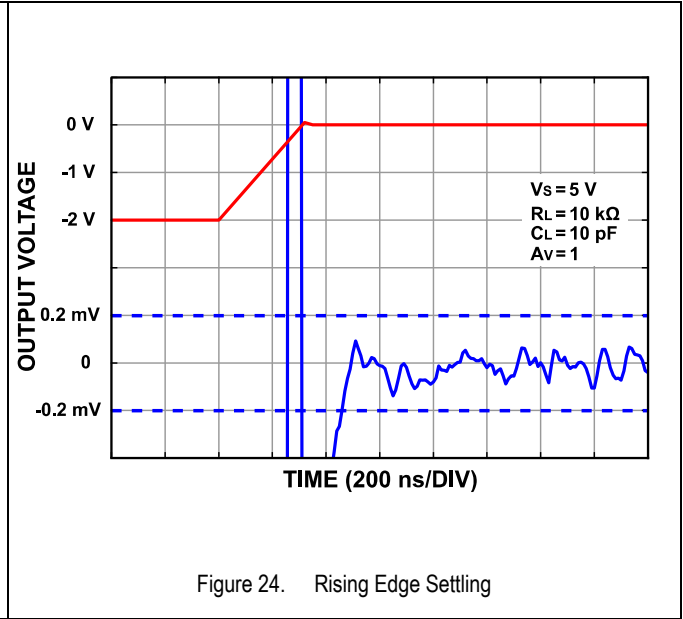
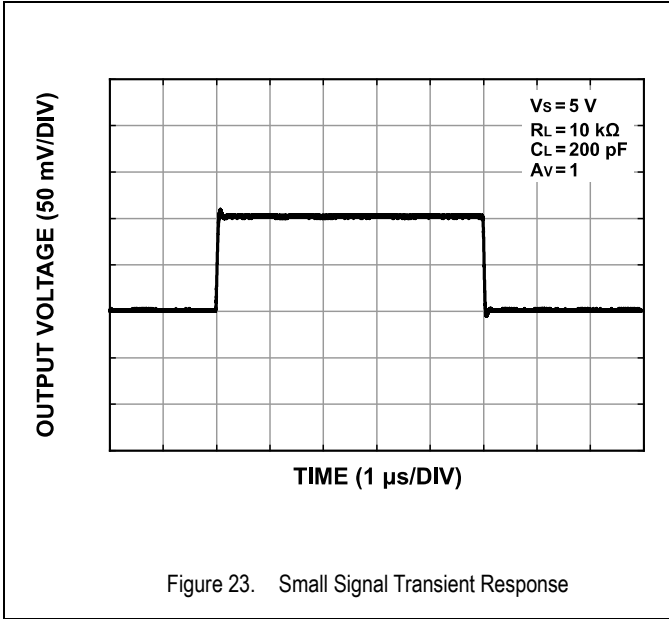
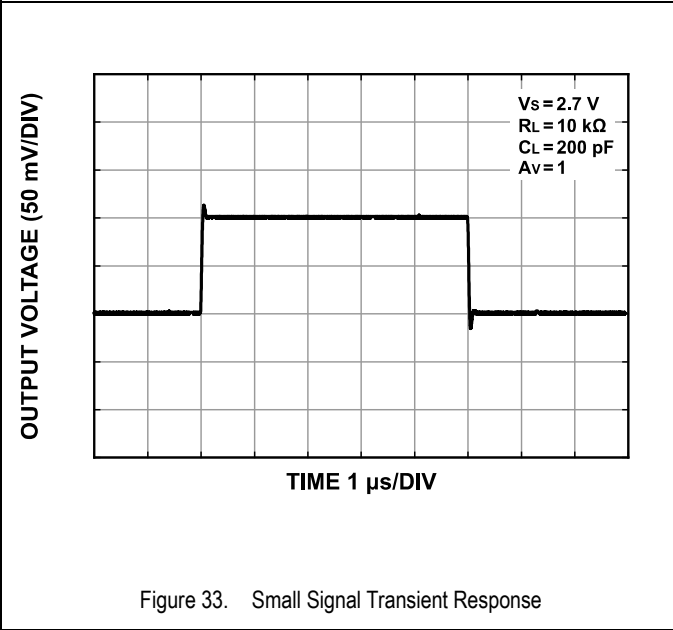
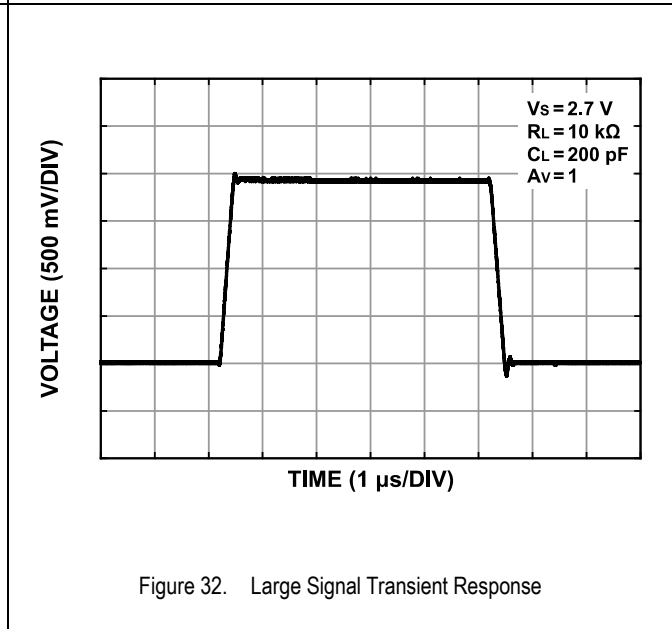
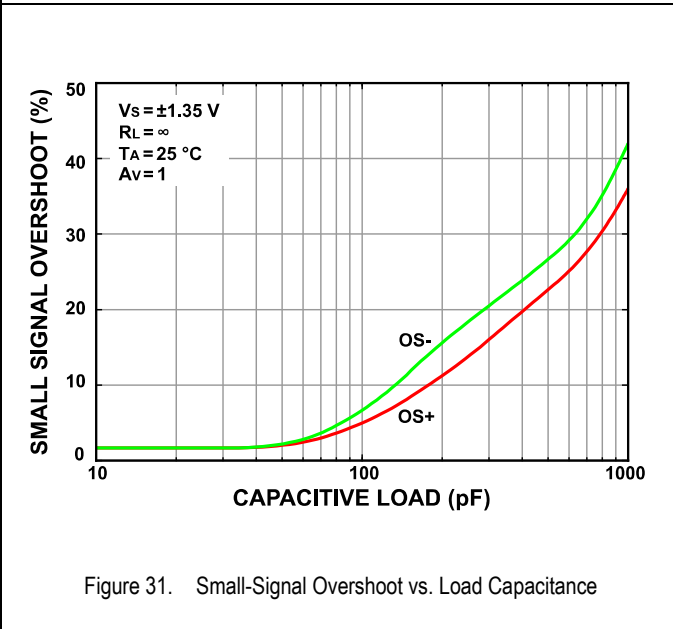
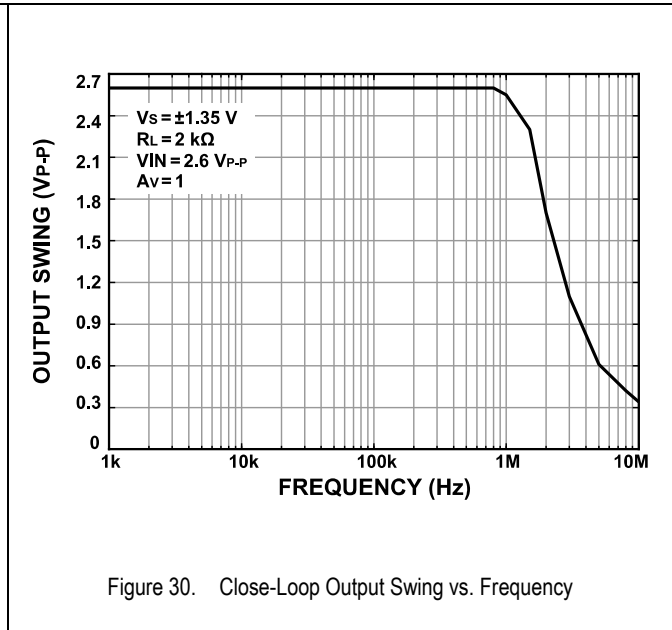
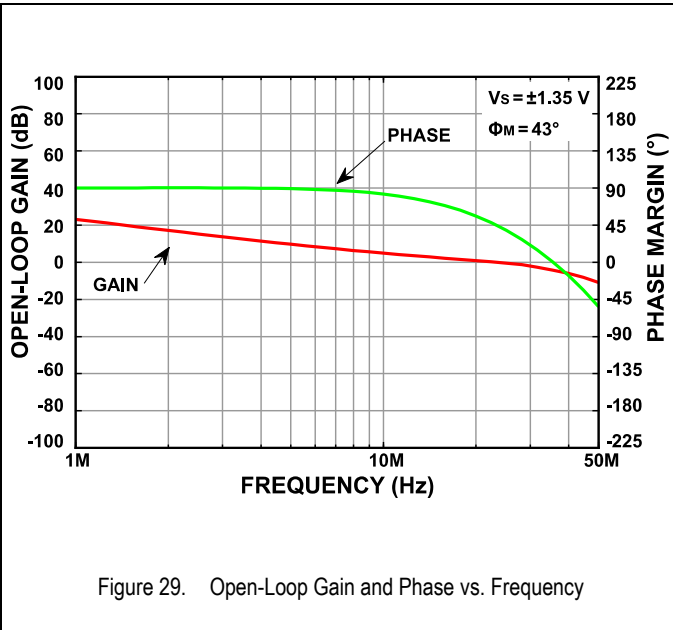


Figure 10. Output Voltage to Supply Rail vs. Load Current









## General Application Information

### Output Phase Reversal

Phase reversal is a change of polarity in the transfer function of the amplifier. This can occur when the voltage applied at the input of an amplifier exceeds the maximum common-mode voltage. Phase reversal can cause permanent damage to the device and may result in system lockups. The AD8615, AD8656, AD8618 and AD8616 do not exhibit phase reversal when input voltages are beyond the supplies.

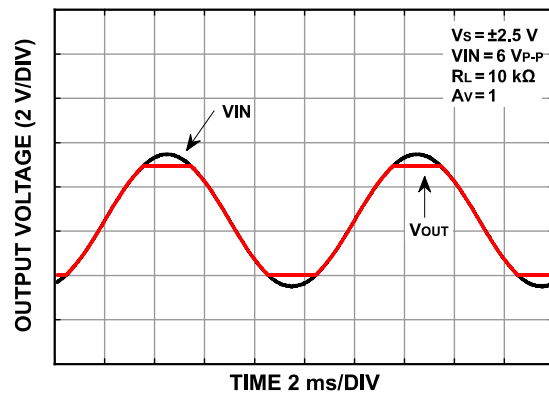


Figure 34. No Phase Reversal

### THD+Noise

AD86XX features low total harmonic distortion (THD) and excellent gain linearity, making these amplifiers a great choice for precision circuits with high closed-loop gain and for audio application circuits. Figure 35 demonstrates that when configured with positive unity gain (the worst case) and driving a 100 kΩ load, the total distortion and noise of AD86XX is approximately 0.0004%.

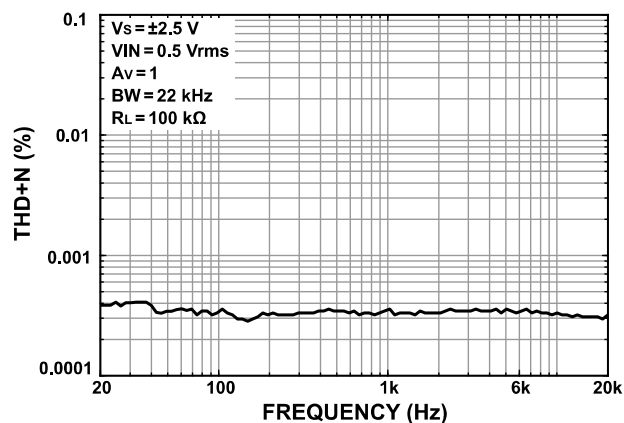


Figure 35. THD+N vs. Frequency

### Total Noise Including Source Resistors

The low input current noise and input bias current of the AD86XX make it the ideal amplifier for circuits with substantial input source resistance. Input offset voltage increases by less than 15 nV per 500 Ω of source resistance at room temperature. The total noise density of the circuit is

$$e_{nTOTAL} = \sqrt{e_n^2 + (i_n R_s)^2 + 4kTR_s}$$

## Outline Information

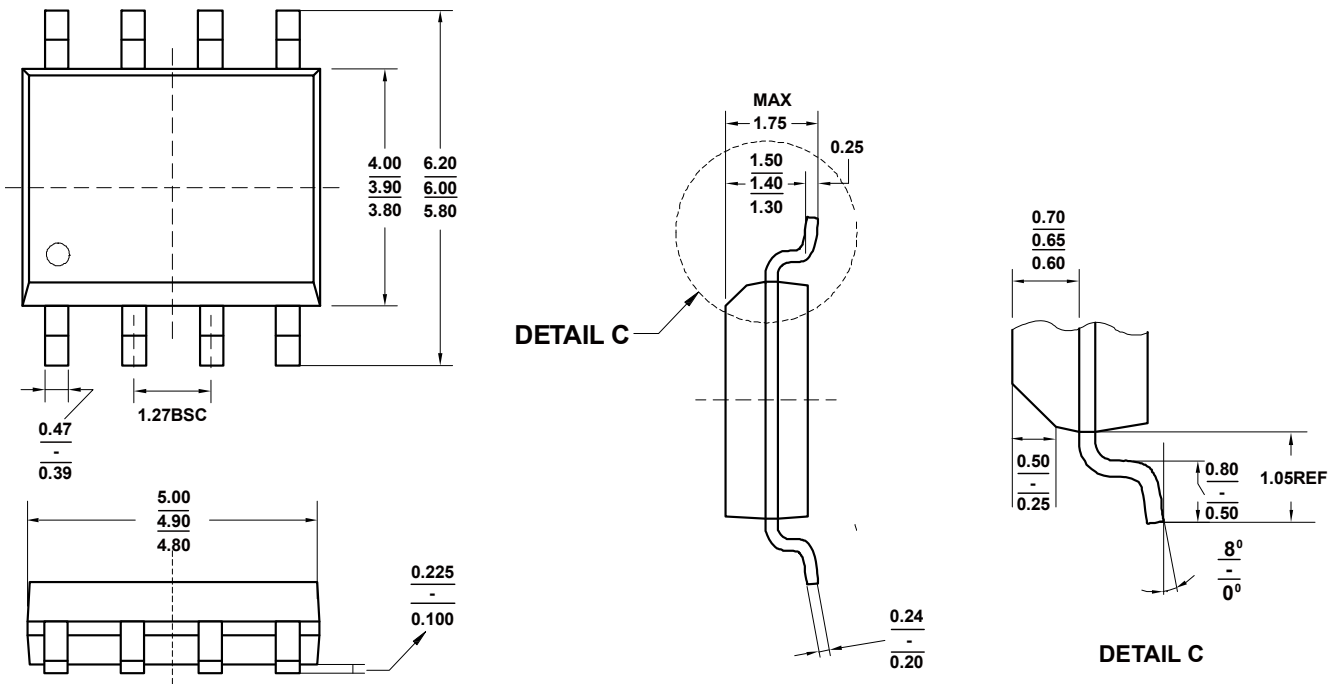


Figure 44. 8-Lead SOIC Package Dimensions shown in millimeters

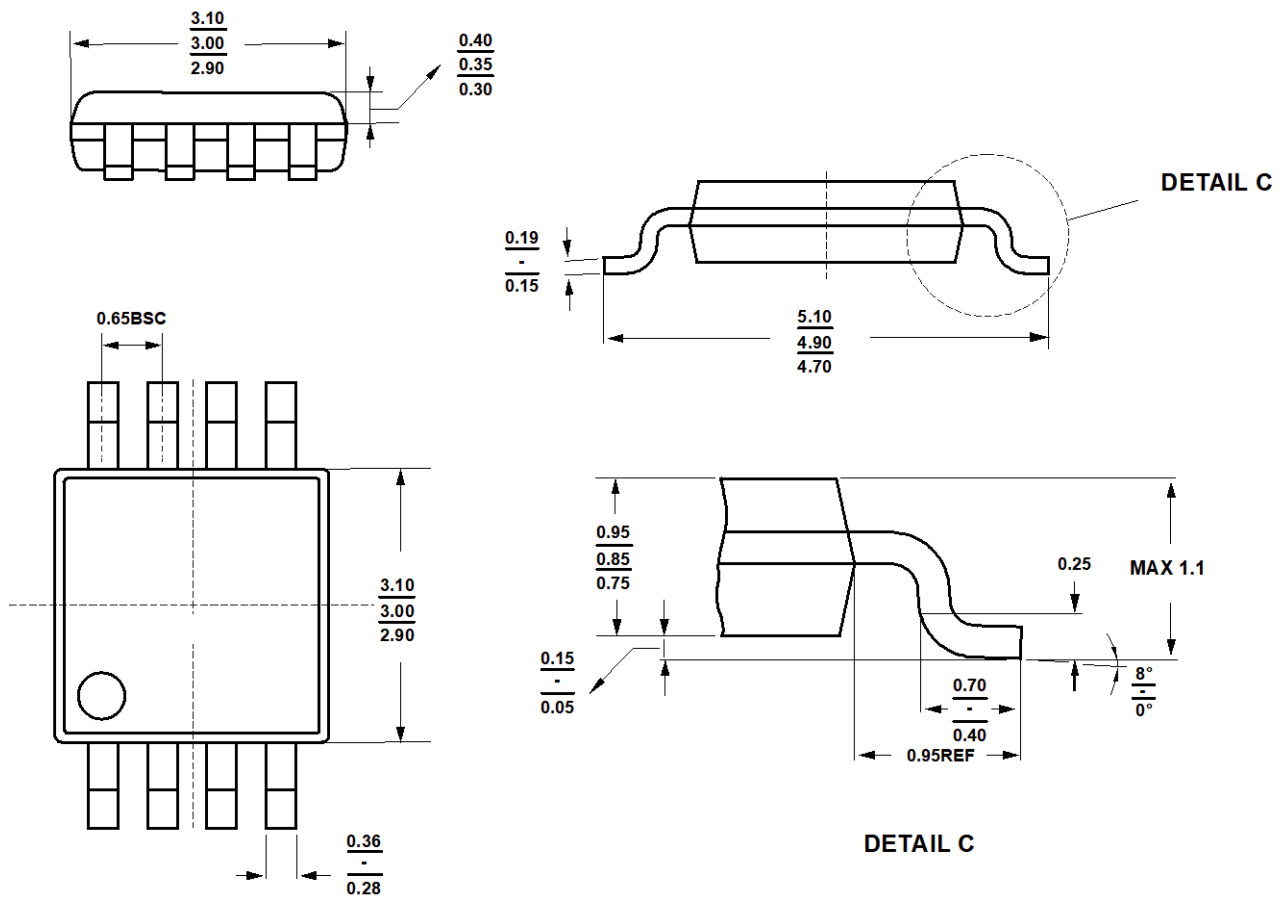


Figure 45. 8-Lead MSOP Package Dimensions shown in millimeters

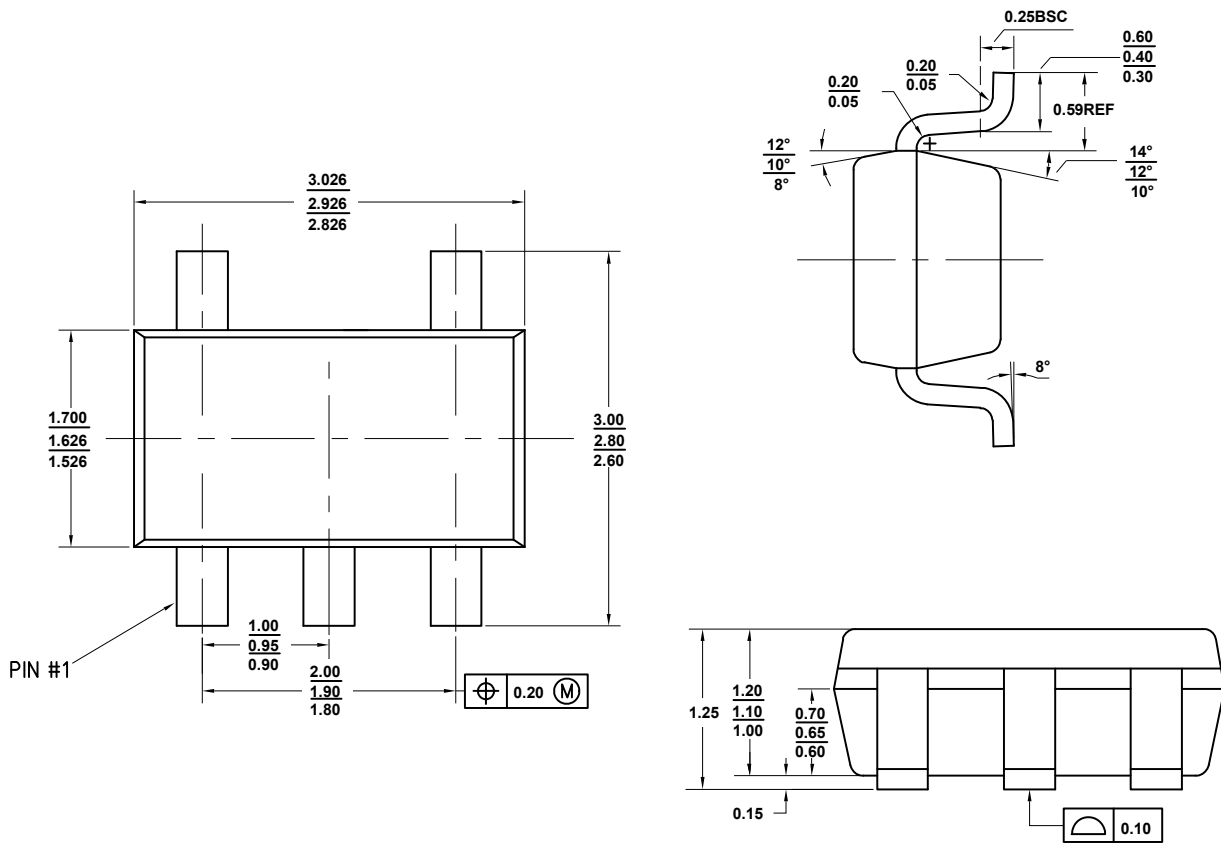


Figure 46. 5-Lead SOT23 Package Dimensions shown in millimeters

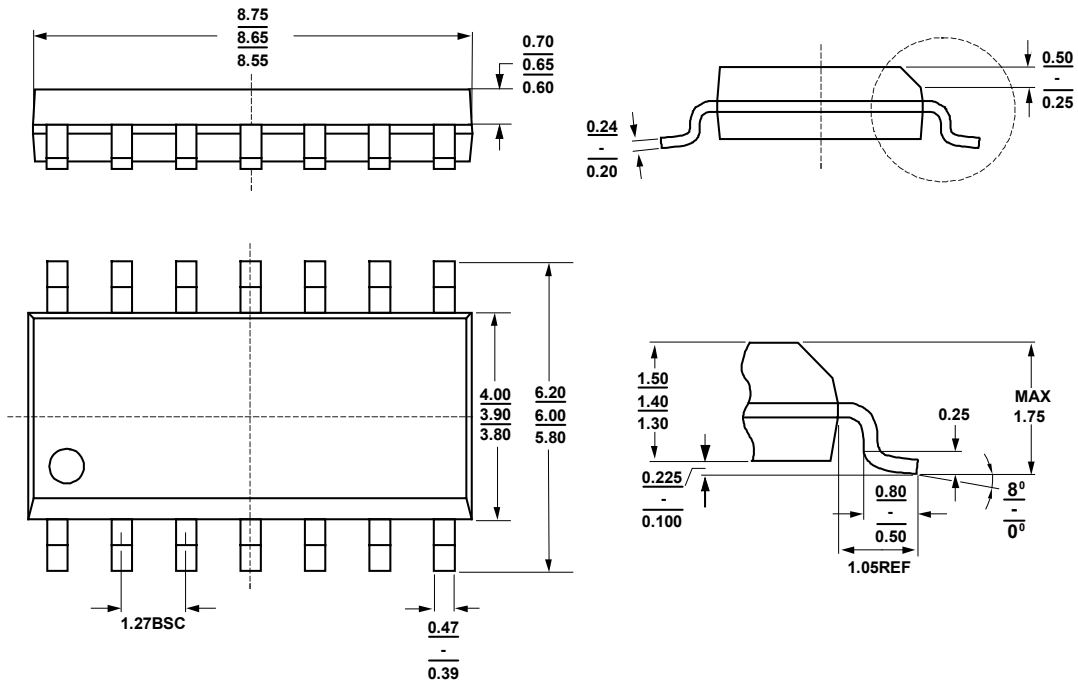


Figure 47. 14-Lead SOIC Package Dimensions shown in millimeters

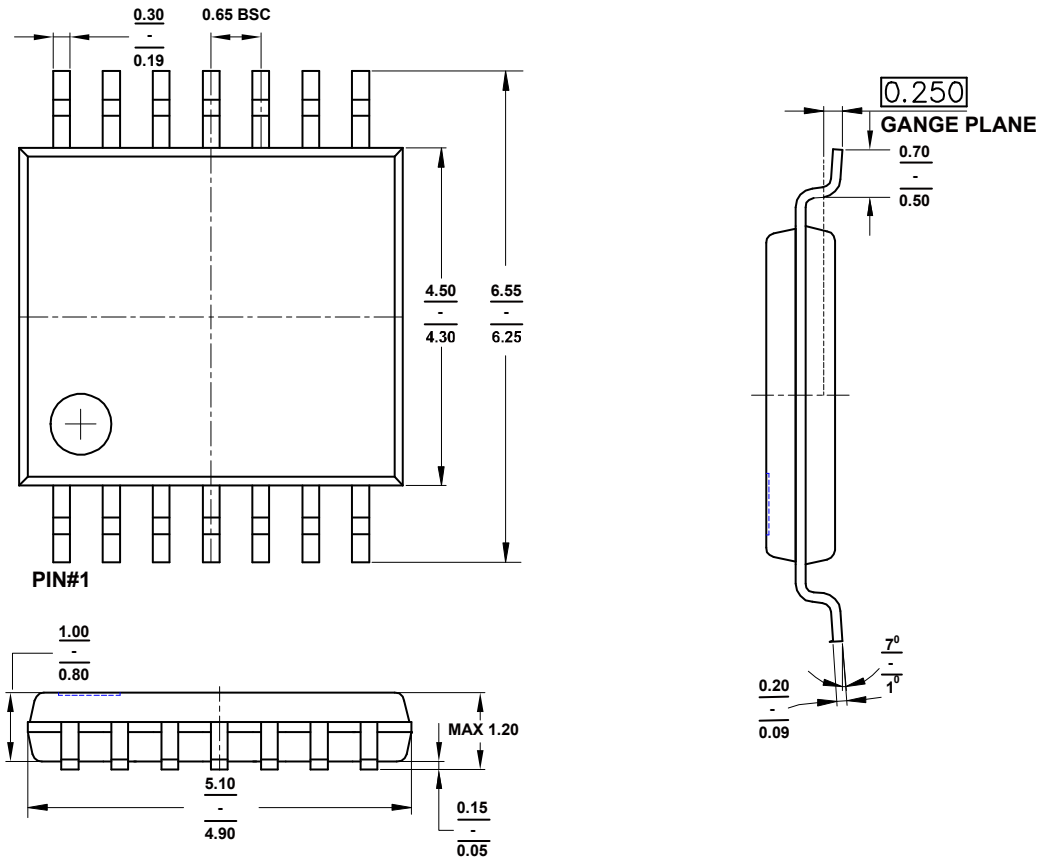


Figure 48. 14-Lead TSSOP Package Dimensions shown in millimeters

## Ordering Guide

Model	Orderable Device	Status <sup>1</sup>	Channels	Package	Temperature Range (°C)	External Package
AD8615	AD8615R	ACTIVE	1	SOT23-5	-40 to +125	7" Reel
AD8656	AD8656ARZ	ACTIVE	2	SOIC-8	-40 to +125	Tube
	AD8656ARZ-REEL7	ACTIVE				13" Reel
	AD8656BRZ	ACTIVE		MSOP-8		Tube
	AD8656BR	ACTIVE				13" Reel
AD8618	AD8618CR	PREVIEW	4	SOIC-14	-40 to +125	Tube
	AD8618CRZ	PREVIEW				13" Reel
	AD8618CRB	PREVIEW		TSSOP-14		Tube
	AD8618CS	PREVIEW				13" Reel
AD8616	AD8616R	PREVIEW	1	SOT23-5	-40 to +125	7" Reel