



MK SD Card Specification

Industrial . High Endurance

Product List

MKSD032G-CGT1A / MKSD064G-CGT1A / MKSD128G-CGT2A

www.mkfounder.com



Revision History

Version	Date	Description
Rev 1.0	2022/05/11	<i>Released</i>
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1. Introduction

The SD6.1 Cards are fully compatible with Physical Layer Specification, Version 6.10 (this specification is available from the SDA), support Ultra High Speed(UHS), provides high write/read speed and high IOPS, It was designed to meet the security, high capacity, high performance and environmental requirements inherent in next generation consumer electronic devices.

The SD card system is a new mass-storage system based on innovations in semiconductor technology. It has been developed to provide an inexpensive, mechanically robust storage medium in card form for multimedia consumer applications. SD card allows the design of inexpensive players and drivers without moving parts. A low power consumption and a wide supply voltage range favors consumer electronic devices.

Ultra High Speed (UHS) Card

It provides up to 104MB/s* performance. UHS cards are backward compatible on non-UHS hosts.

*Based on internal testing; performance may vary depending upon host device.

1 megabyte (MB) =1,000,000bytes.

2. Product List

Part Number	Capacity	Flash Type	Actual Size	Speed Class (Note1)	W/R Speed (Note1)	UHS-I (Note1)	Type
MKSD032G-CGT1A	32GB	TLC	29.12GB	V30 A2	Up to 130/160 MB/s	SDR104	SDXC
MKSD064G-CGT1A	64GB	TLC	58.24GB	V30 A2	Up to 130/160 MB/s	SDR104	SDXC
MKSD128G-CGT2A	128GB	TLC	116.48GB	V30 A2	Up to 130/160 MB/s	SDR104	SDXC

Table 1 Product List

Note1 :

*Measurement based on VTE3100 & VTE4100 Test Metrix device, SW 3.2A software or up version; The card must be reformatted between each script test.

Test scripts:

SD_Card(Spec3.0_High&Extended-Capacity_UHS-I and Non-UHS-I)_Compliance [rev32A]-B87.vte;

SD_Card (Spec2.0-3.0 High&Extended-Capacity_UHS-I) Performance-Speed (Multiple Block Sequential) [rev31M] - SDR104-With Background Data.vte;

SD_Card (Spec3.0-4.0 HC & XC -UHS-I) SD 3.0 Speed Class (Grade 1/3) [rev32A].vte

SD [Spec 5.1_HC&XC_UHS-I] Speed Class (Grade 1) & VSC_6_10_30 [VTE4100, Rail_UHS-I+II] SK1 [5.2.0.2-52B-A05].vte;

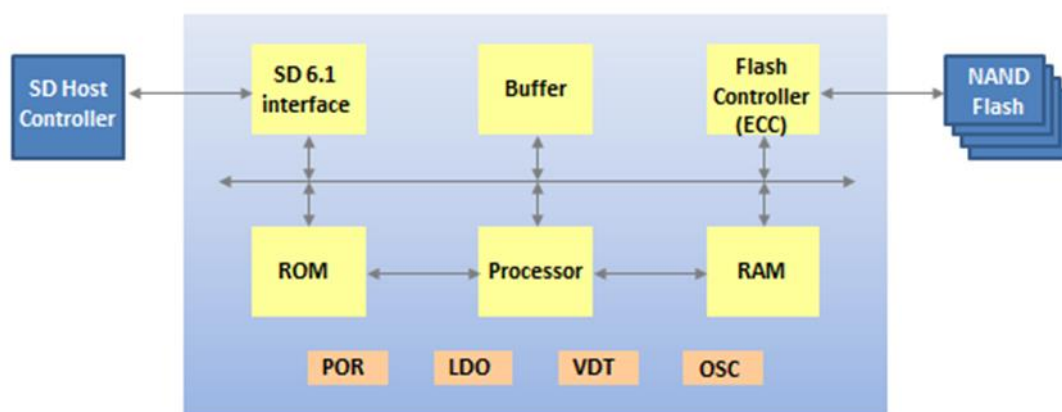
SD [Spec 5.1_HC&XC_UHS-I] A1 Test - SDR50 (w CMD12_DB) [VTE4100, Rail_UHS-I+II] SK1 [5.2.0.1-52A-A00].vte;

*Maximum speed differs from the bus I/F speed. It varies depending upon the card performance. The average speed that a device writes to an SD memory card may vary depending upon the device and the operation it is performing. Normal and high-speed cards can also be used with UHS-I host devices, but the high performance enabled by a UHS-I host device can only be achieved with a UHS-I memory card

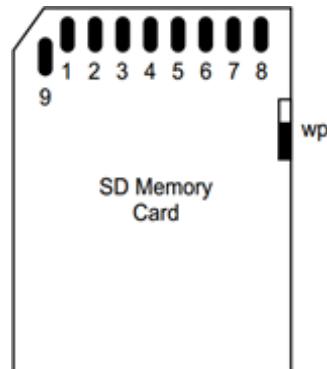
3. Features

- Complies to SD specifications version 6.1
- Voltage operating: 2.7~3.6V.
- Targeted for portable and stationary applications
- Bus Speed Mode:
 - DS-Default Speed mode: 3.3V signaling, frequency up to 25MHz, up to 12.5MB/sec
 - HS-High Speed mode: 3.3V signaling, frequency up to 50MHz, up to 25MB/sec
 - SDR12-1.8V signaling, frequency up to 25MHz, up to 12.5MB/sec
 - SDR25-1.8V signaling, frequency up to 50MHz, up to 25MB/sec
 - SDR50-1.8V signaling, frequency up to 100MHz, up to 50MB/sec
 - SDR104-1.8V signaling, frequency up to 208MHz, up to 104MB/sec
 - DDR50-1.8V signaling, Frequency up to 50 MHz, sampled on both clock edges, up to 50MB/sec
- Switch function command supports Bus Speed Mode, Command System, Drive Strength, and future functions.
- password protection (CMD42-LOCK_UNLOCK)
- LDPC ECC & Global Wear Leveling
- Power management for low power operation

Functional Block Diagram



4. Pin Assignment



Pin No.	SD Mode			SPI Mode		
	Name	Type	Description	Name	Type	Description
1	CD/DAT ₃	I/O/PP	Card Detect / Data Line [Bit 3]	CS	$\bar{3}$	Chip Select (neg true)
2	CMD	PP	Command/Response	DI	I	Data In
3	VSS	S	Supply voltage ground	VSS1	S	Supply voltage ground
4	VDD	S	Supply voltage	VDD	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	VSS	S	Supply voltage ground	VSS2	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit 0]	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line [Bit 1]	RSV		-
9	DAT2	I/O/PP	Data Line [Bit 2]	RSV		-

S: power supply; I: input; O: output; PP: I/O using push-pull drivers

Table 2 Pin Assignment

5. Current Consumption

- Standby current: 150uA (Maximum value)
- Standby current: 100uA (average value)
- Operating current: 100mA (Maximum value)
- Operating current: 80mA (average value)

*Test condition: Realtek5329 card reader @SDR104, VCC=3.3v

6. Reliability and Durability

Temperature	Operation: -25°C/85°C Storage: -40°C/85°C
Moisture and corrosion	Operation: 25°C/95% rel. humidity Storage: 40°C/93% rel. hum./500h Salt Water Spray: 3% NaCl/35°C; 24h acc. MIL STD Method 1009
Durability	10,000 insertion/removal cycles;
Bending	10[N] Center 200[mm/minute] 60[sec]
Torque	0.10Nm, +/-2.5 deg.max.
Drop test	1.5m free fall
Electrostatic Discharge (ESD)	IEC 61000-4-2 contact discharge: +/- 2[kV] and +/- 4[kV] 150[pF],330[Ohm] air discharge: up to +/- 15[kV] 150[pF], 330[Ohm]

Table 3 Reliability and Durability

7. SD Card Registers

7.1. Card Identification Register (CID)

The Card Identification (CID) register is 128 bit wide. It contains the card identification information used during the card identification phase. Every individual flash card shall have a unique identification number.

The structure of the CID register is defined in the following table.

CID Bit	Width	Name	Field
[127:120]	8	Manufacture ID	MID
[119:104]	16	OEM/Application ID	OID
[103:64]	40	Product Name	PNM
[63:56]	8	Product Revision	PRV
[55:24]	32	Product Serial Number	PSN
[23:20]	4	Reserved	---
[19:8]	12	Manufacturing Date	MDT
[7:1]	7	CRC7 check sum	CRC
[0]	1	Not used,always"1	---

Table 4 SD Card CID Table

All contents in the CID table are programmable; Manufacturers can update the CID data through utility. Manufacturers should license MID and OID field form the SD Card Association(SDA)

7.2. Card Specific Data Register (CSD)

The Card-Specific Data register provides information regarding access to the card contents. The CSD defines the data format, error correction type, maximum data access time, whether the DSR register can be used, etc. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27. The CSD Table Version 2.0(as shown below) is applied to SDHC and SDXC Cards. Note that bits [15:0] are programmable by the host side. Refer to the SD specification for detailed information.

CSD Bit	Width	Name	Field	Value	Note
[127:126]	2	CSD structure	CSD_STRUCTURE	01b	V2.0(>2G B Card)
[125:120]	6	Reserved	---	---	---
[119:112]	8	Data read access-time 1	(TAAC)	0E h	
[111:104]	8	Data read access-time2 in CLK cycles(NSA*100)	(NSAC)	00 h	
[103:96]	8	Max data transfer rate	(TRAN_SPEED)	32 h 5A h 0B h 2B h	
[95:84]	12	Card command classes	CCC	5B5 h	
[83:80]	4	Max. read data block length	(READ_BL_LEN)	9 h	512 Byte
[79]	1	Partial block read allowed	(READ_BL_PARTIAL)	0	
[78]	1	Write block misalignment	(WRITE_BLK_MISALIGN)	0	
[77]	1	Read block misalignment	(READ_BLK_MISALIGN)	0	
[76]	1	DSR implemented	DSR_IMP	x	
[75:70]	6	Reserve	---	---	
[69:48]	22	Device size	C_SIZE	xxxxxxh	
[47]	1	Reserved	---	0	
[46]	1	Erase single block enable	(ERASE_BLK_EN)	1	
[45:39]	7	Erase sector size	(SECTOR_SIZE)	7F h	
[38:32]	7	Write protect group size	C_SIZE	0 b	
[31]	1	Write protect group enable	---	0	
[30:29]	2	Reserved	(ERASE_BLK_EN)	0 b	
[28:26]	3	Write speed factor	(SECTOR_SIZE)	010 b	
[25:22]	4	Max. write data block length	(WP_GRP_SIZE)	9 h	
[21]	1	Partial block write allowed	(WP_GRP_ENABLE)	0	
[20:16]	5	Reserved	---	---	
[15]	1	File format group	(FILE_FORMAT_GRP)	0	
[14]	1	Copy flag	COPY	x	
[13]	1	Permanent write protection	PERM_WRITE_PROTECT	x	
[12]	1	Temporary write protection	TMP_WRITE_PROTECT	x	
[11:10]	2	File format	(FILE_FORMAT)	00 b	
[9:8]	2	Reserved	---	00 b	
[7:1]	7	CRC	CRC	---	
[0]	1	Not used,always '1'	---	1	

Table 5 CSD (Version 2.0) Table

8. Bus Operation Conditions

8.1. For 3.3V Signaling

8.1.1. Threshold Level for High Voltage Range

Parameter	Symbol	Min	Max	Unit	Remark
Supply Voltage	V _{DD}	2.7	3.6	V	
Output High Voltage	V _{OH}	0.75* V _{DD}		V	I _{OH} =2mA V _{DD} min
Output Low Voltage	V _{OL}		0.125* V _{DD}	V	I _{OL} =2mA V _{DD} min
Input High Voltage	V _{IH}	0.625* V _{DD}	V _{ss} +0.3	V	
Input Low Voltage	V _{IL}	V _{ss} -0.3	0.25* V _{DD}	V	
Power Up Time			250	ms	From 0V to V _{DD} min

Table 6 Threshold Level for High Voltage

8.1.2. Peak Voltage and Leakage Current

Parameter	Symbol	Min	Max	Unit	Remark
Peak voltage on all lines		-0.3	V _{DD} +0.3	V	
All Inputs					
Input Leakage Current		-10	10	uA	
All Outputs					
Output Leakage Current		-10	10	uA	

Table 7 Peak Voltage and Leakage Current

8.1.3. Bus Signal Line Load

Parameter	Symbol	Min	Max	Unit	Remark
Pull-up resistance	RCMD RDATA	10	100	K Ω	To prevent bus floating
Total bus capacitance for each signal line	C _L		40	pF	1 card C _{HOST} +C _{BUS} shall not exceed 30pF
Card capacitance for each signal pin	CCARD		10	pF	
Maximum signal inductance			16	nH	
Pull-up resistance inside card(pin1)	RDATA3	10	90	K Ω	May be used for card detection
Capacity Connected to Power Line	C _C		5	μ F	To prevent inrush current

Table 8 Bus Operating Conditions - Signal Line's Load

8.1.4. Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.

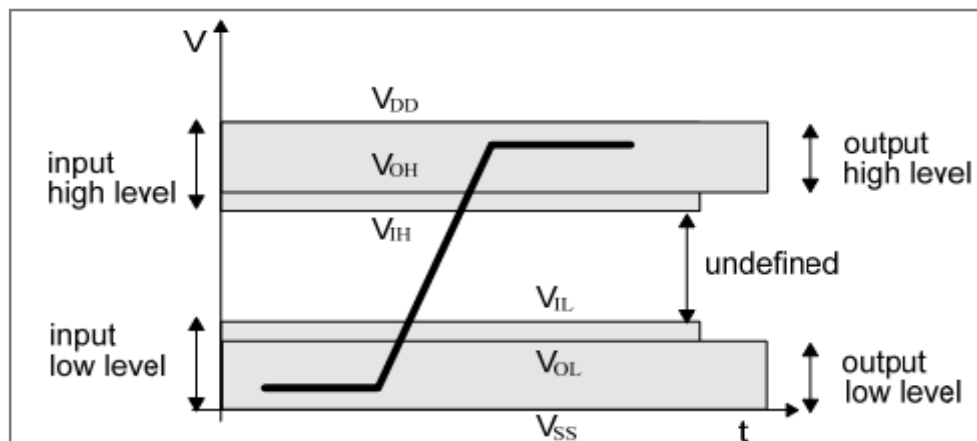
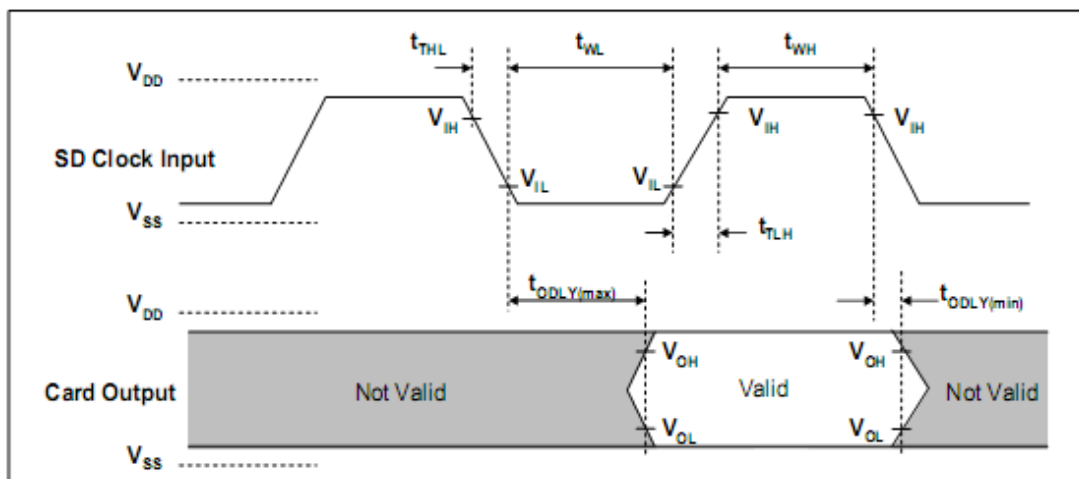
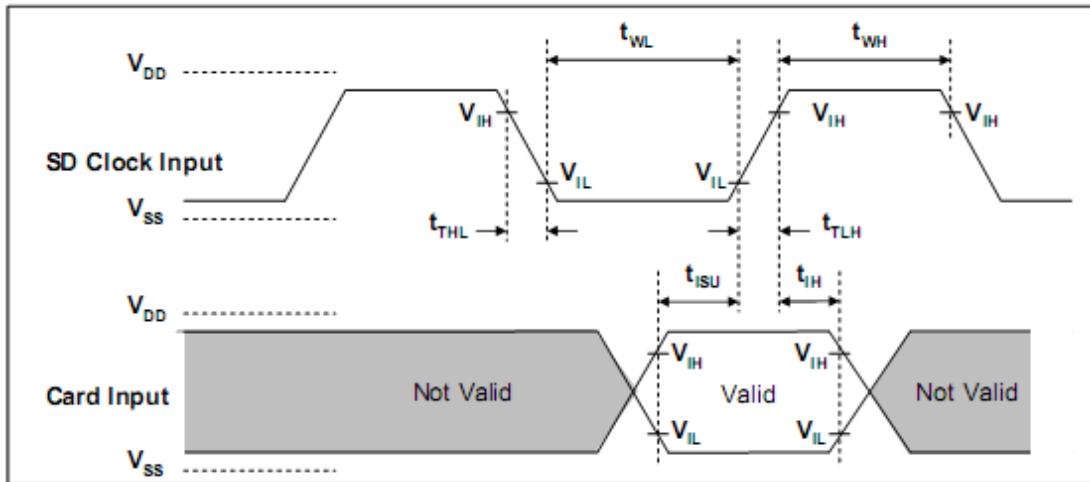


Figure 1: Bus Signal Levels

To meet the requirements of the JEDEC specification JESD8-1A and JESD8-7, the card input and output voltages shall be within the specified ranges shown in Table 6-2 for any VDD of the allowed voltage range:

8.1.5. Bus Timing(Default)



(1) 0 Hz means to stop the clock. The given minimum frequency range is for cases where continuous clock is required (refer to Chapter 4.4-Clock Control)

Parameter	Symbol	Min.	Max	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL}))					
Clock frequency data transfer Mode	fpp	0	25	MHz	$C_{CARD} \leq 10\text{pF}$ (1 card)
Clock frequency Identification Mode	fOD	0(1)/100	400	KHz	$C_{CARD} \leq 10\text{pF}$ (1 card)
Clock low time	tWL	10		ns	$C_{CARD} \leq 10\text{pF}$ (1 card)
Clock high time	tWH	10		ns	$C_{CARD} \leq 10\text{pF}$ (1 card)
Clock rise time	tTLH		10	ns	$C_{CARD} \leq 10\text{pF}$ (1 card)
Clock fall time	tTHL		10	ns	$C_{CARD} \leq 10\text{pF}$ (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	tISU	5		ns	$C_{CARD} \leq 10\text{pF}$ (1 card)
Input hold time	tIH	5		ns	$C_{CARD} \leq 10\text{pF}$ (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	tODLY	0	14	ns	$C_L \leq 40\text{pF}$ (1 card)
Output Hold time	tOH	0	50	ns	$C_L \leq 40\text{pF}$ (1 card)

Table 9: Bus Timing-Parameters Values (Default Speed)

8.1.6. Bus Timing (High-Speed Mode)

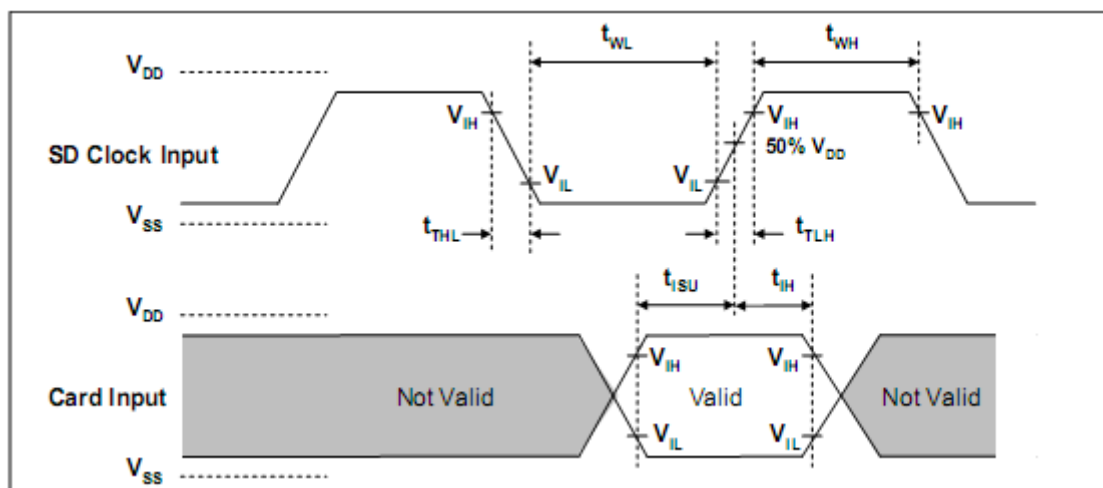


Figure 4: Card Input Timing(High Speed Card)

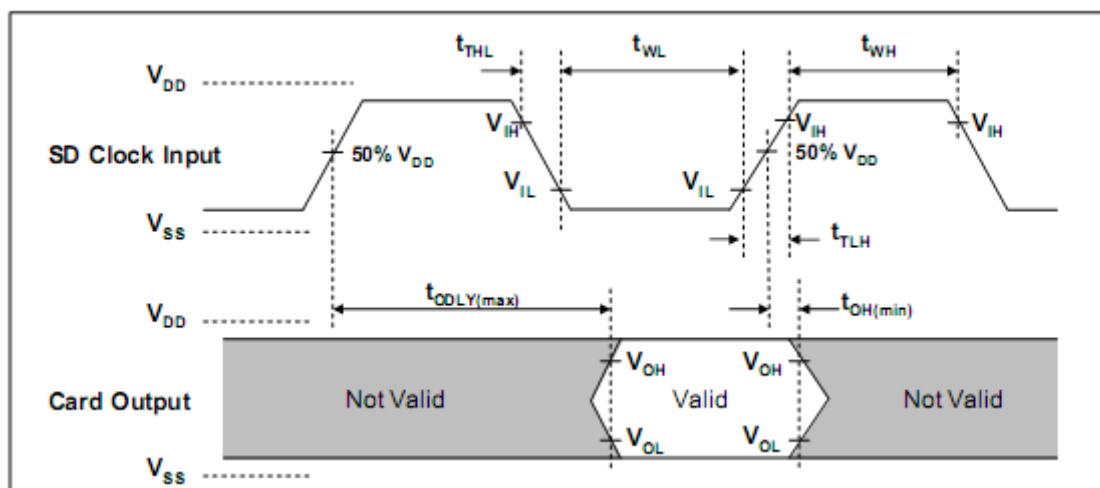


Figure 5: Card Output Timing(High Speed Mode)

Parameter	Symbol	Min.	Max	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL}))					
Clock frequency data transfer Mode	fpp	0	50	MHz	$C_{CARD} \leq 10\text{pF}$ (1 card)
Clock low time	tWL	7		ns	$C_{CARD} \leq 10\text{pF}$ (1 card)
Clock high time	tWH	7		ns	$C_{CARD} \leq 10\text{pF}$ (1 card)
Clock rise time	tTLH		3	ns	$C_{CARD} \leq 10\text{pF}$ (1 card)
Clock fall time	tTHL		3	ns	$C_{CARD} \leq 10\text{pF}$ (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	tISU	6		ns	$C_{CARD} \leq 10\text{pF}$ (1 card)
Input hold time	tIH	2		ns	$C_{CARD} \leq 10\text{pF}$ (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	tODLY		14	ns	$C_L \leq 40\text{pF}$ (1 card)
Output Hold time	tOH	2.5		ns	$C_L \geq 15\text{pF}$ (1 card)
Total System capacitance for each line ¹	C_L		40	pF	1 card

(1) In order to satisfy sever timing , host shall drive only one card.

Table 10: Bus Timing – Parameters Values (High Speed)

8.2. For 1.8V Signaling

8.2.1. Threshold Level for High Voltage Range

Parameter	Symbol	Min	Max	Unit	Remark
Supply Voltage	VDD	2.7	3.6	V	
Regulator Voltage	VDDIO	1.7	1.95	V	Generated by VDD
Output High Voltage	VOH	1.4		V	IOH=2mA VDD min
Output Low Voltage	VOL		0.45	V	IOL=2mA VDD min
Input High Voltage	VIH	1.27	2.0	V	
Input Low Voltage	VIL	V _{SS} -0.3	0.58	V	

Table 11 Threshold Level for High Voltage

8.2.2. Peak Voltage and Leakage Current

Parameter	Symbol	Min	Max	Unit	Remark
Input Leakage Current		-2	2	uA	DAT3 pull-up is disconnected

Table 12: Peak Voltage and Leakage Current

8.2.3. Bus Timing Specification in SDR12, SDR25, SDR50 and SDR104 Modes

8.2.3.1. Clock Timing

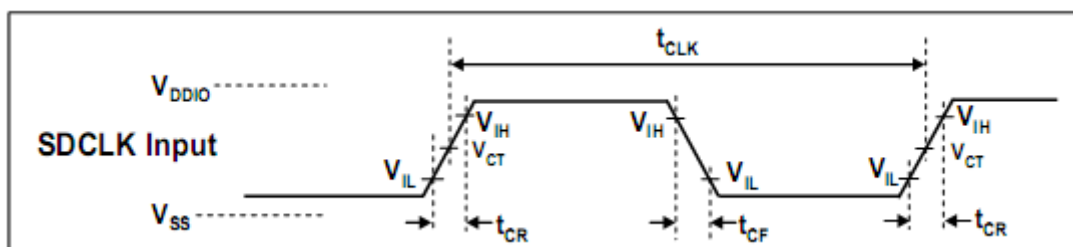


Figure 6: Clock Signal Timing

Symbol	Min	Max	Unit	Remark
tCLK	4.8	-	ns	208MHz (Max.), Between rising edge, $V_{CT}=0.975V$
tCR, tCF	-	$0.2 \cdot t_{CLK}$	ns	tCR, tCF < 2.00ns (max.) at 208MHz, CCARD=10pF tCR, tCF < 2.00ns (max.) at 100MHz, CCARD=10pF The absolute maximum value of tCR, tCF is 10ns regardless of clock frequency.
Clock Duty	30	70	%	

Table 13 Clock Signal Timing

8.2.3.2. Card Input Timing

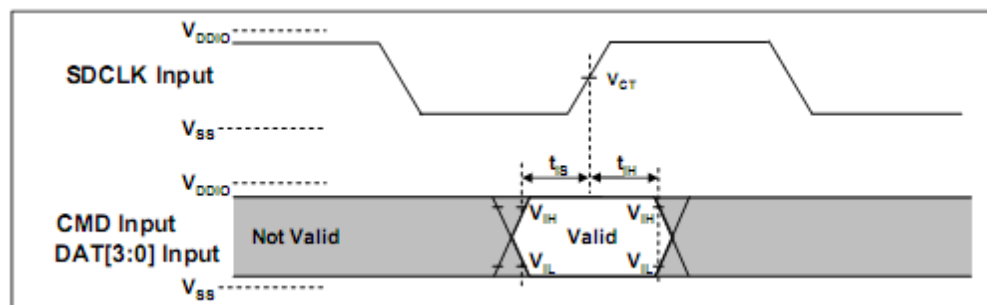


Figure 7: Card Input Timing

Symbol	Min	Max	Unit	SDR104 mode
tIS	1.40	-	ns	C _{CARD} = 10pF, $V_{CT} = 0.975V$
tIH	0.80		ns	C _{CARD} = 5pF, $V_{CT} = 0.975V$
Symbol	Min	Max	Unit	SDR12, SDR25 and SDR50 modes
tIS	3.00	-	ns	C _{CARD} = 10pF, $V_{CT} = 0.975V$
tIH	0.80	-	ns	C _{CARD} = 5pF, $V_{CT} = 0.975V$

Table 14 SDR50 and SDR104 Input Timing

8.2.3.3. Card Output Timing

8.2.3.3.1. Output Timing of Fixed Data Window (SDR12, SDR25 and SDR50)

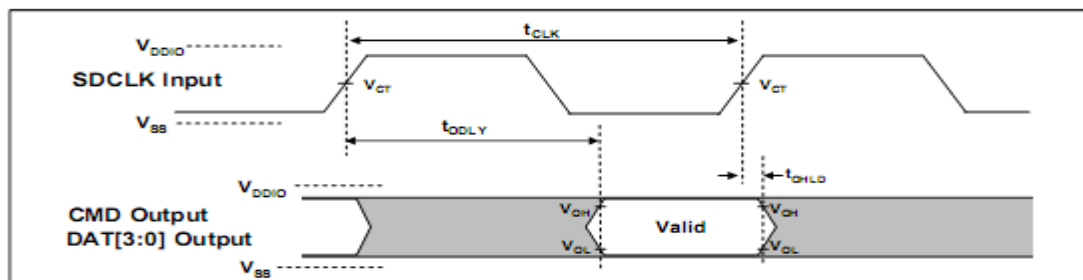


Figure 8: Output Timing of Fixed Data Window

Symbol	Min	Max	Unit	Remark
t _{ODLY}	-	7.5	ns	t _{CLK} ≥ 10.0ns, CL=30pF, using driver Type B, for SDR50.
t _{ODLY}		14	ns	t _{CLK} ≥ 20.0ns, CL=40pF, using driver Type B, for SDR25 and SDR12.
t _{OH}	1.5	-	ns	Hold time at the t _{ODLY} (min.). CL=15pF

Table 15 Output Timing of Fixed Data Window

8.2.3.3.2. Output Timing of Variable Window (SDR104)

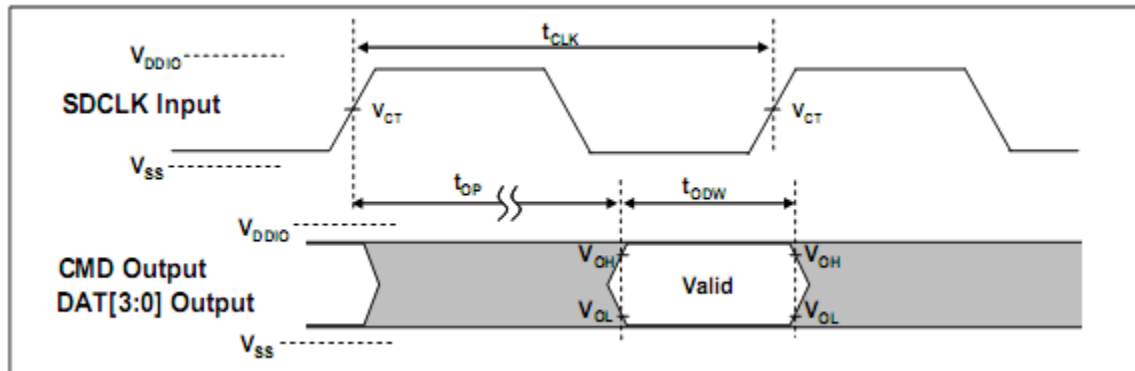


Figure 9: Output Timing of Variable Data Window

Symbol	Min	Max	Unit	Remark
t_{OP}	-	2	UI	Card Output Phase
Δt_{OP}	-350	+1550	ps	Delay variation due to temperature change after tuning
t_{ODW}	0.60	-	UI	$t_{ODW} = 2.88\text{ns}$ at 208MHz

Table 16 Output Timing of Variable Data Window

8.2.4. Bus Timing Specification in DDR50 Mode

8.2.4.1. Clock Timing

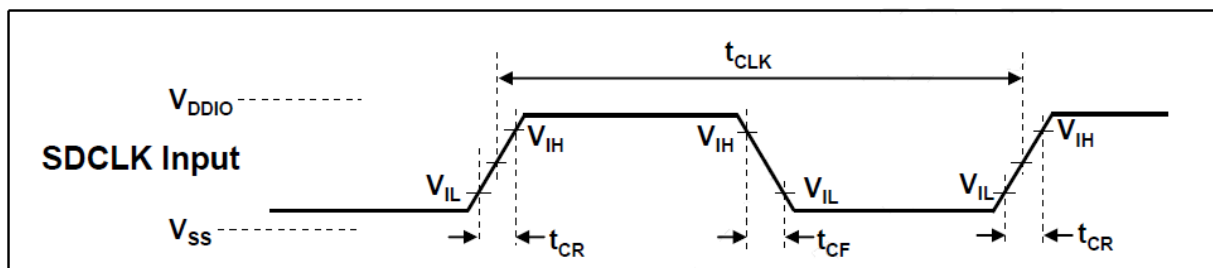


Figure 10: Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{cLK}	20	-	ns	50MHz (Max.), Between rising edge
t_{CR}, t_{CF}	-	$0.2 \cdot t_{cLK}$	ns	$t_{CR}, t_{CF} < 4.00\text{ns}(\text{max.})$ at 50MHz, CCARD=10pF
Clock Duty	45	55	%	

Table 17 Clock Signal Timing

8.2.4.2. Bus Timing for DDR50

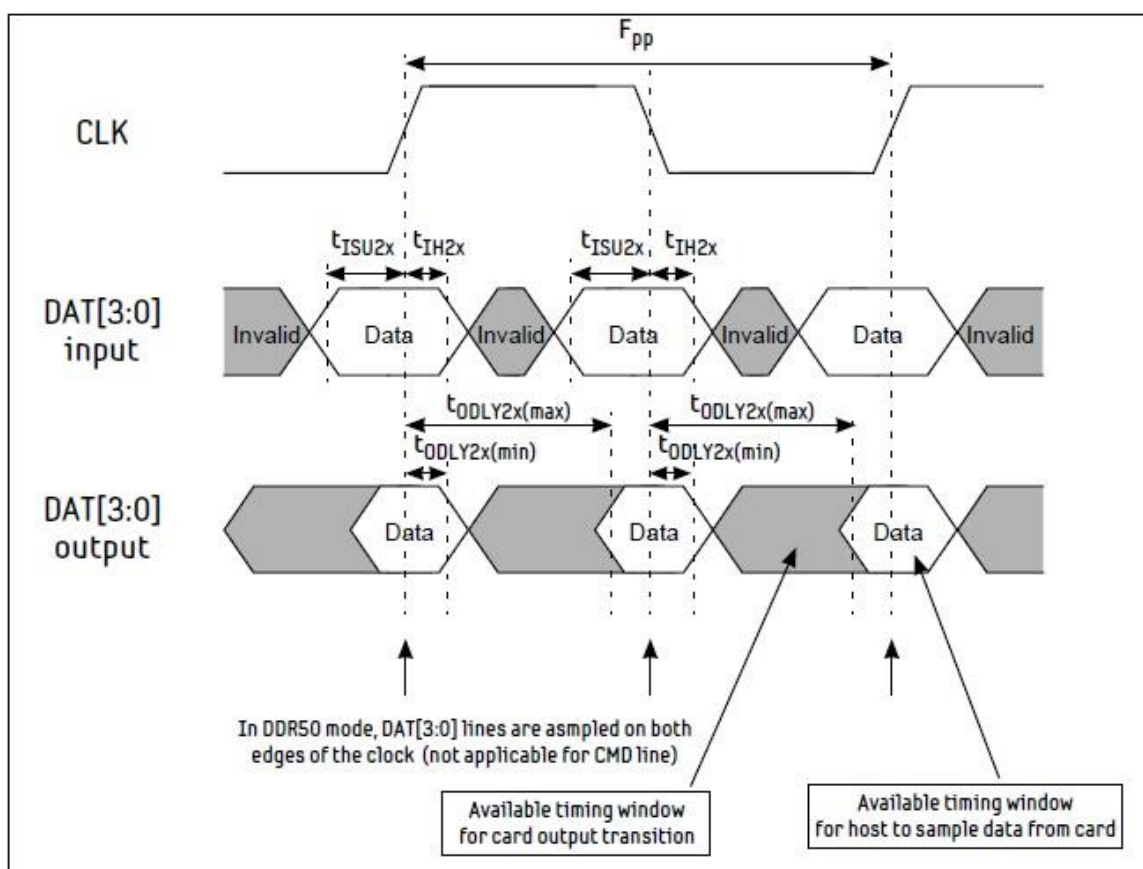


Figure 11: Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

Parameter	Symbol	Min.	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input set-up time	t _{ISU}	3	-	ns	C _{CARD} ≤ 10pF (1 card)
Input hold time	t _{IH}	0.8	-	ns	C _{CARD} ≤ 10pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output Delay time during Data Transfer Mode	t _{ODLY}	-	13.7	ns	C _L ≤ 30pF (1 card)
Output hold time	t _{OH}	1.5	-	ns	C _L ≥ 15pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
Input set-up time	t _{ISU2x}	3	-	ns	C _{CARD} ≤ 10pF (1 card)
Input hold time	t _{IH2x}	0.8	-	ns	C _{CARD} ≤ 10pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output Delay time during Data Transfer Mode Transfer Mode	t _{ODLY2x}	-	7.0	ns	C _L ≤ 25pF (1 card)
Output hold time	t _{ODLY2x}	1.5	-	ns	C _L ≥ 15pF (1 card)

Table 18 Bus Timings – Parameters Values (DDR50 mode)

9. Physical Dimension

Type	Measurement
Length	32.00mm ±0.10mm
Width	24.00mm ±0.10mm
Thickness	2.10mm ±0.15mm
Weight	Approx.2.0 gram

Table 19 Physical Dimension Specifications (Unit in mm)

Mechanical form factor as follows: (Unit in mm)

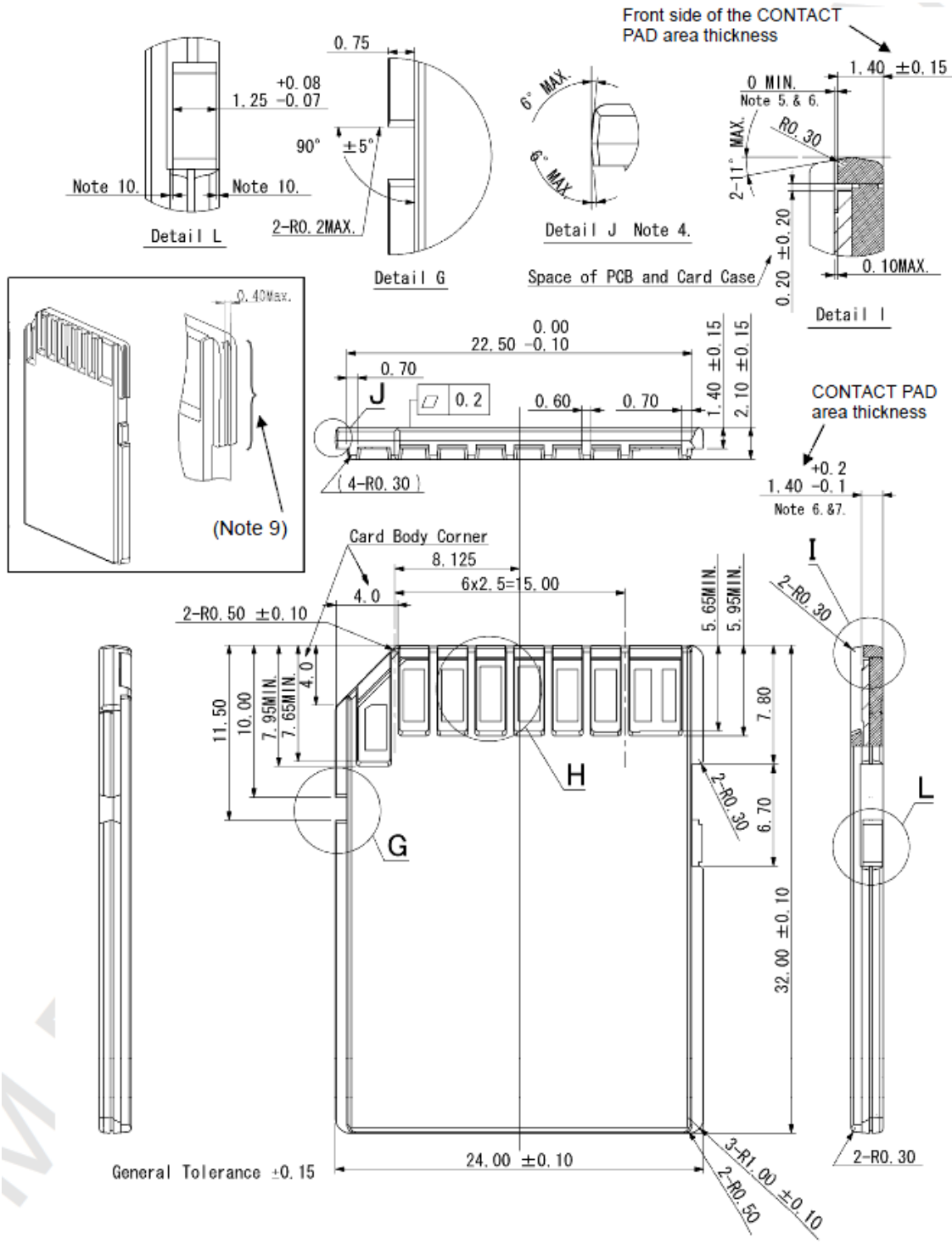


Figure 10: Dimension Drawing