VSC8514

User Guide

VSC8514 Evaluation Board

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Microsemi

a Microchip company

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1 Revision History

The revision history describes the changes that were implemented in this document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 of this datasheet was published in March 2014. This was the first publication of the document.

2 Introduction

The VSC8514 device is a low-power, quad-port Gigabit Ethernet transceiver with copper media interfaces. The device includes an integrated quad two-wire serial multiplexer (MUX) to control power over Ethernet (PoE) modules. It features low electromagnetic interference (EMI) line drivers and integrated line side termination resistors that conserve both power and board space. Dual recovered clock outputs are available to support Synchronous Ethernet (Sync-E) applications, each with programmable squelch options.

This document describes the architecture and usage of the VSC8514 Evaluation Board (VSC8514EV). The Quick Start section describes how to install and run the graphical user interface (GUI) to fully control the evaluation board.

Figure 1 • VSC8514 Evaluation Board

Additional VSC8514 collateral for both the VSC8514 device and VSC8514EV, including schematics, layout, GUI, and application notes can be found on the VSC8514 product web page at: https://www.vitesse.com/products/product.php?number=VSC8514.

3 General Description

The evaluation board, shown in Figure 1, provides the user a way to evaluate the VSC8514 device in multiple configurations. Four RJ-45 connectors are provided for copper media interfaces. The MAC interface is exposed via SMA connectors.

For access to all of the features of the device, an external microcontroller is used to configure the on-board clock chip via a two wire serial bus and the VSC8514 via the MDIO bus. The GUI enables the user to read and write device registers.

3.1 Key Features

3.1.1 Copper Port RJ45 Connections

PHY ports 2 and 3 use the UDE RTA 1648BAK1A with integrated magnetic while PHY ports 0 and 1 use generic RJ45 connectors with discrete Pulse H5008NL magnetics.

SGMII/QSGMII MAC SMA

The QSGMII differential input port is available through SMA connectors J1 and J2, while the output port is available through SMA connectors J4 and J5. Both of them are AC coupled.

Switch Block Control

SW1 controls COMA_MODE, CLK_SQUELCH_IN and REFCLKSEL_[1:0]. The default configuration is with all switches set to low as shown in the figure below.

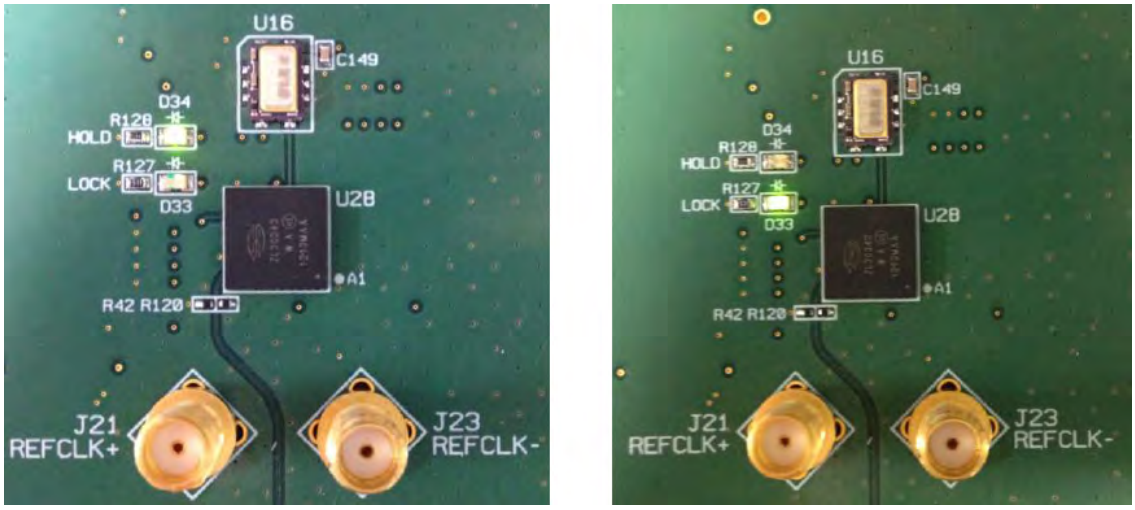
Figure 2 • SW1 Switch Control

3.1.2 Zarlink ZL30343 SyncE G.8262/SETS

The Silabs F311 micro-controller is pre-programmed to configure the Zarlink ZL30343 to provide a 125 MHz differential LVPECL clock to the VSC8514 REFCLK input, either based on the 20 MHz on-board crystal, or RCVRDCLK1 from the VSC8514 (Sync-E mode). When RCVRDCLK1 is enabled to output a proper 125 MHz clock, the ZL30343 will generate a 125 MHz output clock synchronized to the RCVRDCLK1 and will switch from HOLDOVER mode to LOCK mode as indicated by LEDs D33 and D34 as shown in the figure below.

The left side of the illustration shows the HoldOver mode and the right side shows the Lock mode.

Figure 3 • ZL30343 LED Indication



3.1.3 External RefClk Option

The user may choose to provide an external PHY REFCLK via SMA connections to J21 and J23 (as shown in Figure 3 above). To route the SMA signals to the device the user must reorient the zero ohm resistors, R151, and R152.

3.1.4 Recovered Clocks

There are two recovered clocks available from the VSC8514, through J22 and J24. In the default configuration, CLK_SQUELCH_IN is pulled down, which disables the clock squelching and RCVRDCLK1 is connected to the Zarlink device while RCVRDCLK2 is connected to SMA connector J24. RCVRDCLK1 and RCVRDCLK2 connections can be reconfigured by replacing the zero ohm resistors, R19, and R22, respectively.

Network Interface Microcontroller Card

A “Rabbit” microcontroller card is included to facilitate a software interface to the registers on the VSC8514. The controller card has a hard coded static IP address. Refer to the label on the card for the value. This address is required by the user to initiate communications via the board and the GUI.

The factory programmed Rabbit board IP address is: **10.9.70.193**.

4 Quick Start

This section shows the quick start for VSC8514.

4.1 Connecting the Power Supply

The evaluation board uses 5 VDC to power the on-board regulators creating the 3.3 V, 2.5 V, and 1.0 V rails which drive the devices as well as modules. The evaluation board can be powered using the power pack which provides the 5 VDC. Simply plug the AC adaptor into a wall socket and the barrel end into J67 (see the upper right corner of Figure 1). Immediately the user should see several LEDs turn on.

The user may alternately connect the board to a bench style power supply by connecting the red banana plug to 5 VDC and the black banana plug to ground. If the supply provides 3 A the board should come alive as described above.

4.2 PC Software Installation

1. Download the ZIP file to the PC's root directory, normally C:\.
2. Extract to C:\
3. Double click the icon to launch the GUI (It is acceptable to drag the icon to the desktop)

4.3 Connecting to the Board to the PC

The Rabbit board can interface with a PC either through a direct connection to the PC or if configured properly through a local area network. The latter option requires the user to configure the Rabbit's IP address so as to properly reside on the user's network.

The IP address of the board should be written on the Rabbit network interface daughter board card. The default value should be 10.9.70.193. You will need to use this IP address to initially access the board for operation or to change its IP address.

4.3.1 Changing the IP Address of the Board

1. Determine and write down the new unique IP address you wish to change the board to.
2. Directly connect an Ethernet cable from a PC to the Rabbit board.
   NOTE: Some older PCs do not support auto-crossover on the Ethernet connection so a cross-over cable may be needed.
3. Launch a DOS command window by clicking on the Start->Run button and typing "cmd".
4. Within the DOS command window type "Telnet".
5. In the Telnet window, connect to the Rabbit board's address using the open command by typing open 10.9.70.193, as this is the factory default address.
6. You should have a prompt and be able to type help to get a list of commands available on the Rabbit.
   a.) If you are unable to connect, then most likely you will need to change the IP address of the connected PC to have the first 3 octets similar to the board by following the subsequent steps.
   b.) On the PC under Windows -> Control Panel ->Network Connections -> Local Area Connection, right mouse click for Properties. Under the General tab highlight Internet Protocol (TCP/IP) and click on Properties. From there enter the new PC IP address such as 10.9.70.yyy where yyy is a unique value and NOT the same as the Rabbit board. Once complete, return to step 4.
7. From the Telnet window, update the IP address by typing set ip <new IP address> <Enter>, where <new IP address> is in the form of xxx.xxx.xxx.xxx.
   After hitting <Enter> the IP address will change and the Rabbit will save the value and reboot which may take approximately 1 minute.
   The Telnet session will disconnect from the board.
8. Change your PC IP address to the same IP network as the Rabbit board.
9. Telnet to the Rabbit board.
10. Use the following commands to complete configuration of the Rabbit board configuration:
    a) set netmask xxx.xxx.xxx.xxx
    b) set gateway xxx.xxx.xxx.xxx
    c) save env

11. Please record and inform Microsemi of the new IP address of the board when you return so that Microsemi can connect to and reconfigure the board.
12. Re-label the Rabbit board with the new IP.

4.4 Using the Control Software

Connect the VSC8514EV Rabbit microcontroller's RJ-45 directly to the PC or through a network switch if properly configured. Apply 5 VDC to the EVB.

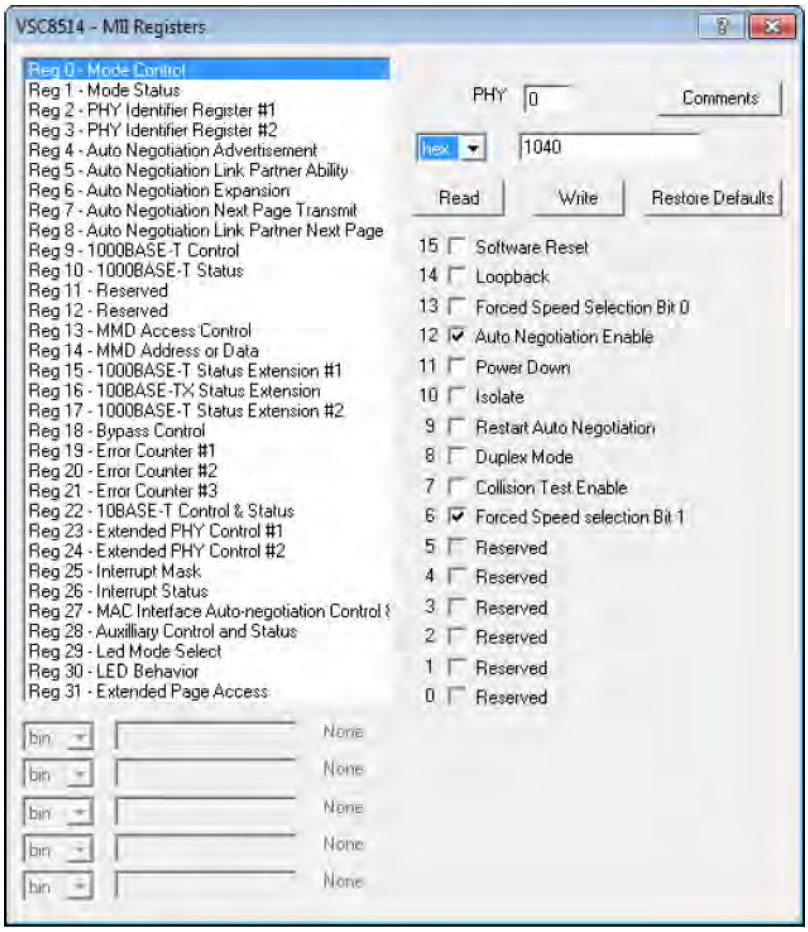
Launch the GUI by double clicking the GUI shortcut located in C:\EliseGUI_4_67 or on the desktop if it has been moved there. The GUI connection window shown in the figure below should appear.

Figure 4 • GUI Connection Window

To make a connection to the EVB, click "Rabbit" and enter the IP address of the EVB, then click on "Connect". The display next to the IP address window should change to "Connected". If it does not, check the IP address, or your network configuration until the connection with the EVB can be successfully established.

Double click on “MII Registers” and the window shown in the following figure should appear:

Figure 5 • MII Registers GUI Window



Be sure the device is up and running by reading MII Register 0. It should read back 0 × 1040. Reading back all 0’s or all 1’s indicates a problem. A checked box means the bit is set to “1,” if unchecked it is “0.”

4.4.1 Board Initialization

Once the evaluation board connectivity has been established and confirmed, the PHY should be initialized. Initialization can be accomplished by running an init-script sequence, such as performed by the pre- and post-reset functions of the PHY API standalone app.

While the init-script sequence may not be required for specific operational modes, an init-script sequence is highly recommended to ensure correct performance over the greatest set of user scenarios for the PHY. After initialization is performed, refer to the PHY datasheet section on configuring the PHY and PHY Interfaces for the desired application.

4.4.2 Copper Media Operation (Auto-negotiation Enabled)

A single register write and some external coax cables enables 1 G Ethernet traffic to be received by the VSC8514 RJ-45 port(s), routed through the VSC8514 and externally looped back via coax cables through the QSGMII interface and transmitted back to the traffic source on the same copper port(s).

The following steps are used to setup an external QSGMII loopback:

1. Set up the copper traffic source (i.e., IXIA or Smartbits)
2. Connect Ethernet cable(s) to a single or multiple RJ-45 ports.
3. Connect two matched coax cables, J1 - J4 and J2 - J5.
4. Write using the "Micro Page Registers" window: 19'd 0 × 400F.
5. Write using the "Micro Page Registers" window: 18'd 0 × 80E0.
6. When "Micro Page" 18'd is read back, bit 15 will clear.
7. Linkup bit is in MII Reg 1, bit 2 (MII 1.2), read twice to update.

Traffic should be the following:

4.4.3 Sync-E Operation

To enable 12 MHz Sync-E operation on this evaluation board a few register writes are required. Write 0 × 8101 on register 23'd of the "Micro Page Registers" to enable RCVRDCLK1 with PHY0 as the clock source when PHY0's link is up in a non-EEE mode and not 1000BT master or 10BT. To select a different port as the clock source or enable a recovered clock for EEE mode, refer to register 23 G in the datasheet for the programming detail. Set MII Reg.9 bit 12 to enable manual slave configuration then issue an auto negotiation restart through reg.0 bit 9.

4.5 Useful Registers

4.5.1 Ethernet Packet Generator

ExtMII 29E is the Ethernet Packet Generator register. Refer to the datasheet for configuration options.

A good CRC packet counter is in ExtMII 18.13:0. A read of the register reads back the good CRC packets and then clears the register so the subsequent reads will be 0 if no traffic has been received. If traffic has been received since the last read, bit 15 will be set.

4.5.2 Copper PHY Error Counters

Idle errors = MII 10.7:0
RX errors = MII 19.7:0
False carrier = MII 20.7:0
Disconnects = MII 21.7:0
CRC errors = ExtMII 23.7:0

4.5.3 Near-End Loopback

When the near-end loopback test feature is enabled, the transmitted data is looped back in the PCS block on the receive data signals. To enable the loopback, set register bit.0.14 to 1.

4.5.4 Far-End Loopback

When the far-end loopback test feature is enabled, incoming data from a link partner on the Copper interface to be transmitted back to the link partner on the Copper interface. To enable the loopback, set register bit.23.3 to 1.

4.5.5 QSGMII SerDes Loopback

There are 3 different types of loopback that occurs in the SerDes block:

- Input loopback: loops serial data from TDP/N onto RDP/N by writing 0 × 9022 to reg.18G
- Facility loopback: loops de-serialized data from TDP/N back to the serialized data onto RDP/N by writing 0 × 9022 to reg.18G
- Equipment loopback: similar to far-end loop but occurs in the SerDes block, by writing 0 × 9042 to reg.18G

5 Additional Information

For any additional information or questions regarding the devices mentioned in this document, contact your local sales representative.

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