
Atmel AVR1018: XMEGA B Schematic Checklist



Features

- Power supplies
- Reset circuit
- Clocks and crystal oscillators
- JTAG and PDI
- USB
- LCD

8-bit Atmel Microcontrollers

Application Note

1 Introduction

A good hardware design comes from a proper schematic. Since Atmel® AVR® XMEGA® B devices have a fair number of pins and functions, the schematic for these devices can be large and quite complex.

This application note describes a common checklist which should be used when starting and reviewing the schematics for an Atmel XMEGA B design.

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2 Power supplies

2.1 Power supply connections

All power supply pins of the device must be connected to the microcontroller supply.

Both VCC and AVCC must be connected to the same microcontroller positive supply, thus ensuring that they both share an identical supply profile. Likewise both ground pins must be connected to the same microcontroller ground reference supply.

Figure 2-1. Power supply schematic.

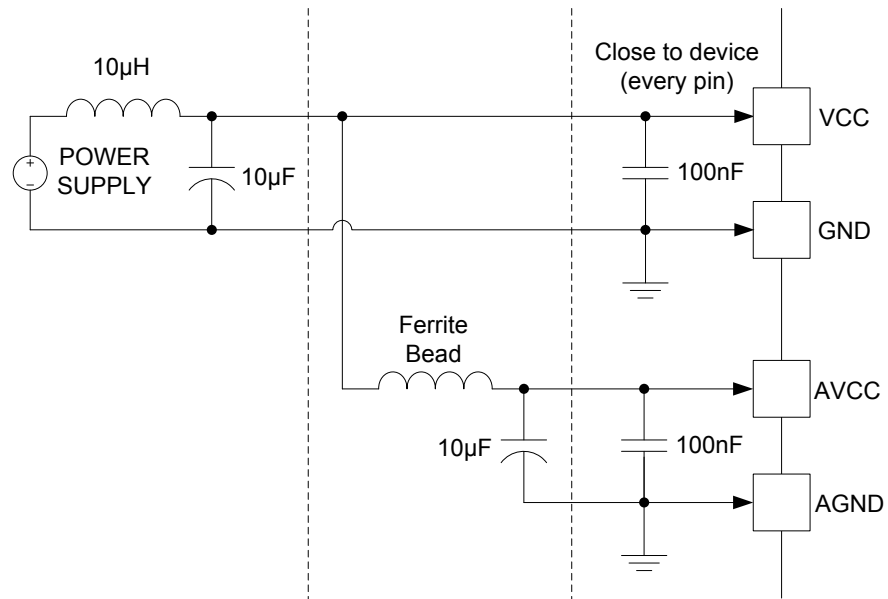


Table 2-1. Power supply checklist.

Signal name	Recommended pin connection	Description
VCC	1.6V to 3.6V Decoupling/filtering capacitors 100nF ⁽¹⁾⁽²⁾ and 10µF ⁽¹⁾ Decoupling/filtering inductor 10µH ⁽¹⁾⁽³⁾	Digital supply voltage
AVCC	1.6V to 3.6V Decoupling/filtering capacitors 100nF ⁽¹⁾⁽²⁾ and 10µF ⁽¹⁾ Ferrite bead ⁽⁴⁾ prevents the VCC noise interfering the AVCC	Analog supply voltage
GND		Ground

- Notes:
1. These values are given only as a typical example.
 2. Decoupling capacitor should be placed close to the device for each supply pin pair in the signal group, low ESR caps should be used for better decoupling.
 3. Wire wound inductor should be added between the external power and the VCC for power filtering.
 4. Ferrite bead has better filtering performance than the common inductor at high frequency. It can be added between VCC and AVCC for preventing digital noise from entering the analog power. The BEAD should provide enough impedance (For example 50Ω at 20MHz and 220Ω at 100MHz) for separating the digital power to the analog power.

2.2 External analog reference connections

The following schematic checklist is only recommended if the design is using the external analog reference. If the internal reference is used, the circuit is not necessary.

Figure 2-2. External VREF schematic with two references.

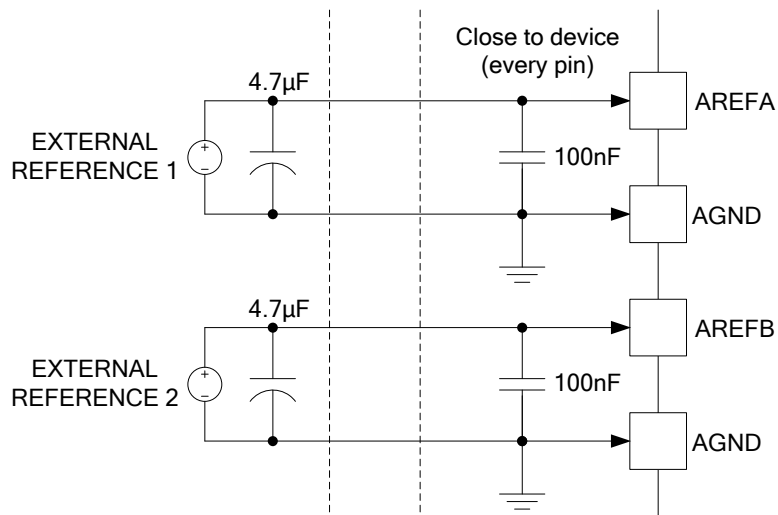


Figure 2-3. External VREF schematic with one reference.

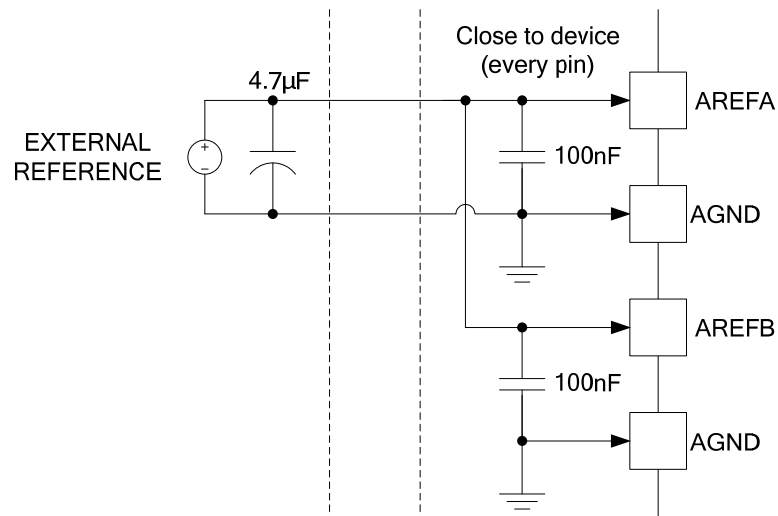


Table 2-2. External analog reference checklist.

Signal name	Recommended pin connection	Description
AREFA	1.0V to AVCC-0.6V for ADC Decoupling/filtering capacitors 100nF ⁽¹⁾⁽²⁾ and 4.7µF ⁽¹⁾	External reference from AREF pin on PORT A.
AREFB	1.0V to AVCC-0.6V for ADC Decoupling/filtering capacitors 100nF ⁽¹⁾⁽²⁾ and 4.7µF ⁽¹⁾	External reference from AREF pin on PORT B.
GND		Ground



Signal name	Recommended pin connection	Description
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- Notes:
1. These values are given only as a typical example.
 2. Decoupling capacitor should be placed close to the device for each AREF pin, low ESR caps should be used for better decoupling.

3 External reset circuit

The external reset circuit is connected to /RESET pin when the external reset function is used. If internal reset is used, the circuit is not necessary. The reset switch also can be removed, if the manual reset is not necessary.

Figure 3-1. External reset circuit example schematic.

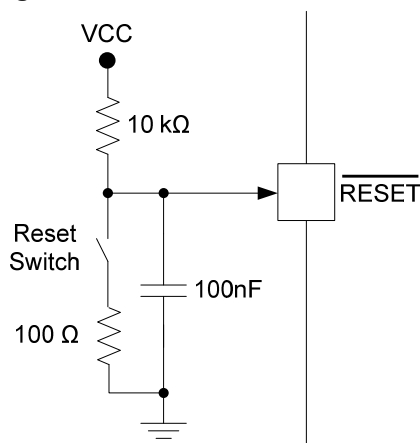


Table 3-1. Reset circuit checklist.

Signal name	Recommended pin connection	Description
<u>RESET</u>	Reset low level threshold voltage VCC = 2.7 - 3.6V: Below 0.45*VCC VCC = 1.6 - 2.7V: Below 0.42*VCC	Reset pin

- Notes:
1. The pull-up resistor makes sure that reset does not go low unintended. When the PDI programming and debugging is used, the reset line is used as clock. The reset pull-up should be 10kΩ or weaker, or be removed altogether.
 2. The pull-down resistor prevents from overvoltage on the RESET pin when the switch is pressed.
 3. Any reset capacitors should be removed if PDI programming and debugging is used. Other external reset sources should be disconnected.

4 Clocks and crystal oscillators

4.1 External clock source

Figure 4-1. External clock source example schematic.

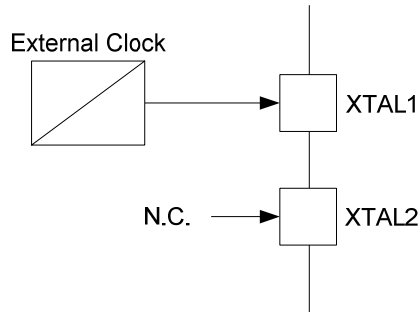


Table 4-1. External clock source checklist.

Signal name	Recommended pin connection	Description
XTAL1	XTAL1 is used as input for an external clock signal	Input for inverting Oscillator pin 1
XTAL2	Can be left unconnected or used as GPIO	

4.2 Crystal oscillator

Figure 4-2. Crystal oscillator example schematic.

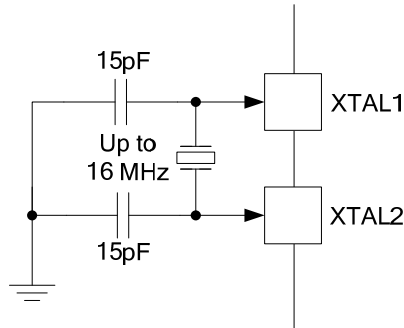


Table 4-2. Crystal oscillator checklist.

Signal name	Recommended pin connection	Description
XTAL1	Biasing capacitor 15pF ⁽¹⁾⁽²⁾	External crystal between 0.4MHz to 16MHz
XTAL2	Biasing capacitor 15pF ⁽¹⁾⁽²⁾	

- Notes:
1. These values are given only as a typical example. Please refer to the crystal datasheet to determine the capacitor value for the crystal used or refer to the application note "AVR1003: Using the Atmel XMEGA Clock System".
 2. Decoupling capacitor should be placed close to the device for each supply pin pair in the signal group.

4.3 External real time oscillator

The Low-frequency Crystal Oscillator is optimized for use with a 32.768kHz watch crystal. When selecting crystals, load capacitance and crystal's Equivalent Series

Resistance, ESR must be taken into consideration. Both values are specified by the crystal vendor.

Atmel XMEGA B oscillator is optimized for very low power consumption, and thus when selecting crystals, see [Table 4-3](#) for maximum ESR recommendations on 9pF and 12.5pF crystals.

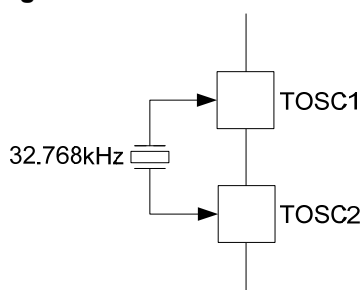
Table 4-3. Maximum ESR recommendation for 32.768kHz watch crystal.

Crystal CL (pF)	Max ESR [kΩ] ⁽¹⁾
9.0	65
12.5	30

Note: 1. Maximum ESR is typical value based on characterization.

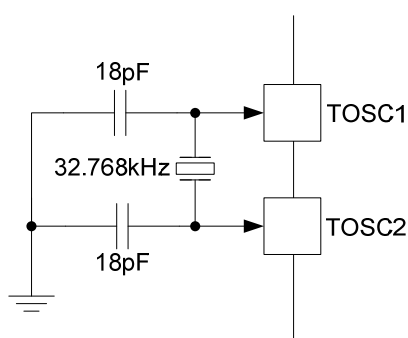
The Low-frequency Crystal Oscillator provides an internal load capacitance of typical 3.0pF. Crystals with recommended 3.0pF load capacitance can be without external capacitors as shown in [Table 4-3](#).

Figure 4-3. External real time oscillator without biasing capacitor.



Crystals specifying load capacitance (CL) higher than 3.0pF, require external capacitors applied as described in [Table 4-4](#).

Figure 4-4. External real time oscillator with biasing capacitor.



To find suitable load capacitance for a 32.768kHz crystal, please consult the crystal datasheet.

Table 4-4. External real time oscillator checklist.

Signal name	Recommended pin connection	Description
TOSC1	Biasing capacitor 18pF ⁽¹⁾⁽²⁾	LCD/Timer Oscillator pin 1
TOSC2	Biasing capacitor 18pF ⁽¹⁾⁽²⁾	LCD/Timer Oscillator pin 2



Signal name	Recommended pin connection	Description
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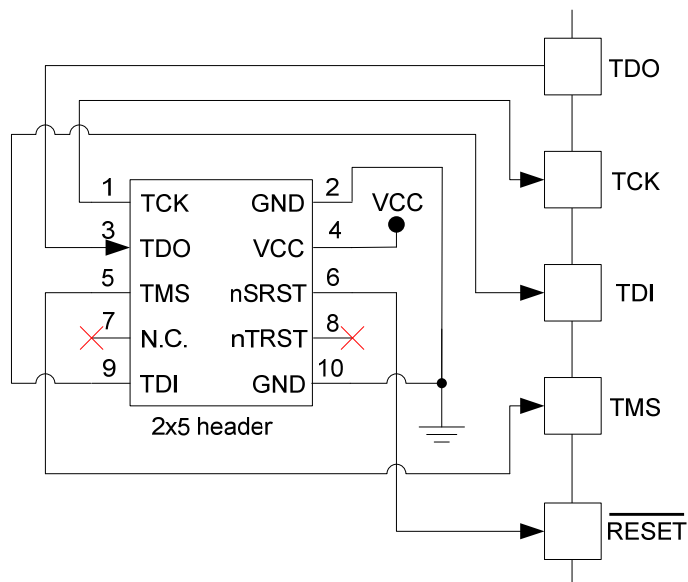
Notes: 1. These values are given only as a typical example. Please refer to the crystal datasheet to determine the capacitor value for the crystal used or refer to the application notes "AVR1003: Using the Atmel XMEGA Clock System" and "AVR4100: Selecting and testing 32kHz crystal oscillators for Atmel AVR microcontrollers".

2. Load capacitor should be placed close to the crystal, GND and device oscillator pins.

5 JTAG and PDI ports

5.1 JTAG port interface

Figure 5-1. Atmel JTAG port interface example schematic.



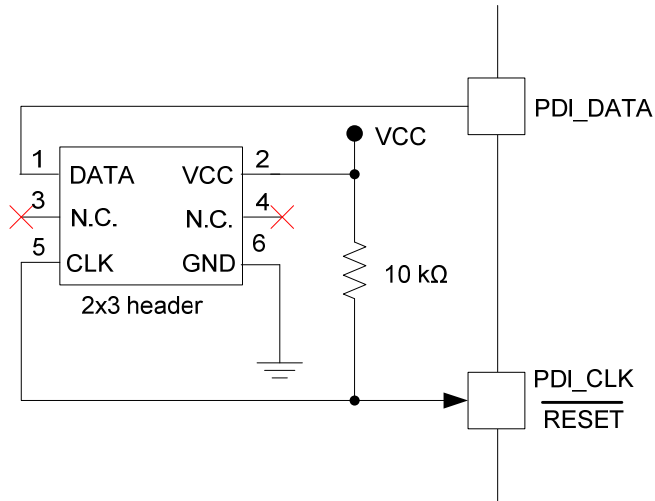
The schematic of [Table 5-1](#) corresponds to the standard Atmel tools JTAG header (For example Atmel JTAGICE3, AVRONE!, ...).

Table 5-1. JTAG port interface checklist.

Signal name	Recommended pin connection	Description
TDO		Test data output, driven on falling TCK
TCK		Test clock, fully asynchronous to system clock frequency
TDI		Test data input, sampled on rising TCK
TMS		Test mode select, sampled on rising TCK
$\overline{\text{RESET}}$		Device external reset line

5.2 PDI port interface

Figure 5-2. PDI port interface example schematic.



The schematic of [Table 5-2](#) corresponds to the standard Atmel tools PDI header (For example Atmel JTAGICE3, AVRONE!, ...).

Table 5-2. PDI port interface checklist.

Signal name	Recommended pin connection	Description
PDI_CLK	This pull-up resistor makes sure that reset does not go low unintended. When the PDI programming and debugging is used, the reset line is used as clock. The reset pull-up should be 10kΩ or weaker, or be removed altogether. Any reset capacitors should be removed if PDI programming and debugging is used. Other external reset sources should be disconnected.	PDI clock input / Reset pin
PDI_DATA		PDI_DATA: PDI data input / output

6 USB interface

The impedance of the USB differential data line pair is 90Ω to each other and 45Ω to ground. The termination of the line is included within the Atmel XMEGA B device as serial resistors. To ensure proper signal integrity, the two D+/D- signals must be closely routed on the PCB (Refer to “AVR1017: XMEGA - USB Hardware Design Recommendations” application note).

Figure 6-1. Low cost USB interface example schematic.

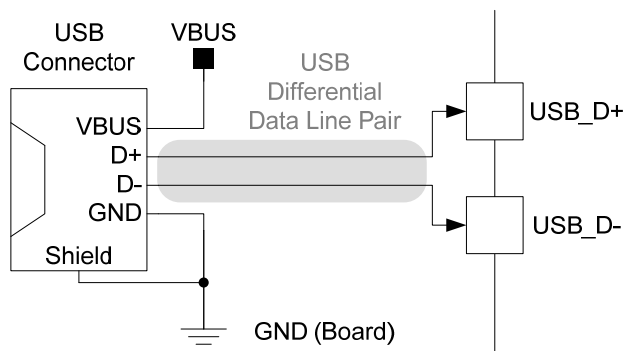


Figure 6-2. Protected USB interface example schematic.

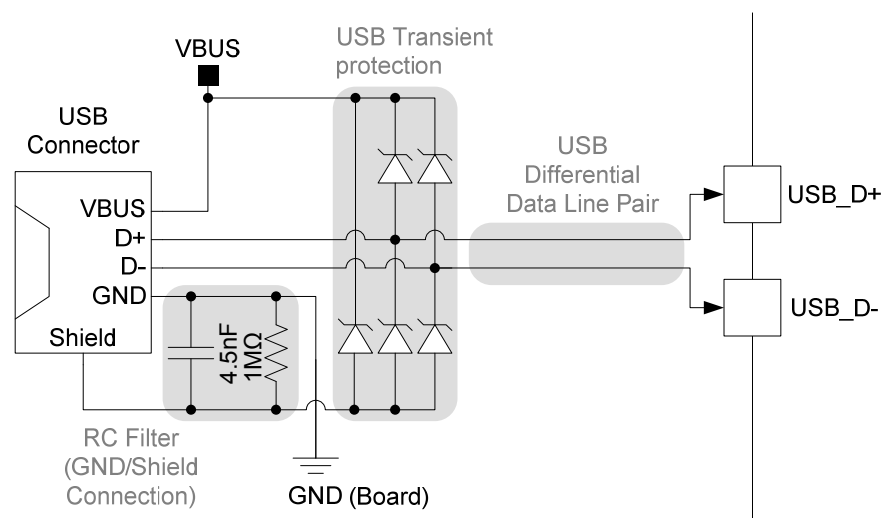


Table 6-1. USB interface checklist.

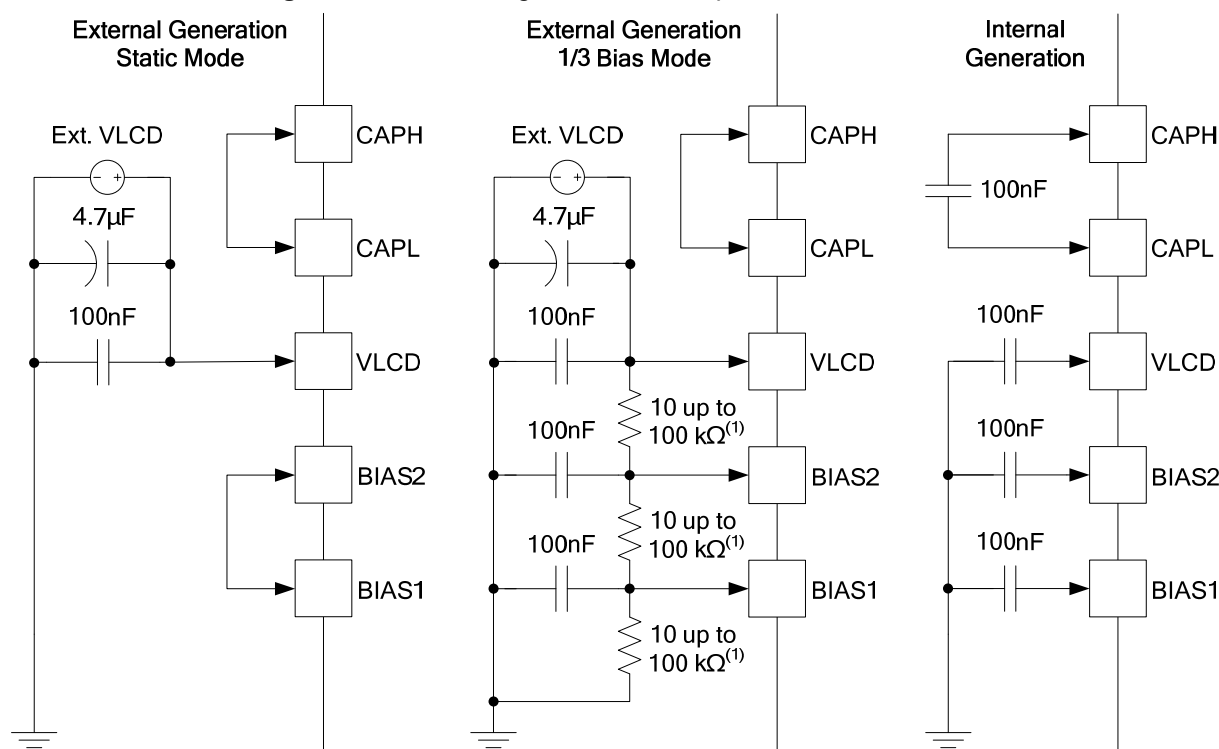
Signal name	Recommended pin connection	Description
D+	The impedance of the pair should be matched on the PCB to minimize reflections	USB full speed / low speed positive data upstream pin
D-	- USB differential tracks should be routed with the same characteristics (length, width, number of vias, etc.) - Signals should be routed as parallel as possible, with a minimum number of angles and vias	USB full speed / low speed negative data upstream pin

7 LCD interface

7.1 Bias generation

Voltages for on-chip LCD buffers can be generated by the device itself or externally.

Figure 7-1. LCD bias generation example schematic.



NOTE

Bias generation can be provided by other sources of voltage than by a division resistor.

Table 7-1. LCD bias interface checklist.

Signal name	Recommended pin connection	Description
CAPH	- Internal bias generation: 100nF between CAPH and CAPL close to device - External bias generation: CAPH/CAPL connected together	High end of flying capacitor
CAPL		Low end of flying capacitor
VLCD	Internal bias generation: 100nF to GND close to device	LCD voltage multiplier output
	External bias generation: 100nF for decoupling close to device	LCD voltage input
BIAS2	- Internal bias generation: 100nF to GND close to device - External 1/3 bias generation: 100nF for decoupling close to device - External static generation: BIAS1/BIAS2 connected together	LCD intermediate voltage 2 output (VLCD * 2/3)
BIAS1		LCD intermediate voltage 1 output (VLCD * 1/3)

7.2 Terminal signals

No external component is required on segment and common terminal buses. To help the board routing, a segment or/and common terminal buses swapping can be enabled (c.f. SEGSWP and COMSWP bit in LCD.CTRLA register).

Table 7-2. LCD terminal interface checklist.

Signal name	Recommended pin connection	Description
COMn	Routed as bus of analog signals	LCD common terminal output
SEGn		LCD segment terminal output



8 Suggested reading

8.1 Datasheet and manual

The datasheet and the manual contain block diagrams of the peripherals and details about implementing firmware for the device. The datasheet and the manual are available on <http://www.atmel.com/AVR> in the Datasheets & Manuals section.

8.2 Evaluation kit schematic

The evaluation kit Atmel XMEGA-B1 XPLAINED contains the full schematic for the board; it can be used as a reference design. The schematic is available on <http://www.atmel.com/AVR> in the Tools & Software section.

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Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: (+1)(408) 441-0311
Fax: (+1)(408) 487-2600
www.atmel.com

Atmel Asia Limited
Unit 01-5 & 16, 19F
BEA Tower, Millennium City 5
418 Kwun Tong Road
Kwun Tong, Kowloon
HONG KONG
Tel: (+852) 2245-6100
Fax: (+852) 2722-1369

Atmel Munich GmbH
Business Campus
Parking 4
D-85748 Garching b. Munich
GERMANY
Tel: (+49) 89-31970-0
Fax: (+49) 89-3194621

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chou-ku, Tokyo 104-0033
JAPAN
Tel: (+81) 3523-3551
Fax: (+81) 3523-7581

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