Functional Safety Package Errata

SAFETY-PKG-M2S-M2GL-F/NL

Introduction

This functional safety package errata document is an early notification of issues along with a detailed description of the issues, the condition of occurrence, and the workaround. Microchip continues to work on updating the Functional Safety User Guide with these issues and further details on workarounds.

Errata Description

Nine issues have been identified and can affect the functional safety designs when using the IEC-61508 certified Libero® SoC 11.8 SP4 and CoreGPIO. We are providing this document as an early notification of these issues and continue to work on updating the Functional Safety User Guide with these issues and further details on workarounds.

Microchip Parts Affected

Customers using the SmartFusion® 2 and IGLOO® 2 family of devices that uses the SAFETY-PKG-M2S-M2GL-F or SAFETY-PKG-M2S-M2GL-NL functional safety package.

Impacts to Data Sheet

Not applicable.

Change Impact

Customers utilizing any of the outlined configurations to design their high-reliability applications need to evaluate the use and impact to their functional safety designs.

Change Implementation Status

The status is in progress. The changes to the functional safety package including the Functional Safety Manual will be completed and provided to the customers.

Method to Identify Change

The Functional Safety User Guide will be updated to reflect the information provided and any identified workarounds for these issues.

Qualification Plan

Not applicable.

Workaround

The workaround for identified issues will be available in Revision B of the Functional Safety User Guide.

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1. Details of Identified Issues

Nine issues have been identified and can affect the functional safety designs when using the IEC-61508 certified Libero SoC 11.8 SP4 and CoreGPIO.

1.1 SmartTime: Over-Optimistic Clock-to-Out Delay for LSRAM

Problem Description

There is an optimistic clock-to-out delay when using the SmartFusion 2/IGLOO 2 LSRAM under a specific configuration, which might give unreported silicon violations.

Condition of Occurrence

Write Feed-Through Mode is on (WMODE = 1) and the Write enable is low (WEN = 0).

1.2 I/O State during Programming is not Invalidating Generate Bitstream

Problem Description

I/O State During Programming settings are not propagated to the programming file and “Generate Bitstream” state is not invalidated.

Condition of Occurrence

I/O State during programming is not set according to the settings that the customer set in the “I/O State During Programming”.

1.3 Optimistic Local Clock Network Delay when Local Clock RGB Area Coverage is too Wide

Problem Description

Designs using clocks, routed towards the global network through an RCLKINT macro, may require the cascading of multiple Row Global Buffers (RGBs) if the loads on that clock, cover a large area in the device. In this case, the clock skew between distant FFs might be larger than the span of what is expected in a local area. In extreme cases (large device, short data path, or distant FFs), a skew-induced timing violation can exist that is undetected by the tools.

Condition of Occurrence

The exposure to this issue is limited to SmartFusion 2 and IGLOO 2 designs with local clock nets, using only the largest devices such as, M2S150 and M2GL150 and their variants.

1.4 DAT Bitstream File is Incorrect when using Programming Recovery

Problem Description

If the Libero design has Programming Recovery enabled in the Configure Programming options tool and uses Enable Custom Security Options in Configure Security tool, the DAT bitstream file generated will be incorrect and will not erase the security completely on the device when running the Erase action.

Condition of Occurrence

SmartFusion 2 and IGLOO 2 designs with Programming Recovery enabled in the Configure Programming options tool and uses Enable Custom Security Options in Configure Security tool.

1.5 Inconsistent SmartTime Behavior for DDR

Problem Description

Designs which applied multiple, duplicate, or overlapping constraints could face a scenario where SmartTime did not apply the last valid constraint entered, but instead applied a combination of the duplicate constraints.

Condition of Occurrence

Designs with multiple, duplicate, or overlapping constraints on DDR inputs applied to the same pin.

1.6 Clock Generation Value is 0 ns for Muxed Clocks

Problem Description

Timing model of CCC does not account for CCC CLK1 input resulting in clock generation value of 0 ns for muxed clocks.

Condition of Occurrence

SmartFusion 2 and IGLOO 2 designs where CCC CLK1 input is used in generated clock constraints.

1.7 CCC SmartTime vs BA Simulation: Delay from Input PAD to CCC GL has a Mismatch

Problem Description

For designs containing CCC with internal feedback, incorrect port name is written in the SDF file due to pin swapping. This results in a delay mismatch between SmartTime vs back-annotated simulation.

Condition of Occurrence

SmartFusion 2 and IGLOO 2 designs containing CCC with internal feedback.

1.8 Mismatch between SmartTime and BA Simulation on Outpad Delay

Problem Description

SmartTime skips IOTRI_OB_EB and IOOUTFF_BYPASS instances in timing analysis yet back-annotated netlist still contains these two instances while back-annotated sdf file does not have them. This will cause back-annotated simulation to use default delays on these two instances resulting in a delay discrepancy between back-annotated simulation and SmartTime.

Condition of Occurrence

SmartFusion 2 and IGLOO 2 designs containing Output pads.

1.9 Simulation Issue Found with CoreGPIO v3.1 when VHDL HDL is Used

Problem Description

The APB slave address (PADDR) of CoreGPIO is not qualified with the PSEL signal. Due to this issue, any APB slave address outside the permissible range of CoreGPIO results in a simulation error. The issue in the IP does not have an impact in hardware validation.

Condition of Occurrence

The issue is observed only when HDL generated language option is selected as VHDL. The issue is observed if the APB slave address falls outside the permissible range of CoreGPIO. The permissible range is based on the CoreGPIO configuration.

2. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
A	11/2023	Initial Revision

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