VESA Display Stream Compression Encoder IP v1.0 User Guide

Introduction

Display Stream Compression (DSC) is a visually lossless video compression targeted for display devices. As there is demand for higher video resolutions and higher frame rates, the data bandwidth required to transmit the video keeps increasing. To transmit high video resolutions such as 4K and 8K, the source, transmission path, that is the display cable, and the display should support higher data rates. These high data rates increase the cost of the source, cable and the display. DSC is used to reduce the data rate required to transmit high resolution videos and there by reducing the cost. DSC was first introduced by Video Electronics Standards Association (VESA) in 2014. DSC compression is supported by the latest versions of the popularly used protocols such as HDMI, Display port, and MIPI DSI.

DSC implements compression by combining a group of pixels in a horizontal line. The compression algorithm uses several stages such as prediction, quantization, entropy encoding, and rate control. There are two types of algorithms for prediction, which are Modified Median Adaptive Filter (MMAP) and Mid-Point Prediction (MPP). The predicted data is quantized based on the rate control to achieve constant bandwidth at the output. The quantized data is then passed to the Variable Length Coding (VLC) that minimizes the bits used to represent the quantized output. These compression stages are implemented for Y, Cb, and Cr component and the outputs of these stages are combined at the end using a substream multiplexer.

DSC supports splitting a video frame into multiple slices horizontally with equal size. The slicing of a frame allows parallel processing of slices to handle high resolution video frames. The DSC IP supports two slices and uses MMAP and MPP predictions.

Features

DSC has the following features:

- VESA DSC 1.2a Spec
- Implements Compression on YCbCr 444 Video Format
- Supports 12-bits Per Pixel (12 bpp) and 8-bits Per Component
- Standalone Operation, CPU, or Processor Assistance not Required
- Supports Compression for 432x240, 648x480, 960x540, 1296x720, and 1920x1080 Resolutions at 60 Frames Per Second (fps)
- Supports Two Slices

Supported Families

DSC supports the following family of products:

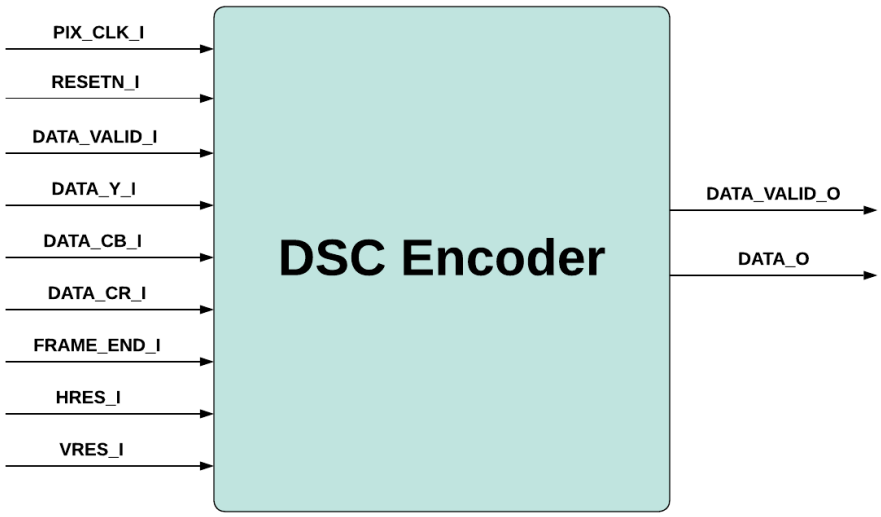
- PolarFire® SoC FPGA
- PolarFire FPGA

Table of Contents

1. Hardware Implementation

The following figure shows the DSC IP block diagram.

Figure 1-1. DSC Encoder IP Block Diagram



1.1 Inputs and outputs

The following table lists the input and output ports of DSC IP.

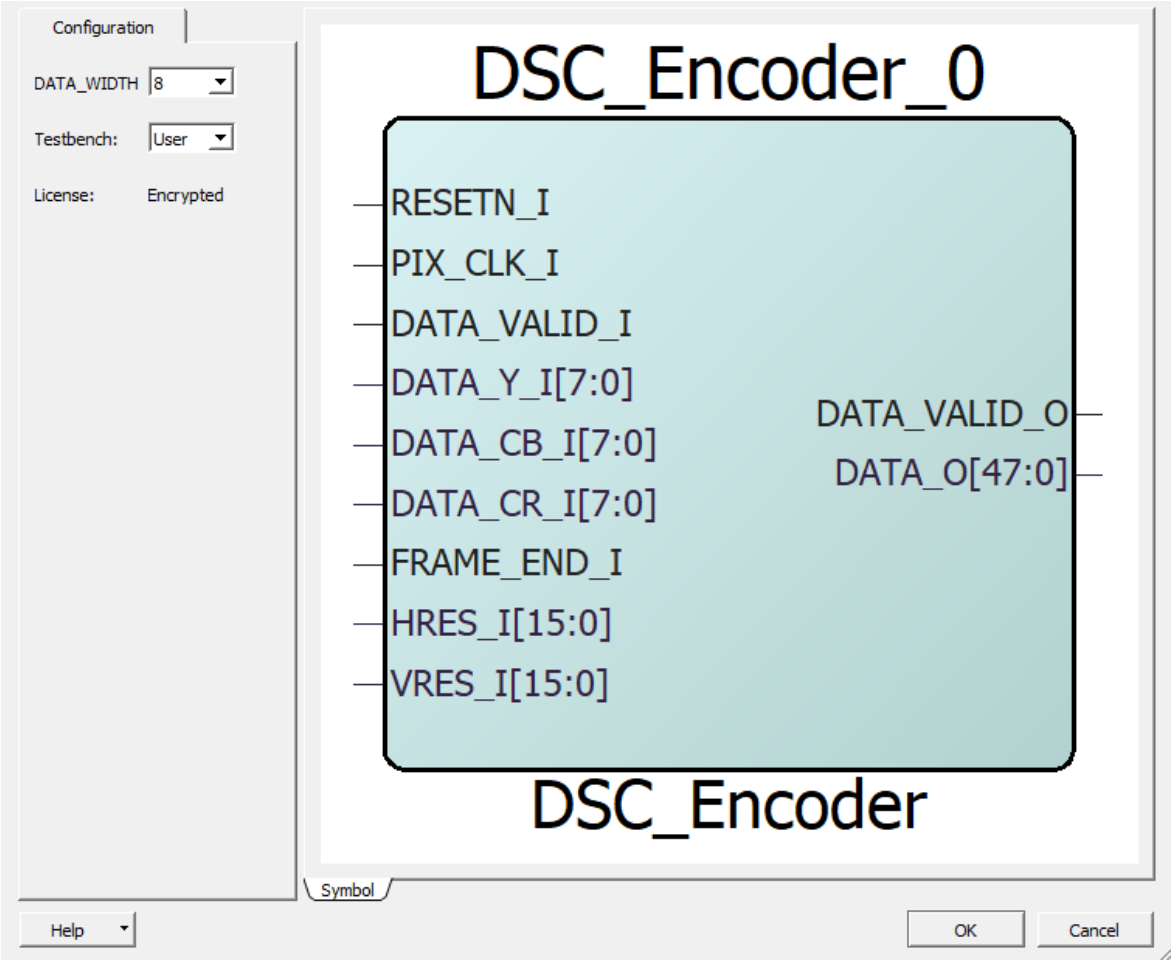
Table 1-1. Input and Output Ports of DSC IP

Signal Name	Direction	Width	Description
PIX_CLK_I	Input	1	Input clock with which incoming pixels are sampled
RESETN_I	Input	1	Active-low asynchronous reset signal to the design
DATA_VALID_I	Input	1	Input pixel data valid signal
DATA_Y_I	Input	8	8-bit Luma pixel input in 444 format
DATA_CB_I	Input	8	8-bit Cb pixel input in 444 format
DATA_CR_I	Input	8	8-bit Cr pixel input in 444 format
FRAME_END_I	Input	1	End of frame indication
HRES_I	Input	16	Horizontal resolution of input image
VRES_I	Input	16	Vertical resolution of input image
DATA_VALID_O	Output	1	Signal denoting compression data is valid
DATA_O	Output	48	DSC encoded data bitstream output

1.2 Configuration Parameters

The following figure shows the DSC Encoder IP configuration parameters.

Figure 1-2. DSC Encoder IP Configurator



1.3 Hardware Implementation of DSC IP

This section describes the different internal modules of the DSC Encoder IP. The data input to the IP must be in the form of a raster scan image in the YCbCr 444 format.

The following figure shows the DSC Encoder IP block diagram that divides the input image into two slices. The width of each slice is half of the input image width and the slice height is same as the input image height.

Figure 1-3. DSC Encoder IP Block Diagram Slice 1

The following figure shows the DSC Encoder block diagram for each slice.

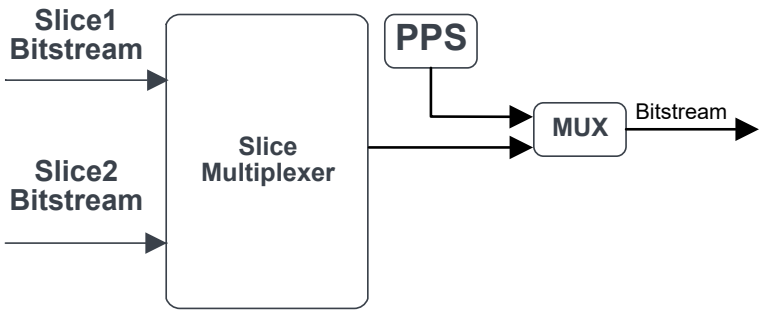
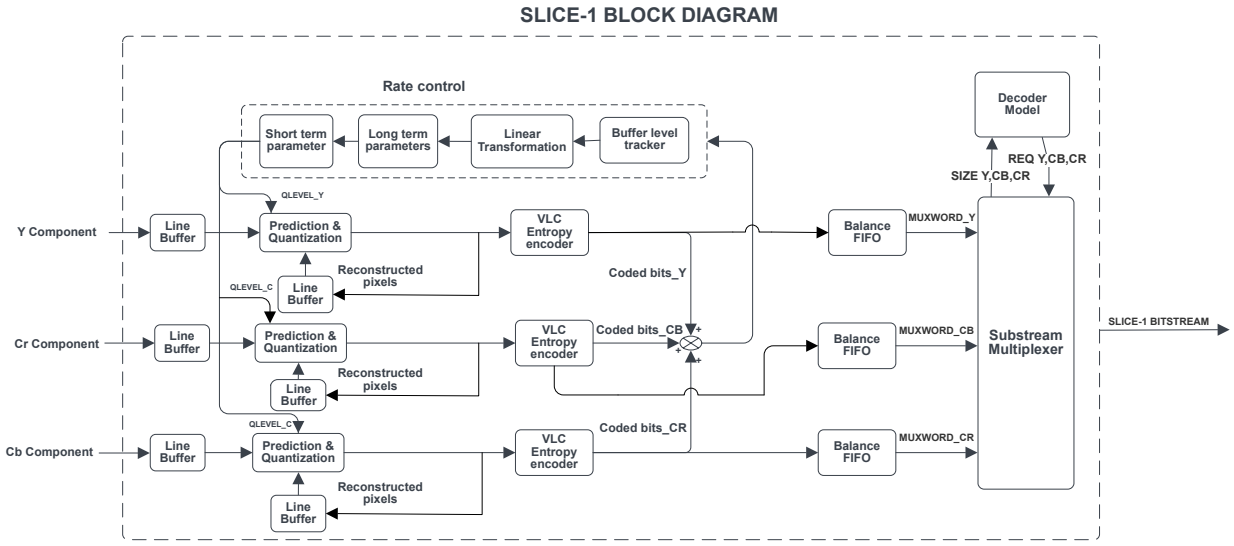


Figure 1-4. DSC Encoder Block Diagram Slice 2



1.3.1 Prediction and Quantization

Each group, consisting of three consecutive pixels, is predicted by using the MMAP and MPP algorithms. Predicted values are subtracted from the original pixel values, and the resulting residual pixels are quantized. In addition, reconstruction step is performed in the encoder wherein, the inverse quantized residuals are added to the predicted sample to ensure that both encoder and decoder have the same reference pixels.

MMAP algorithm uses the current group's pixels, the previous line's adjacent pixels, and the reconstructed pixel immediately to the left of the group. This is the default prediction method.

The MPP predictor is a value at or near the midpoint of the range. The predictor depends on the rightmost reconstructed sample value of the previous group.

1.3.2 VLC Entropy Encoder

The size of each residual is predicted using the previous residual size and changing the Quantization Parameter (QP). Variable length encoding effectively compresses the residual data.

1.3.3 Rate Control

Rate control block calculates the master Quantization Parameter (masterQP) to be used for prediction and VLC to ensure that the rate buffer neither underflows nor overflows. masterQP value is not transmitted along the bitstream, and the same rate control algorithm is imitated in the decoder. The RC algorithm is designed to optimize subjective

picture quality by way of its QP decisions. Lower QP on flat areas of the image and Higher QP on busy areas of the image ensures you to maintain constant quality for all the pixels.

1.3.4 Decoder Model

Decoder is an idealized theoretical actual decoder model. Decoder model dictates how the substeams Y, Cb, and Cr are multiplexed. The Balance FIFOs ensure that the multiplexer has at least one mux word’s worth of data whenever the multiplexer receives a request signal from the decoder model.

1.3.5 Substream Multiplexer

The substream multiplexer multiplexes the Y, CB, and Cr components into a single slice of data. Each muxword has 48-bit data. Muxwords are inserted in the bitstream depending on the size of their syntax elements.

1.3.6 Slice Multiplexer

Each picture is divided into two equal slices. Each slice is independently decoded without referencing other slices. Two slices are merged in the bitstream by the slice multiplexing process.

2. Testbench

Testbench is provided to check the functionality of the DSC IP.

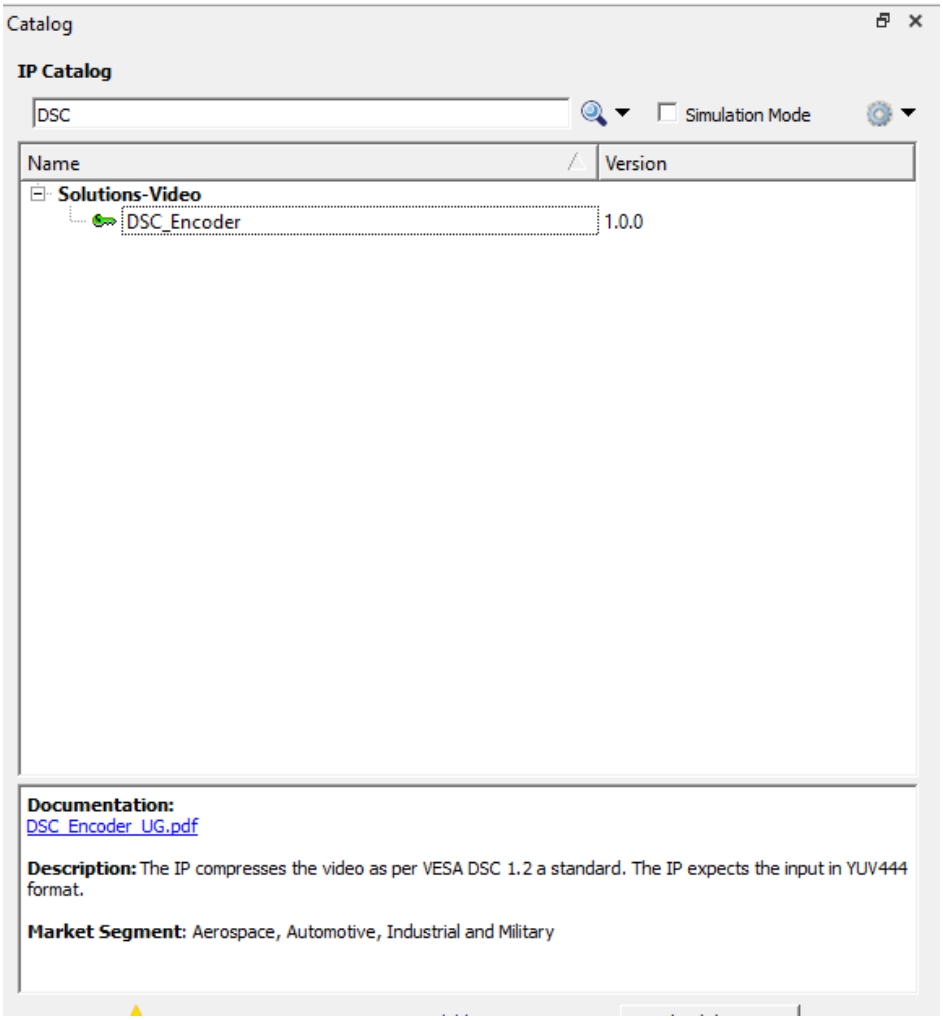
2.1 Simulation

The simulation uses a 432x240 image in YCbCr444 format represented by three files, each for Y, Cb, and Cr as input and generates a `.txt` file format that contains one frame.

To simulate the core using the testbench, perform the following steps:

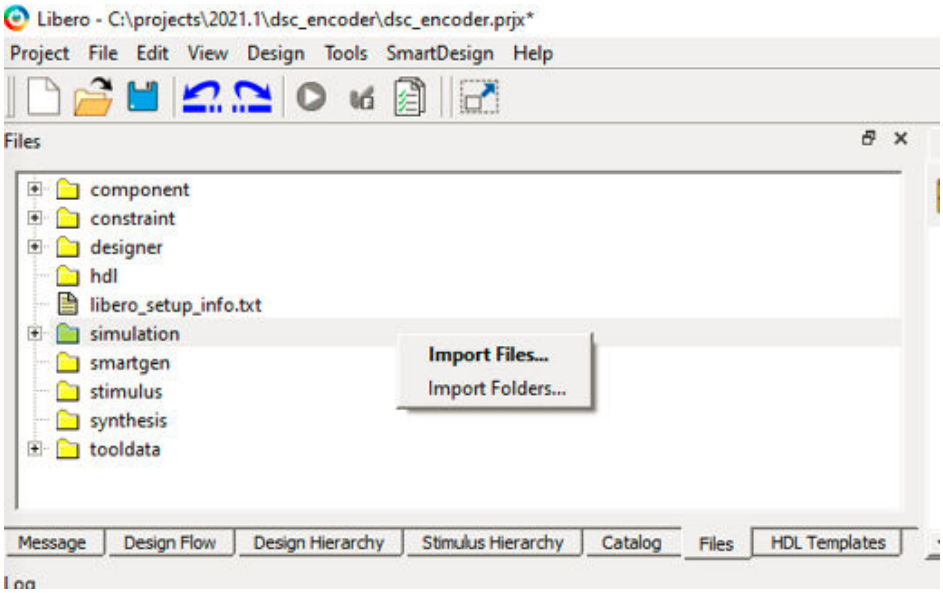
1. Go to Libero® SoC **Catalog** tab, expand **Solutions-Video**, double-click **DSC_Encoder**, and then click **OK**.
   Note: If you do not see the **Catalog** tab, navigate to **View > Windows** menu and click **Catalog** to make it visible.

   Figure 2-1. DSC Encoder IP Core in Libero SoC Catalog



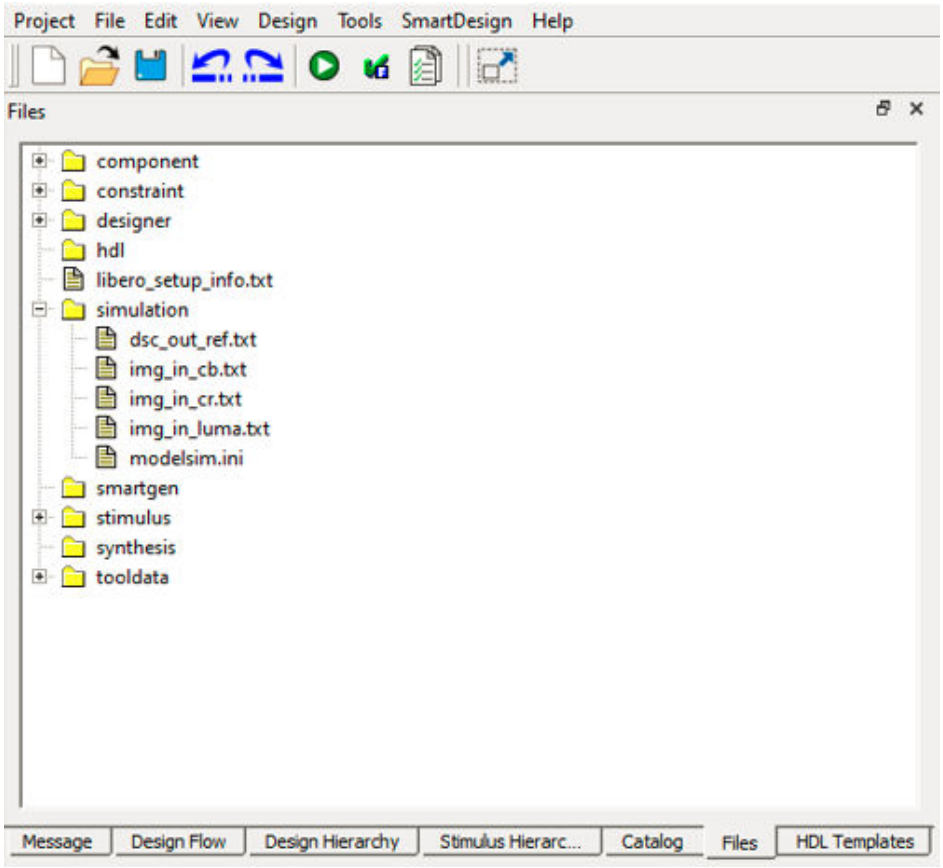
2. Go to the **Files** tab, right-click **simulation**, and then click **Import Files**.

Figure 2-2. Import Files



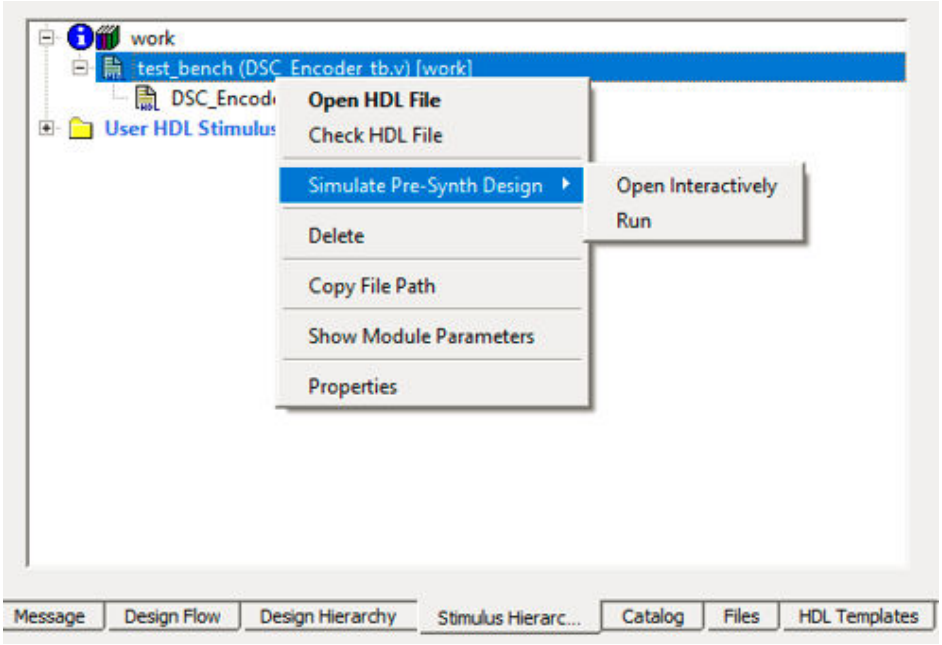
3. Import the `img_in_luma.txt`, `img_in_cb.txt`, `img_in_cr.txt`, and `DSC_out_ref.txt` files from the following path: `..\<Project_name>\component\Microchip\SolutionCore\ DSC_Encoder\<DSC IP version>\Stimulus`.
   The imported file is listed in the **simulation** folder as shown in the following figure.

Figure 2-3. Imported Files



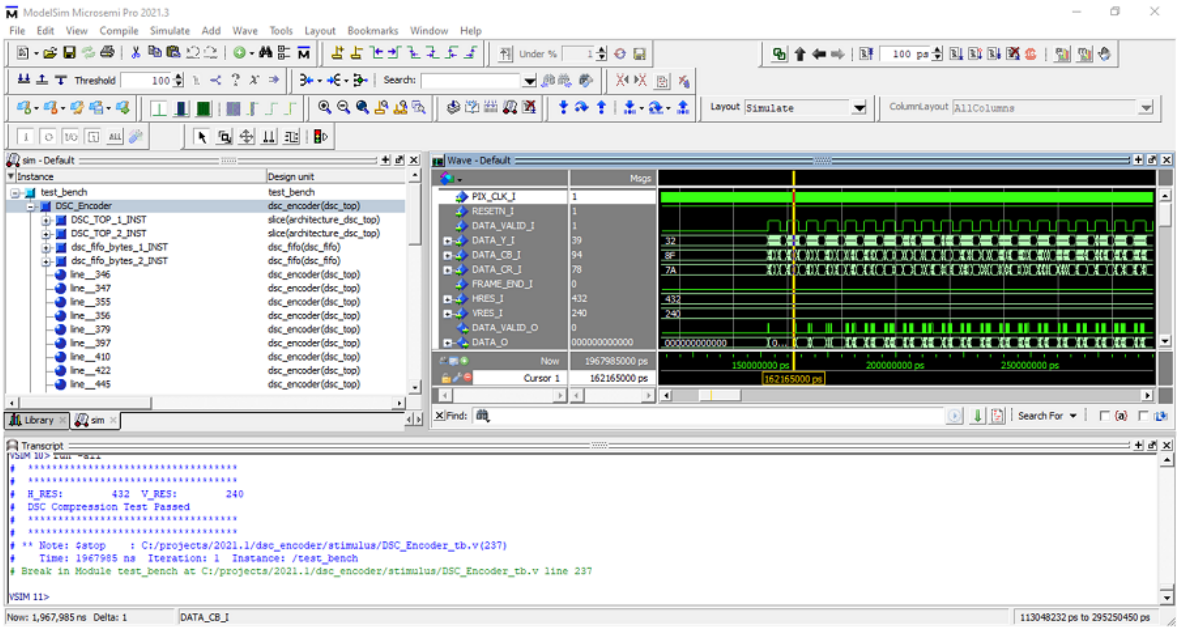
4. Go to Libero SoC **Stimulus Hierarchy** tab, select the testbench (`DSC_Encoder_tb. v`), right-click and then click **Simulate Pre-Synth Design > Open Interactively**. The IP is simulated for one frame.
   Note: If you do not see the **Stimulus Hierarchy** tab, navigate to **View > Windows** menu, and then click **Stimulus Hierarchy** to make it visible.

Figure 2-4. Simulating the Pre-Synthesis Design



ModelSim opens with the testbench file as shown in the following figure.

Figure 2-5. ModelSim Simulation Window



Note: If the simulation is interrupted due to the runtime limit specified in the `DO` file, use the `run -all` command to complete the simulation.

3. License

VESA DSC IP is provided only in encrypted form.

Encrypted RTL source code is license locked, which needs to be purchased separately. You can perform simulation, synthesis, layout, and program the Field Programmable Gate Array (FPGA) silicon using the Libero design suite.

Evaluation license is provided for free to explore the VESA DSC IP features. The evaluation license expires after an hour’s use on the hardware.

4. Installation Instructions

DSC IP core must be installed to the IP Catalog of the Libero SoC software. This is done automatically through the IP Catalog update function in the Libero SoC software, or the IP core can be manually downloaded from the catalog. Once the IP core is installed in the Libero SoC software IP Catalog, the core can be configured, generated, and instantiated within the SmartDesign tool for inclusion in the Libero projects list.

5. Resource Utilization

The following table lists the resource utilization of a sample DSC IP design made for PolarFire FPGA (MPF300TS-1FCG1152I package) and generates compressed data by using 4:4:4 sampling of input data.

Table 5-1. Resource Utilization

Resource	Usage
DFFs	11132
4LUT	21988
LSRAM	48
uSRAM	0
Math Blocks	2
Interface DFFs	1800
Interface 4LUT	1800

6. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

Table 6-1. Revision History

Revision	Date	Description
B	09/2022	Updated the 3. License section
A	09/2022	Initial release

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