
SmartFusion2

FIFO Controller without Memory Configuration



Table of Contents

Introduction	3
1 Functionality	4
Write Depth/Width and Read Depth/Width	4
Single Clock (CLK) or Independent Write and Read Clocks (WCLOCK, RCLOCK)	4
Write Enable (WE)	4
Read Enable (RE)	4
Allow Write when FIFO is Full	4
Allow read when FIFO is Empty	4
Asynchronous Reset (RESET)	4
Generating Flags in the FIFO Controller without Memory	5
2 Area and Speed in the FIFO Controller	6
3 Timing Diagrams	7
Write Operation	7
Read Operation	7
Operations with a Variable Aspect Ratio	8
4 Port Description	9
A Product Support	10
Customer Service	10
Customer Technical Support Center	10
Technical Support	10
Website	10
Contacting the Customer Technical Support Center	10
ITAR Technical Support	11

Introduction

The FIFO Controller without Memory generates only the FIFO controller logic. This core is intended to be used along with either a Two-Port Large SRAM or a Micro SRAM.

The FIFO Controller without Memory is independent of depth and width cascading of RAM Blocks.

The FIFO Controller without Memory has single-RAM-location granularity with the empty / full flags.

It supports many more optional status ports for increased visibility and usability. These optional ports are described in more detail in the sections below.

In this document, we describe how you can configure a FIFO Controller without Memory instance and define how the signals are connected.

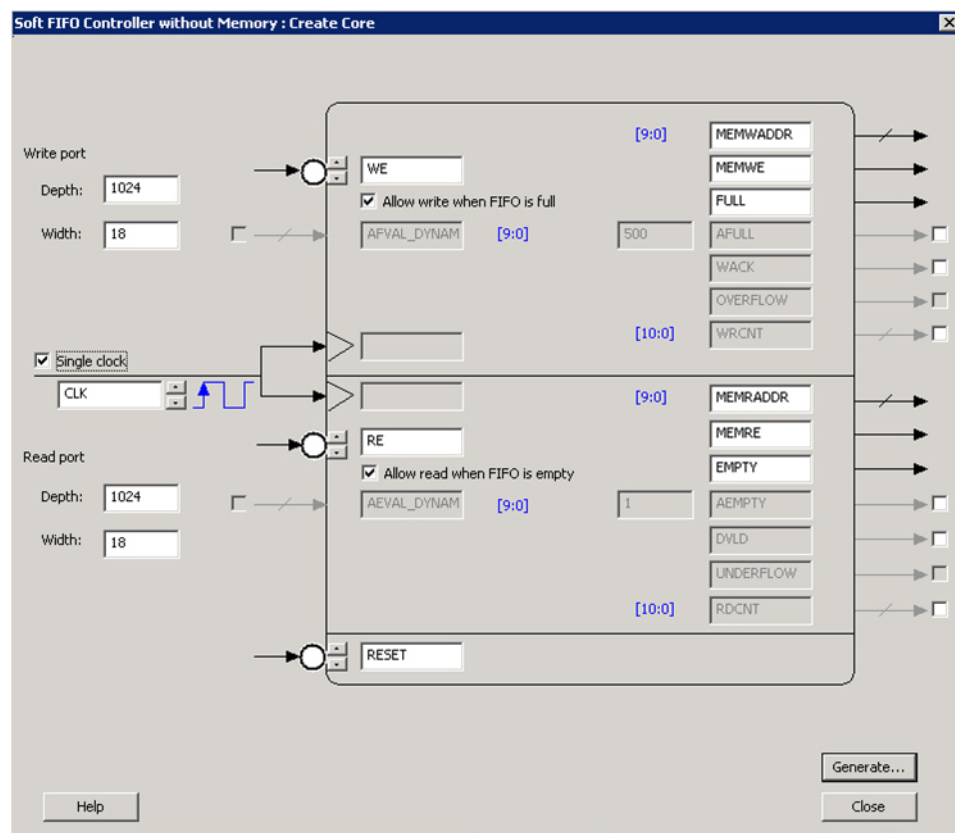


Figure 1 • FIFO Controller without Memory Configurator

1 – Functionality

Write Depth/Width and Read Depth/Width

The depth range for each port is 1-99999. The width range for each port is 1-999.

The two ports can be independently configured for any depth and width. (Write Depth * Write Width) must equal (Read Depth * Read Width).

Single Clock (CLK) or Independent Write and Read Clocks (WCLOCK, RCLOCK)

The FIFO Controller without Memory offers a dual- or single-clock design. The dual clock design allows independent read and write clock domains. Operations in the read domain are synchronous to the read clock, and operations in the write domain are synchronous to the write clock.

Selecting the single clock option results in a much simpler, smaller and faster design.

The default configuration for FIFO Controller without Memory is a Single clock (CLK) to drive WCLOCK and RCLOCK with the same clock. Uncheck the Single clock checkbox to drive independent clocks (one each for Write and Read).

Clock Polarity - Click the up or down arrows to change the active edge of your Write and Read clocks. If you use a single clock you can select on only CLK; if you use independent clocks you can select the polarity of both the WCLOCK and RCLOCK.

Write Enable (WE)

WE controls when the write data is written to the Write Address (MEMWADDR) of the RAM at the clock edge.

WE Polarity - Click the up or down arrows to change the active edge of WE signal.

Read Enable (RE)

Asserting the RE causes the RAM data at the read address (MEMRADDR) location to be read out.

RE Polarity - Click the up or down arrows to change the active edge of RE signal.

Allow Write when FIFO is Full

Select this checkbox to enable the FIFO to continue write when it is full. Your existing FIFO value will be overwritten.

Allow read when FIFO is Empty

Select this checkbox to enable the FIFO to continue to read when it is empty.

Asynchronous Reset (RESET)

Asserting the active-low RESET signal resets the FIFO Controller without Memory.

RESET Polarity - Click the up or down arrows to change the active edge of RESET signal.

Generating Flags in the FIFO Controller without Memory

Flags in the FIFO Controller without Memory are generated as follows:

- The Full, Empty, Almost Full, and Almost Empty flags are registered outputs of this module.
- The Almost Full and Almost Empty flags are optional ports; you can set the threshold values statically or dynamically.
 - To set a static value for the threshold: deselect the checkbox next to the AFVAL or AEVAL port; this disables the port(s) and enables the text control box next to the AFULL / AEMPTY port(s). Enter your desired static threshold into this field.
 - To set a dynamic value for the threshold, select the checkbox(es) next to the AFVAL or AEVAL port, this enables core generation with one or both buses. You can then dynamically input your desired threshold values.
- The Full flag is asserted on the same clock that the data that fills the FIFO is written.
- The Empty flag is asserted on the same clock that the last data is read out of the FIFO.
- The Almost Full flag is asserted on the same clock on which the threshold has been reached.
- The Almost Empty flag is asserted on the same clock on which the threshold has been reached. For example, if you specify an almost empty threshold of 10, the flag asserts on the same read clock that causes the FIFO to contain 10 elements.

2 – Area and Speed in the FIFO Controller

The size and operating frequency of the FIFO Controller is dependent upon the configuration and optional features that are enabled; note that:

- A single clock design will be smaller and faster; this is because the synchronizers and gray encoder/decoders are not required.
- Port depths that are not a power of 2 will generate a larger and slower design. The reason is that logic optimization occurs for power-of-2 depths. Thus, if you need a 66 x 8 FIFO, it may be more advantageous to select a FIFO depth of 64 or 128 if area and/or speed are concerns.

3 – Timing Diagrams

Write Operation

During a write operation when the WE signal is asserted the FIFO stores the value on the DATA bus into the memory. The WACK signal is asserted each time a successful write operation occurs on the FIFO. If the FIFO fills up, the FULL flag is asserted indicating that no more data can be written. The AFULL flag is asserted when the number of elements in the FIFO equals the threshold amount.

If a write operation is attempted while the FIFO is full, the OVERFLOW signal is asserted on the next clock cycle, indicating that an error has occurred. The OVERFLOW signal is asserted for each write operation that fails. A sample timing diagram of a FIFO with depth configuration of 4, almost full value set to 3, and rising clock edge is shown in [Figure 3-1](#).

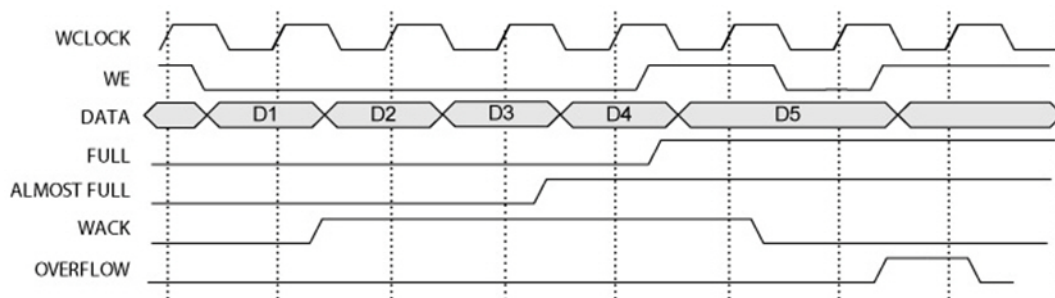


Figure 3-1 • Write Operation and Flags

Read Operation

During a read operation when the RE signal is asserted the FIFO reads a data value onto the Q bus from the memory. The data is available to the client two clock cycles after the assertion of the RE, this data is held on the bus until the next RE is asserted. The DVLD signal is asserted on the same clock cycle that the data is available. Therefore, the client logic can monitor the DVLD signal for indication of valid data. However, DVLD only asserts for the first clock cycle that the new data is available, whereas the actual data may still be on the data bus.

If the FIFO is emptied then the EMPTY flag is asserted to indicate that no more data elements can be read. The AEMPTY flag is asserted when the number of elements in the FIFO equals the set threshold amount.

If a read operation is attempted while the FIFO is empty, the UNDERFLOW signal is asserted on the next clock cycle indicating that an error has occurred. The UNDERFLOW signal is asserted for each read operation that fails.

A sample timing diagram of a FIFO with depth configuration of 4, almost empty value set to 1, and rising clock edge is shown in [Figure 3-2](#).

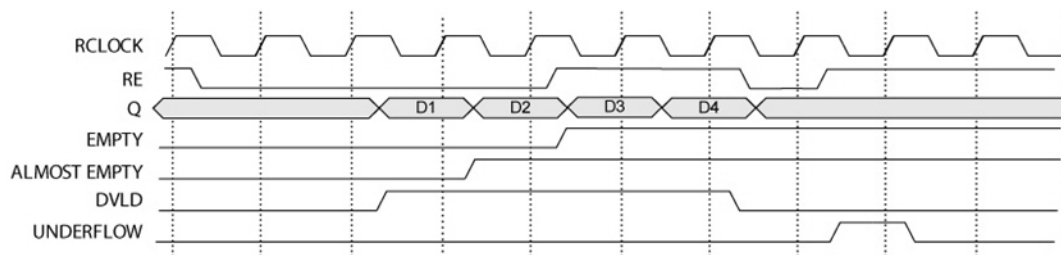


Figure 3-2 • Read Operation and Flags

Operations with a Variable Aspect Ratio

A FIFO with variable aspect width has different depth and width configurations for the write and read side. There are some special considerations when using this type of FIFO:

Data order - Write side has smaller width than Read side: The FIFO starts writing to the least significant portion of the memory up. (refer to the timing diagram below)

- **Data order** - The Write side has larger width than Read side, i.e. the FIFO starts reading from the least significant portion of the memory. Meaning if the first word into the write side is 0xABCD, the words read out of the FIFO will be 0xCD followed by 0xAB.
- **Full flag generation** - The FULL is asserted when a full word from the write perspective cannot be written in. The FULL de-asserted only if there is enough space in the FIFO to write a full word from the write aspect ratio. (refer to the timing diagram in [Figure 3-3](#))
- **Empty flag generation** - The EMPTY is de-asserted only when a full word from the read aspect ratio can be read out. The EMPTY is asserted if the FIFO does not contain a full word from the read aspect ratio (refer to the timing diagram in [Figure 3-3](#)).
- The implication of the status flag generation is that it is possible to have a partial word in the FIFO that may not be immediately visible on the read side. For example, consider when the write side has a smaller width than the read side. The write side writes 1 word and finishes. In this type of scenario, the application using the FIFO must consider what a partial data word represents.
- If the partial data word cannot be processed downstream than it is meaningless to take it out of the FIFO until it has reached a full-word. However, if the partial word is considered valid and can be processed downstream in its 'incomplete' state, then some other type of mechanism needs to be designed to handle this condition.

[Figure 3-3](#) illustrates a condition where the write side is configured has x4 width and the read side as x8 width.

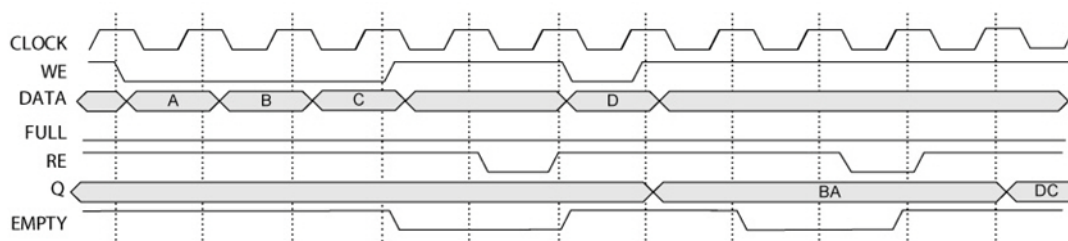


Figure 3-3 • Write and Read Operations with a Variable Aspect

4 – Port Description

Table 4-1 lists the FIFO Controller without Memory signals in the generated macro.

Table 4-1 • FIFO Controller without Memory Signals

Port	Direction	Description
WE	Input	Write data into FIFO when signal is asserted
RE	Input	Read data from FIFO when signal is asserted
WCLOCK	Input	All signals in the write domain are synchronous to this clock
RCLOCK	Input	All signals in the read domain are synchronous to this clock
FULL	Output	Indicates that the FIFO is full
EMPTY	Output	Indicates that the FIFO is empty
RESET	Input	Asynchronous reset
AEMPTY	Output	Indicates that the FIFO has reached the Almost Empty threshold value
AFULL	Output	Indicates that the FIFO has reached the Almost Full threshold value
AEVAL[]	Input	Dynamic Almost empty threshold value
AFVAL[]	Input	Dynamic Almost full threshold value
WACK	Output	Indicates that a write on the FIFO succeeded
DVLD	Output	Indicates that a read on the FIFO succeeded
OVERFLOW	Output	Indicates that a write in the previous clock cycle failed
UNDERFLOW	Output	Indicates that a read in the previous clock cycle has failed
RDCNT[]	Output	The remaining number of READ domain elements in the FIFO
WRCNT[]	Output	The remaining number of WRITE domain elements in the FIFO
MEMWADDR []	Output	Memory write address for external memory
MEMRADDR[]	Output	Memory read address for external memory
MEMWE	Output	Memory write enable for external memory
MEMRE	Output	Memory read enable for external memory
CLK	Input	Single Clock to drive WCLOCK and RCLOCK

A – Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call 800.262.1060

From the rest of the world, call 650.318.4460

Fax, from anywhere in the world, 408.643.6913

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Visit the Customer Support website (www.microsemi.com/soc/support/search/default.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the website.

Website

You can browse a variety of technical and non-technical information on the SoC home page, at www.microsemi.com/soc.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to [My Cases](#).

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. [Sales office listings](#) can be found at www.microsemi.com/soc/company/contact/default.aspx.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within [My Cases](#), select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the [ITAR](#) web page.



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