

Programmable Ramp Generator Technical Brief

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This technical brief provides a straightforward discussion on the PRG features, method of configuration and sample applications for different modes of operation.

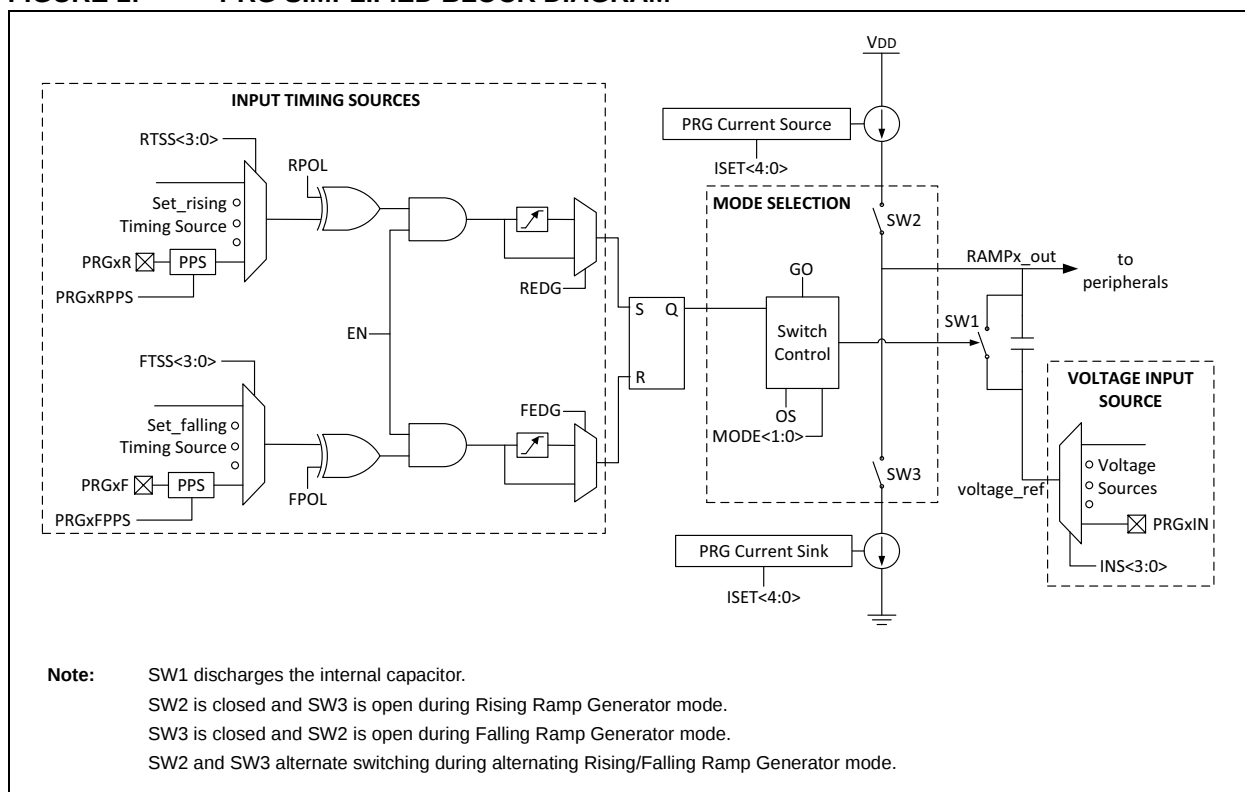
INTRODUCTION

A voltage ramp signal finds its purpose in a circuit application that requires a linear change of voltage. It is commonly used as a reference signal, slope compensator or a voltage sweep generator. The Programmable Ramp Generator (PRG) peripheral provides voltage ramp signals with no processor overhead. The PRG can produce a falling ramp, a rising ramp or alternating rising/falling ramp triggered from many input sources. A programmable current source/sink selects the slope rate of the PRG output.

BLOCK DIAGRAM

In the block diagram shown in [Figure 1](#), the PRG's ramp generation function works by driving a constant current into the internal capacitor. The resulting voltage across this internal capacitor is added to or subtracted from the voltage input source. The mode of operation of the ramp output relies mainly on the control of internal analog switches. The duration between the moment the ramp starts and stops is determined by the input timing sources.

FIGURE 1: PRG SIMPLIFIED BLOCK DIAGRAM



INPUT TIMING SOURCES

The PRG combines two selectable independent timing sources to generate control timing for its ramp output. These sources can be an external input from the PRGxR and PRGxF pins, or output/s from other peripherals. The set rising input is selected by setting the Set Rising Timing Source Select bits (RTSS<3:0>) in the PRGxRTSS register while the set falling input is selected by setting the Set Falling Timing Source Select bits (FTSS<3:0>) in the PRGxFTSS register. The polarity of timing sources is selected by setting the

Fall Event Polarity Select bit (FPOL) and the Rise Event Polarity Select bit (RPOL) in the PRGxCON1 register.

In [Figure 2](#), when set rising input (S) is true and set falling input is false (R), the PRG output timing (Q) is true or vice versa. When both S and R are false, Q retains its previous state. However, when both S and R inputs are true, R dominates S and forces Q to False state. This condition can be encountered when the same source for both set rising and falling is used. To control the operation with this condition, either of the two timing inputs must be inverted. Otherwise, Q will not produce a timing pulse as shown in [Figure 3](#).

FIGURE 2: DIFFERENT INPUT SOURCES

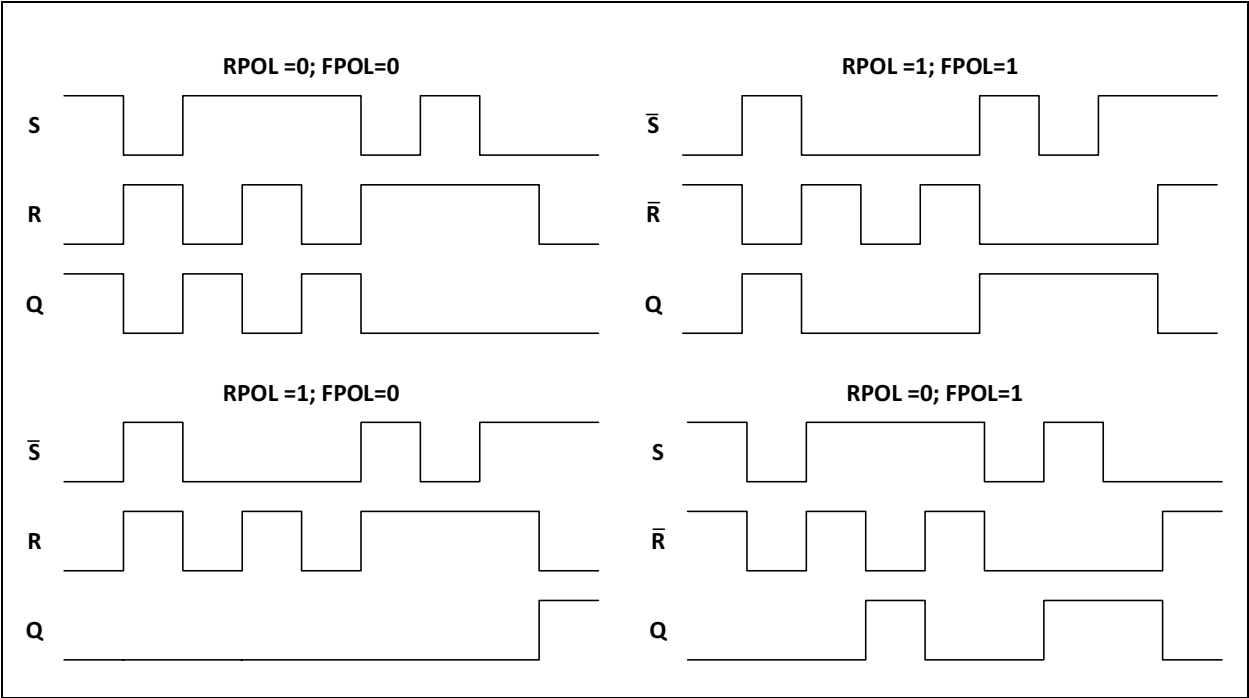
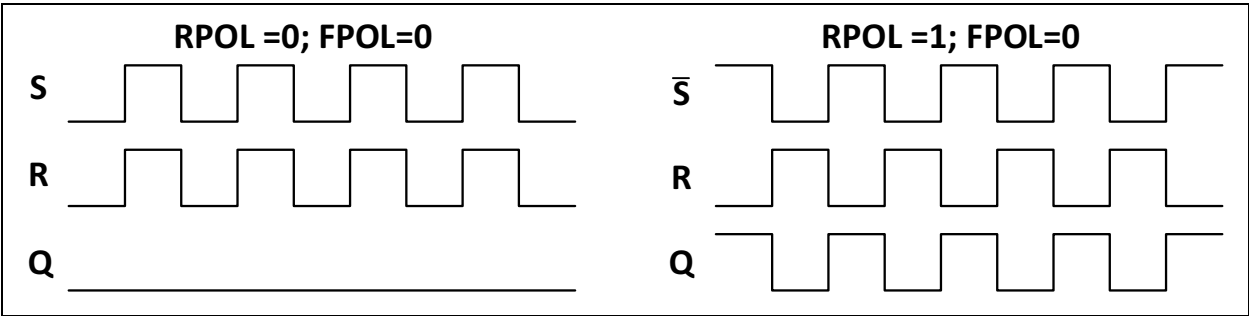


FIGURE 3: SINGLE-ENDED INPUT SOURCE



Aside from the selectable timing input sources and the polarity event, the input timing source detection method can also be selected. The two event input detection methods for PRG are level sensitive and edge sensitive. The set rising and set falling input detection are selected by setting the Set Rising Input Mode Select bit (REDG) and Set Falling Input Mode Select bit (FEDG) in the PRGxCON0 register, respectively. In general, edge-sensitive operation is useful when timing inputs are derived from periodic sources while level-sensitive operation is useful when timing inputs are derived from voltage thresholds.

The timing sources for the PRG may vary from device to device. Some of the available peripherals that can be used as PRG's timing sources are Comparator, PWM (Pulse-Width Modulation) and CCP (Capture, Compare, PWM) output. The peripheral must be configured beforehand and selected as the PRG's timing source. For a device that has Peripheral Pin Select (PPS), the PRGxR and PRGxF are remapped to the desired input pins through the PPS Input Selection Register (xxxPPS). By changing the "xxx" notation in the register name to PRGxR and PRGxF, any available I/O pin can be selected as PRGxR and PRGxF. For example, in order to use RA0 and RA1 as the PRGxR pin and PRGxF pin respectively, the xxxPPS becomes PRGxRPPS and PRGxFPPS. This register should be set to a corresponding value defined in the data sheet to assign RA0 and RA1 as PRGxR pin and PRGxF pin.

Voltage Input Source

The PRG's voltage input source serves as a voltage reference to the linear ramp output. The input source can be any of the following: external source from the PRGxIN0 or PRGxIN1 pins, the buffered output of the internal Fixed Voltage Reference (FVR), or one of the internal Digital-to-Analog Converters (DAC). The op amp outputs share the PRGxIN0 and PRGxIN1 pins so that the reference signal can be buffered by the op amp by enabling both the op amp and selecting the corresponding PRGxIN pin. Reference sources are selected by setting the Voltage Input Select bits (INS<2:0>) in the PRGxINS register.

PRG Current Source/Sink

The programmable current on the PRG has a vast selection of source/sink currents to configure the desired PRG output slope rate. In applications that require a steep voltage rate in the PRG output, a high-current setting must be selected. The constant ramp current is selected with the Source/Sink Set bits (ISET<3:0>) in the PRGxCON2 register. [Table 1](#) shows the current settings for the PRG peripheral of a PIC16F1769 microcontroller. The current settings may vary from one device to the other. Please refer to the data sheet of the particular device.

TABLE 1: PROGRAMMABLE RAMP GENERATOR CURRENT SETTINGS OF PIC16F1769

ISET<4:0>	Current Setting (μA)	Slope Rate (V/μs)	ISET<4:0>	Current Setting (μA)	Slope Rate (V/μs)
0h	2	0.2	10h	10	1.0
1h	2.5	0.25	11h	11	1.1
2h	3	0.3	12h	12	1.2
3h	3.5	0.35	13h	13	1.3
4h	4	0.4	14h	14	1.4
5h	4.5	0.45	15h	15	1.5
6h	5	0.5	16h	16	1.6
7h	5.5	0.55	17h	17	1.7
8h	6	0.6	18h	18	1.8
9h	6.5	0.65	19h	19	1.9
Ah	7	0.7	1Ah	20	2
Bh	7.5	0.75	1Bh	21	2.1
Ch	8	0.8	1Ch	22	2.2
Dh	8.5	0.85	1Dh	23	2.3
Eh	9	0.9	1Eh	24	2.4
Fh	9.5	0.95	1Fh	25	2.5

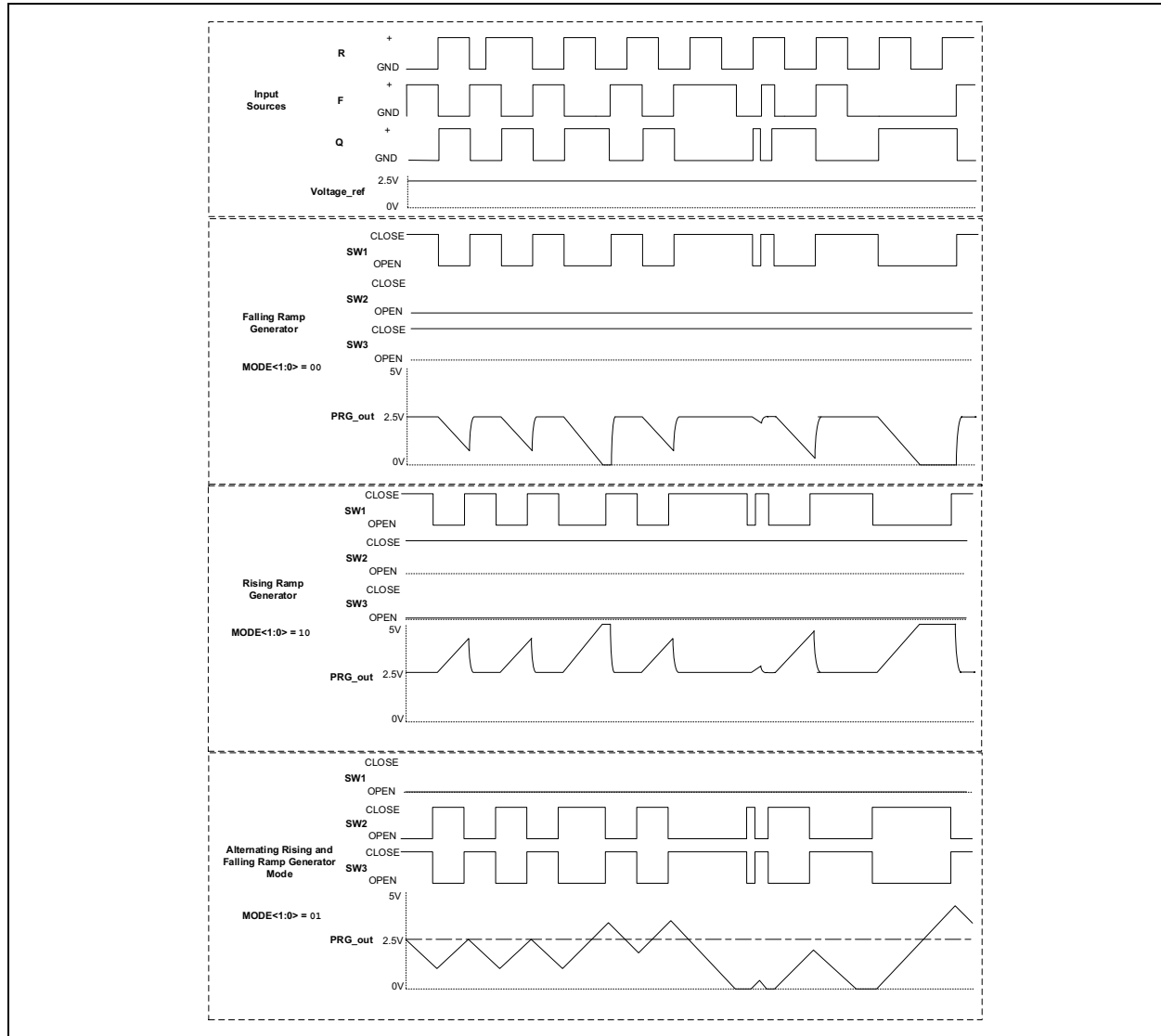
PRG MODE SELECTION

The PRG can be operated in the following three voltage ramp generator modes:

1. Falling Ramp Generator – Slope Compensation
2. Rising Ramp Generator
3. Alternating Rising/Falling Ramp Generator

These modes are selected by setting the Programmable Ramp Generator Mode Selection bits (MODE<1:0>) of PRGxCON0. [Figure 4](#) shows the PRG output for each mode that is controlled by internal analog switches SW1, SW2 and SW3. SW1 discharges the internal capacitor when the switch is closed, while SW2 and SW3 connect the other side of the capacitor to the programmable current source and current sink, respectively. The switching of SW2 and SW3 dictate the flow of charge in the internal capacitor. These switches toggle depending on the configured mode.

In the Falling Ramp mode, SW2 is open, SW3 is closed and SW1 toggles ON and OFF. Since SW3 is closed while SW1 is open, the internal capacitor is charged by a current sink. The voltage across the capacitor is subtracted from the voltage input source and produces a falling ramp output at the configured slope rate. The Rising Ramp mode has the same operation with the Falling Ramp mode except for the SW2 and SW3 switching states. In this mode, SW2 is closed and SW3 is open. When SW2 is closed while SW1 is open, the internal capacitor is charged by the current source, producing a rising ramp output. In the alternating Rising/Falling Ramp mode, SW1 remains open and SW2 and SW3 toggle alternately. This means that when SW2 is closed, SW3 is open or vice versa. Since SW1 remains open in this mode, the reference voltage has no effect on the PRG output because there will be no discharge state to take it to the reference voltage. The SW2 and SW3 that toggles alternately will connect the internal capacitor to either source or sink current to charge the capacitor from one direction to another. This will produce an alternating rising and falling ramp on the PRG output.

FIGURE 4: PRG MODE OF OPERATION

One of the challenges with the alternate switching of SW2 and SW3 in Alternating Ramp mode is that the source and sink currents that flow through the internal capacitor do not exactly match due to several factors. These factors can be the parasitic resistance of the capacitor, noise, production variance and temperature. It greatly affects the performance of the PRG operating in an open-loop system (Figure 5), which determines the PRG's average output voltage to drift over time. This event is an inherent limitation of the system, which makes it impossible to be trimmed out. However, the average voltage drift can be reduced by creating a feedback-loop system on the PRG (Figure 6). The PRG output is tied to one of the comparator inputs while the comparator output acts as one of the PRG timing inputs to maintain the peak voltage level of the PRG output. Hence, the average voltage of the PRG output in a closed-loop system will have a small drifting deviation compared with the open-loop system.

To be able to see the PRG's average voltage drift in Alternating Ramp Generator mode, the device with PRG module has been subjected to a continuously increasing temperature environment. This accelerates the effect of temperature in the performance of the PRG output. As shown in Figure 7, there is a significant average voltage deviation when the PRG operates in an open-loop system. However, this deviation minimizes and produces almost constant average voltage when a closed-loop system is employed.

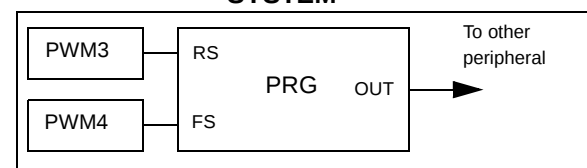
FIGURE 5: PRG'S OPEN-LOOP SYSTEM

FIGURE 6: PRG'S CLOSED-LOOP SYSTEM

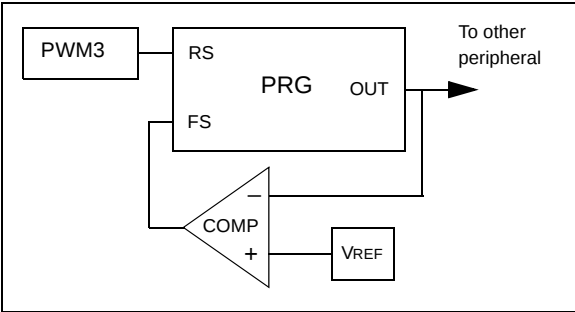
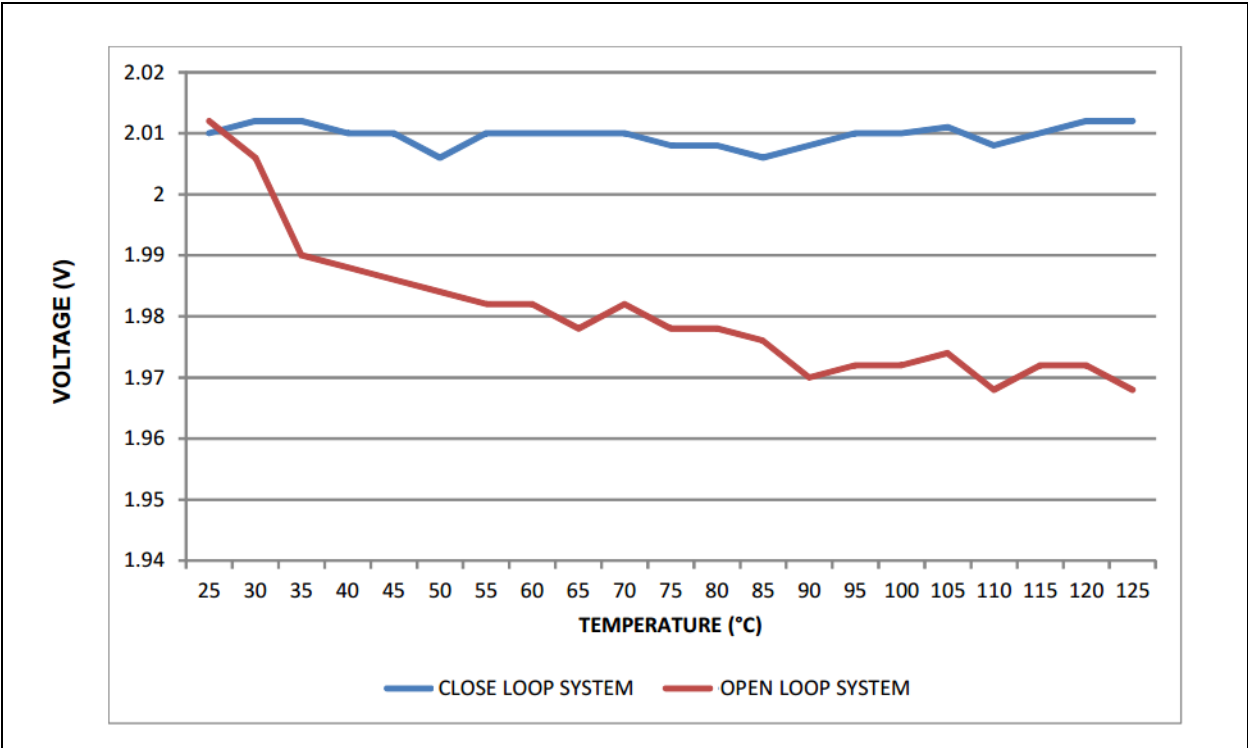


FIGURE 7: PRG AVERAGE VOLTAGE VS. TEMPERATURE



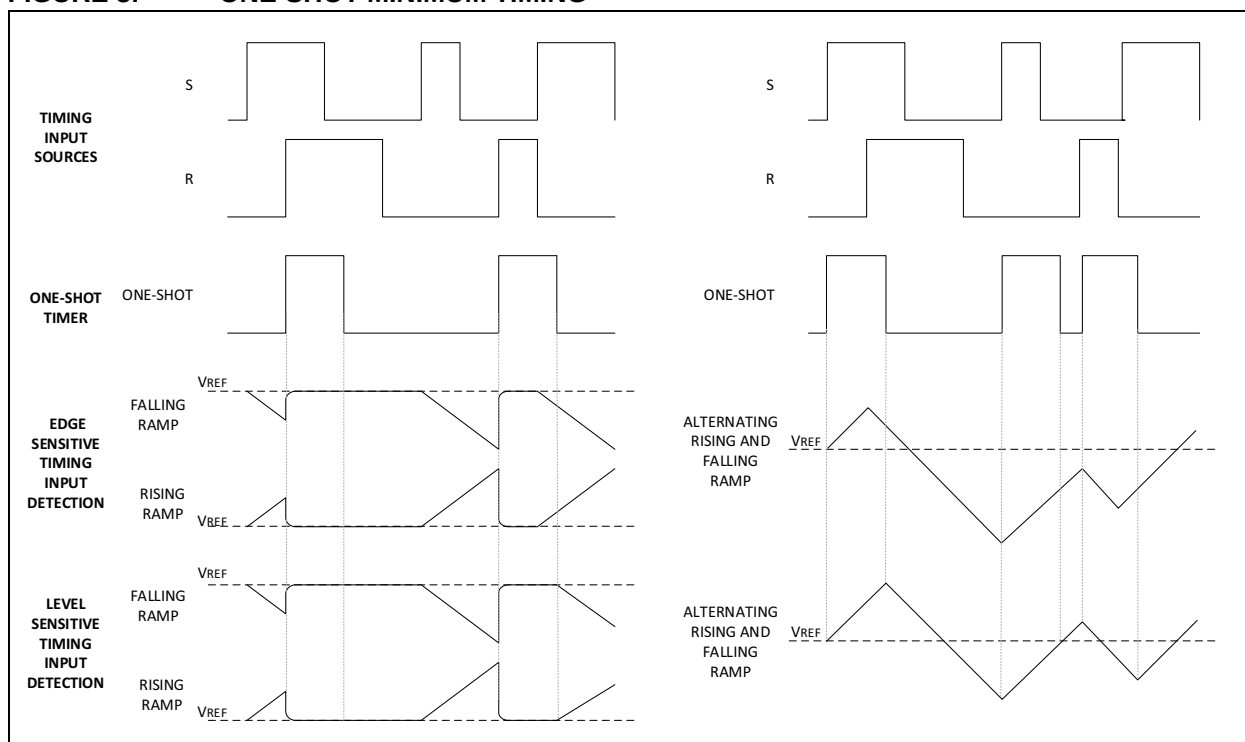
ONE-SHOT TIMER

The PRG module features an optional one-shot timer that ensures a minimum capacitor discharge time for both the Rising and the Falling Ramp modes and a minimum rising or falling ramp duration for the Alternating Ramp mode. In the Rising and Falling Ramp modes, the one-shot timer ensures that the capacitor is discharged by holding the capacitor shorting switch SW1 closed for at least the one-shot period (typically 50 ns), whereas in the Alternating Ramp mode, both the rising and falling ramps persist for a minimum of the one-shot period.

Edge-sensitive timing inputs that occur during the one-shot period are ignored while level-sensitive timing inputs that occur during, and extend beyond, the one-shot period are suspended until the end of the one-shot time. The one-shot timer is enabled by setting the OS bit of the PRGxCON0 register.

Figure 8 shows the effect of one-shot and input timing detection on the Rising Ramp, Falling Ramp and Alternating Ramp modes.

FIGURE 8: ONE-SHOT MINIMUM TIMING



ENSURING PRG PROPER OPERATION

To ensure proper operation of the PRG, the following bits must be set and monitored: the Enable bit (EN) and the Start bit (GO) in the PRGxCON0 register and the Ready Status bit (RDY) in the PRGxCON1 register. The EN bit should be set first to permit the PRG peripheral to stabilize the selected programmable current and analog circuits before operation. Once it has been stabilized, the RDY bit will be set indicating that PRG peripheral is prepared to provide the linear ramp output. The GO bit can now be set to start the PRG operation. However, setting the GO bit triggers the one-shot timer even if the one-shot is disabled. This event leads to an extended time duration of one-shot period before the PRG operates.

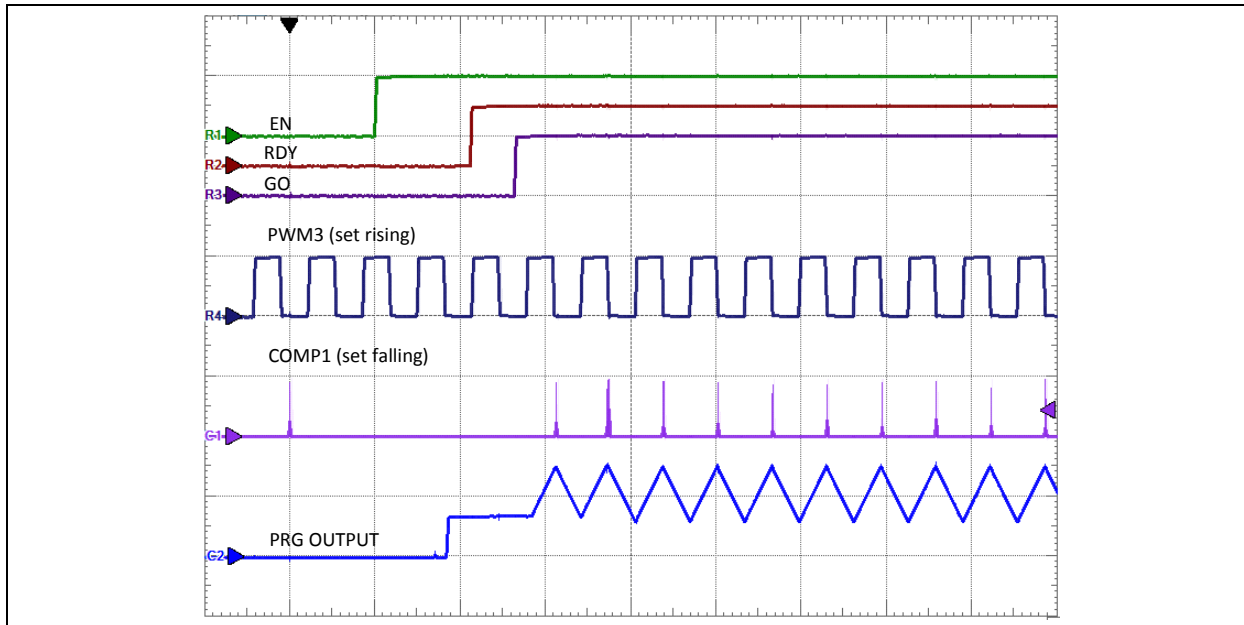
Example 1 exhibits the code sequence to ensure predictable PRG operation. The SYSTEM_Initialize() function initializes the peripherals that were configured using the MPLAB® Code Configurator (MCC), including the setting of the PRG enable. It is followed by the while(!PRG1_IsReady()) to evaluate the status of the PRG RDY bit. When the PRG1_IsReady() becomes true, the firmware will execute the PRG1_StartRampGeneration() function to set the PRG GO bit. Figure 9 shows the timing diagram of the PRG.

EXAMPLE 1: CODE SEQUENCE TO ENSURE PREDICTABLE PRG OPERATION

```
void main(void)
{
    // initialize the device
    SYSTEM_Initialize();           //includes PRG enable and PRG settings
    while(!PRG1_IsReady());       //wait for PRG to stabilize
    PRG1_StartRampGeneration();    //start PRG operation

    while (1)
    {
        // Add your application code
    }
}
```

FIGURE 9: PRG TIMING DIAGRAM



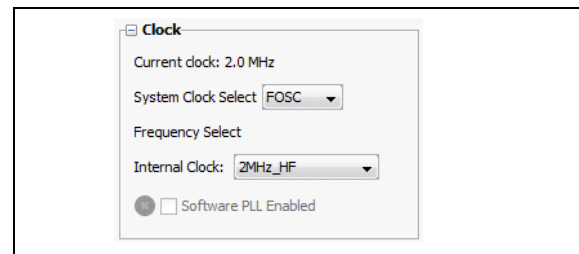
CONFIGURING THE PRG USING MPLAB® CODE CONFIGURATOR (MCC)

In this section, the MPLAB® Code Configurator (MCC) is utilized to easily configure the PRG peripheral. The MCC is a user-friendly plug-in tool for MPLAB® X IDE, which generates drivers for controlling and driving peripherals of PIC® microcontrollers, based on the settings and selections made in its Graphical User Interface (GUI). For installation and setup of the MCC in MPLAB X IDE, refer to the “MPLAB Microchip Code Configurator User’s Guide” (DS40001725) which can be found at www.microchip.com.

The following steps can be used as a guide on how to configure the PRG peripheral in PIC16F1769 using MCC.

1. Navigate to: Tools – Embedded – MPLAB Code Configurator to launch the MCC.
2. Set the desired Configuration registers and the system clock source on the System label inside of MPLAB X in the Project Resources window.

EXAMPLE 2:



- Configure the set rising timing input source to be used:

- PWM Configuration:**

- In the Device Resources area where lists of all the supported peripherals of the PIC16F1769 are shown, select the peripheral to configure (i.e., PWM). Expand the PWM and the 10-bit under it. Double click the PWM3::PWM to add it to the Project Resources area.
- From the Project Resources area, select the peripheral to configure (i.e., PWM3::PWM). The parameters of the selected peripheral will be displayed in the composer area. These parameters can be modified to the desired peripheral settings.
- In the Composer area, after selecting PWM3::PWM in the Project Resources, select the enable PWM check-box, set the duty cycle to 50% and the Timer2 as the timing source. When Timer2 is selected as the timing source, the configurator automatically adds it to the Project resources.

EXAMPLE 3:

Please refer to the selected timer to adjust the PWM frequency

☒ Enable PWM PWM Polarity: ☐ inverted ☒ not inverted

Select a timer: **Timer2** PWM Period: 32.0000 us

Duty Cycle: **50** % PWM Frequency: 31.25 kHz

CCPR Value: 31 PWM Resolution: 6 bits

- Timer2 Configuration:**

- In the Composer area, after selecting the TMR2::Timer in the Project Resources, select the enable Timer check-box and set the clock source to FOSC/4. The prescaler and postscaler should be set to 1:1 and the Period Value to 0x0F.

EXAMPLE 4:

☒ Enable Timer

Timer Clock: Clock Source: **FOSC/4** Timer Period: Period Value: 0x00 ≤ **0x0F** ≤ 0xFF

Postscaler: **1:1** Timer Period: 500.0 ns ≤ **8.0 us** ≤ 128.0 us

Prescaler: **1:1** Ext Reset Source: **T2INPPS pin**

Polarity: **Rising Edge** Control Mode: **Roll over pulse**

☐ Enable Prescaler O/P Sync Start/Reset Option: **Software control**

☐ Enable Clock Sync

- Configure the set falling timing input source to be used:

- Comparator Configuration:**

- In the Composer area, after selecting the CMP1::CMP in the Project Resources, select the enable Comparator check-box. Set the positive and negative inputs to PRG1_output and CIN1-, respectively.

Note: The CIN1- in this example is from an external input voltage. This voltage acts as the comparator's trip point (i.e., 4.5V).

EXAMPLE 5:

☒ Enable Comparator Positive Input: **PRG1_out...**

☐ Enable Synchronous Mode Negative Input: **CIN1-**

☐ Enable Comparator Hysteresis Output Polarity: ☐ Inverted ☒ Non Inverted

☐ Enable Comparator Zero Latency Filter Interrupt Flag Set On: ☐ rising edge ☐ falling edge

- Configure the voltage input source to be used:

- FVR Configuration:**

- In the Composer area, after selecting the FVR::FVR in the Project Resources, select the enable FVR check-box. Change the FVR amount sent to Comparators, DAC and CPS to 2x.

EXAMPLE 6:

☒ Enable FVR FVR amount sent to Comparators, DAC and CPS: **2x**

FVR amount sent to ADC: **off**

☐ Enable Temperature Sensor

- After configuring the timing input and voltage input sources, the PRG peripheral can now be configured by clicking the PRG1::Default in the Project Resources area.

- PRG Configuration:**

- In the Composer area, select the Enable Ramp Generator option. Set the Ramp Generator mode to alternating ramp generator and the voltage input source to FVR_buffer.
- Set the PWM3_output for the ramp rising timing source with Edge input sensitivity and High rising event polarity.
- Set the sync_C10UT for the ramp falling timing source with Level input sensitivity and High falling event polarity.
- Set the slope rate of the PRG to 0.20 V/us.

EXAMPLE 7:

☒ Enable Ramp Generator

Ramp Generator Mode: **alternating ramp generator** ☐ Enable One Shot

Voltage Input Source: **FVR_buffer1** Slope Rate: 0.2 V/us ≤ **0.20 V/us** ≤ 2.5 V/us

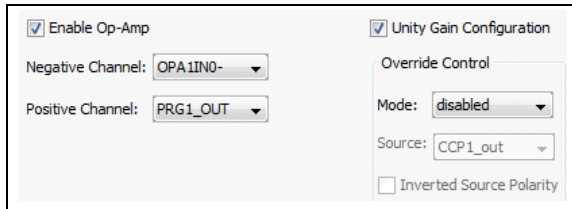
Ramp Rising Timing Source: Timing Source: **PWM3_output** Ramp Falling Timing Source: Timing Source: **sync_C10UT**

Input Sensitivity: ☒ Edge ☐ Level Input Sensitivity: ☐ Edge ☒ Level

Rising Event Polarity: ☒ High ☐ Low Falling Event Polarity: ☒ High ☐ Low

11. To output the PRG waveform to the microcontroller pin, the PRG output must be connected to OPA peripheral.
 - OPA Configuration:
 - In the Composer area, after selecting the OPA1::OPA in the Project Resources, select the enable op amp and unity gain configuration check-boxes. Set the positive channel of OPA to PRG1_OUT.
12. Click the Generate Code button on the top left corner of the Composer area. This will generate the main.c file to the project automatically. It will also initialize each peripheral and leave an empty while(1) loop for custom code entry. See [Example 9](#) for the generated initialization code for the PRG peripheral.
13. On the generated main.c file, additional code sequence must be added to initiate PRG operation ([Example 1](#)). [Figure 9](#) is the timing diagram for this example.

EXAMPLE 8:



EXAMPLE 9: MCC GENERATED INITIALIZATION CODE FOR PRG

```
void PRG1_Initialize(void)
{
// RG1MODE alternating ramp generator; RG1OS disabled; RG1FEDG level_sensitive; RG1REDG
edge_sensitive; RG1G0 not operating; RG1EN enabled;
    PRG1CON0 = 0xA4;
    // RG1RPOL active_high; RG1RDY not ready; RG1FPOL active_high;
    PRG1CON1 = 0x00;
    // INS FVR_buffer1;
    PRG1INS = 0x02;
    // RG1ISET 0;
    PRG1CON2 = 0x00;
    // RTSS PWM3_output;
    PRG1RTSS = 0x05;
    // FTSS sync_C1OUT;
    PRG1FTSS = 0x00;
}
```

APPLICATIONS OF THE PRG

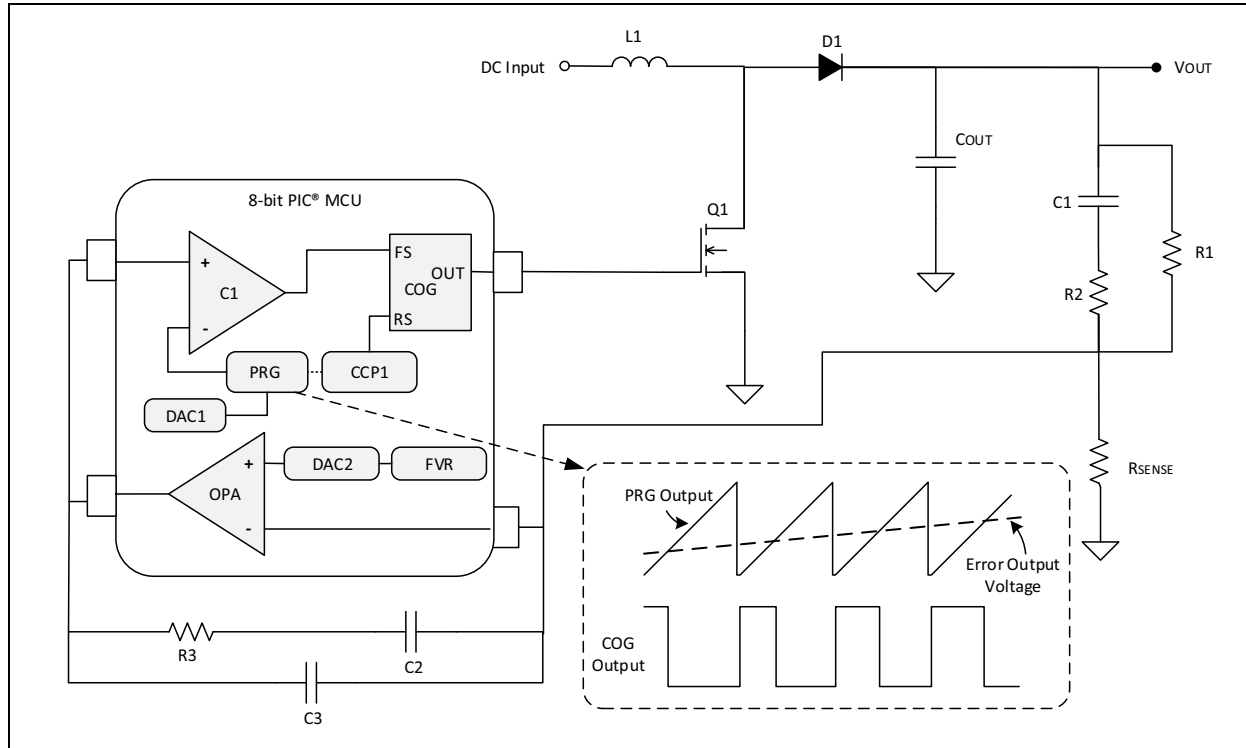
In this section, sample applications of PRG based on its mode of operation are presented.

Slope Compensation in Continuous Current Mode Control

The PRG in Falling Ramp mode can be used as slope compensator in a DC-to-DC converter operating in Continuous Current mode as shown in [Figure 10](#). The decaying ramp produced by the PRG prevents the sub-harmonic oscillations and helps stabilize the output when the duty cycle exceeds 50%. Refer to TB3120 – “Slope Compensator on PIC® Microcontrollers” (DS90003120) and TB3104 – “Boost Converter Using the PIC16F753 Analog Features” (DS90003104) for more information about the slope compensation operation.

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FIGURE 11: DC-TO-DC CONVERTER USING VOLTAGE MODE



Voltage Reference in Class-D Amplifier

The alternating rising and falling waveform produced by the PRG can be used as a reference signal in a half-bridge and full-bridge class-D amplifier (Figure 12). In this application, a close loop PRG configuration is implemented to address the average voltage problem in Alternating Ramp mode. The PRG's alternating ramp output is compared with the analog audio input signal through an internal comparator with inverted output.

The comparator's output produces pulse waveforms that are directly proportional to the instantaneous values of the audio signal (Figure 13). These pulse waveforms are fed to the COG whose complementary PWM outputs drive Q1 and Q4 high, Q2 and Q3 low or vice versa. Finally, a low pass filter is used to remove the carrier frequency and recreate the analog audio signal.

FIGURE 12: FULL-BRIDGE CLASS-D AMPLIFIER

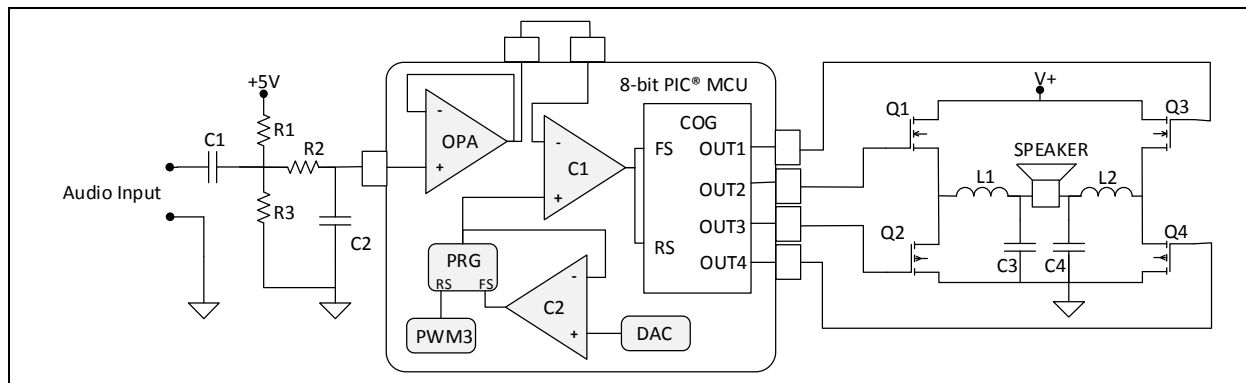
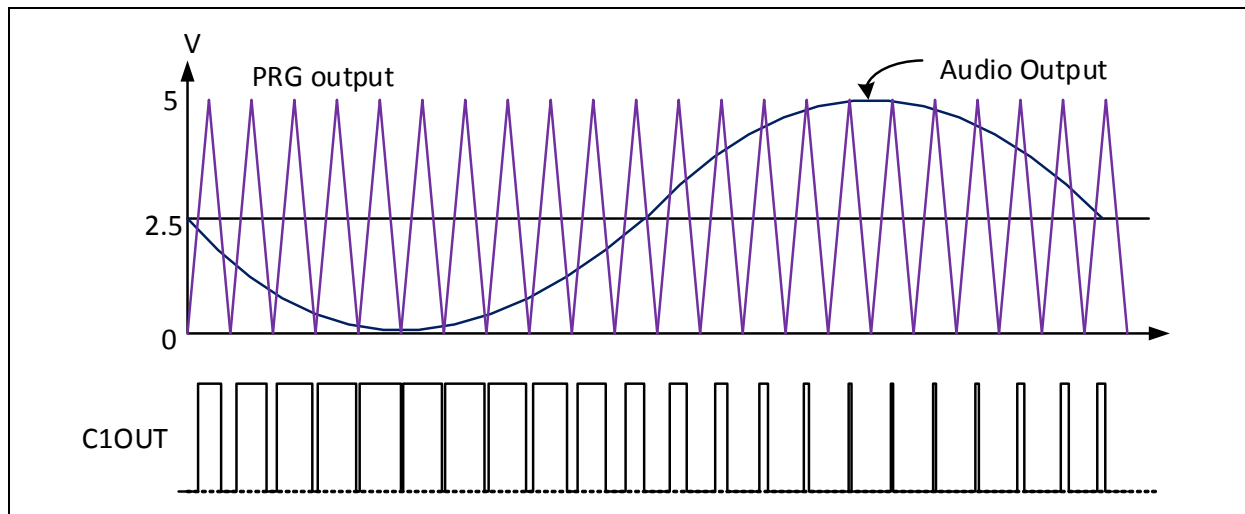


FIGURE 13: CLASS-D ANALOG AND DIGITAL WAVEFORMS

CONCLUSION

This technical brief describes how the Programmable Ramp Generator peripheral works on PIC microcontrollers. It covers the PRG peripherals' features and capabilities. The technical brief also provides sample initialization codes to ensure proper operation of the peripheral and sample application for each of the PRG modes.

TB3140

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