TB3128

CRC and Memory Scan on 8-Bit Microcontrollers Technical Brief

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INTRODUCTION

In most applications today, data integrity is necessary for both storage and transmission. A popular error-detection technique, the Cyclic Redundancy Check (CRC) can be used to preserve the integrity of data in memory and communications.

This technical brief provides information about the Cyclic Redundancy Check (CRC) peripheral along with the Memory Scan functionality available on a range of PIC® microcontrollers. The CRC calculation and Memory Scan methods along with different standards and commonly used CRC polynomials are also explained in this technical brief. The CRC and Memory Scan peripheral are useful while performing the memory tests required in the IEC 60730 standard to support the Class B certification.

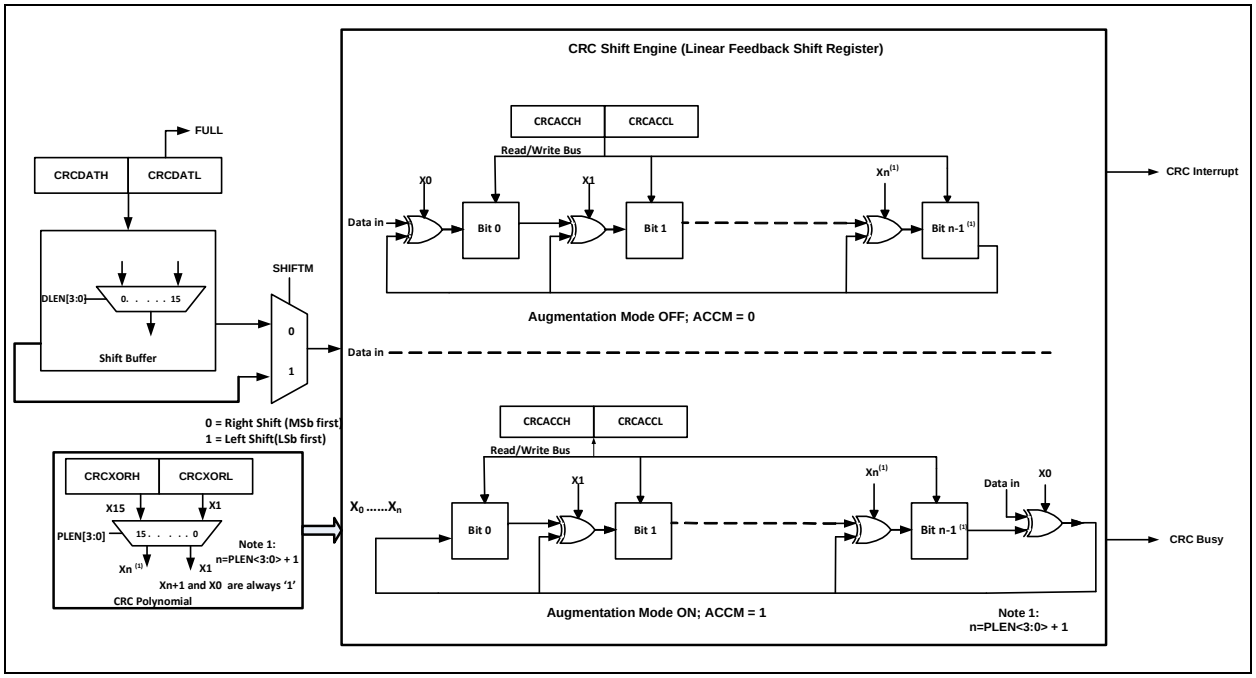
CRC PERIPHERAL ON PIC MICROCONTROLLER

The Cyclic Redundancy Check (CRC) module provides a software-configurable hardware-implemented CRC checksum generator. The CRC algorithm treats the data to be a binary number. This number is divided by another binary number called the polynomial. The remainder of this division is the CRC checksum, which is appended to the data. Every integer can be expressed uniquely as a polynomial in base 2 with coefficients that are either '0' or '1'. It is convenient to interpret the polynomial in terms of a dummy variable X.

For example, a message 110101 is represented by the polynomial: $X^5 + X^4 + X^2 + 1$ $(1*2^5 + 1*2^4 + 0*2^3 + 1*2^2 + 0*2^1 + 1*2^0)$

In communication systems, when messages are transmitted, the CRC checksum is appended to the message. The receiver then divides the message (including the calculated CRC) by the same polynomial that the transmitter used (in order to implement a CRC based on a polynomial, the transmitter and receiver must use the same polynomial). If the result of this division yields a zero, then the transmission is considered to be successful. However, if the result of this division is not equal to zero, then an error is considered to have occurred during the transmission and corrective action needs to be taken against the presumed data corruption. A CRC is called an n-bit CRC when its checksum value is n-bits long.

FIGURE 1: BLOCK DIAGRAM OF CRC



The CRC module uses a Linear Feedback Shift Register (LFSR) implementation to perform the polynomial division required for the CRC calculation, as shown in Figure 1. The CRC module can accept up to a 17-bit (n+1) generator polynomial. In any (n+1) bit polynomial, X^n and X^0 are always '1'. While loading the (n+1) bit polynomial into the CRCXOR<15:1> register, only X^{n-1} to X^0 should be entered. The PLEN<3:0> bits are used to specify the length of the polynomial. While loading the length, the MSB and LSB of the (n+1) bit polynomial should be excluded. Hence, n-1 should be loaded.

For example, in CRC-16-ANSI, a 17-bit polynomial $X^{16}+X^{15}+ X^2 + 1$, n = 16.

So, PLEN<3:0> = n – 1 = 15

CRCXOR<15:1> = 0b100000000000010

(CRCXOR <0> is unimplemented since CRC hardware considers X^{16} and X^0 to be '1')

So, CRCXOR can be either 0x8005 or 0x8004. The CRC engine reads it as 0x8005, but if CPU reads it using software, it is read as 0x8004.

The data needs to be loaded into the CRCDATH and CRCDATL registers in the same sequence. Once the data is loaded into the CRCDATL register, the entire 16-bit data is moved into the Shift buffer, this is a readable register. The DLEN bits determine the data width (the valid bits in the CRCDATH and CRCDATL registers). Only the data as determined by the DLEN bits are moved to the shift buffer. If the SHIFTM bit is set to '1', the data will be shifted with LSb first, else data will be shifted with MSb first.

Augmentation of Zeros

For the CRC calculation to be completed, all the data bits need to be shifted through all the XOR gates, and this requires adding zeros equal to the length of the polynomial at the end. This is known as augmentation of zeros. Previously, this had to be taken care of in software. Now, Augmentation mode is available to take care of this in hardware, thereby reducing the software overhead. By setting ACCM bit to '1', one can enable Augmentation mode.

Initial CRC Value (Seed Value)

This is the initial value that provides a fixed starting point from which the data bits can progress. Many CRC algorithms initialize their seed value to a non-zero value. As in real applications, many data strings are likely to begin with a long series of '0's and the computation of CRC ignores any number of '0's ahead of the first '1' bit.

To avoid this problem, before computing the n-bit CRC we will always begin by exclusive ORing the leading n bits with an n-bit string of non-zero value.

The seed value can be used in two methods for the CRC calculation, for example:

Direct Method

The seed value is loaded in to the CRCACC <15:0> registers.

Non-Direct Method

The seed value is considered to be the initial data value and prefixed with the actual data stream and the CRCACC<15:0> register is loaded with 0x0000.

The BUSY bit indicates if the CRC has completed calculations. Once the BUSY bit is '0', the check value can be read from the CRCACC<15:0> registers. The CRCIF flag will also get set to '1'.

MEMORY SCAN MODULE ON PIC MICROCONTROLLER

The Program Memory Scan module can be used in conjunction with the CRC module to perform a CRC calculation over a range of program memory addresses. The CRC module is coupled with the Memory Scan module for faster CRC calculations. The Memory Scan module can automatically provide data to the CRC module. This memory test will be helpful for the IEC 60730 standard to support the Class B certification.

Four modes of memory scan operation are possible:

Burst: CPU operation is stalled until the whole memory scan is completed. It gives highest memory scan throughput.

Concurrent: Scan starts immediately after setting of SCANGO bit. CPU operation is stalled during the memory access.

CPU resumes execution following each access.

Triggered: Waits to begin the scan until the rising edge from separate trigger clock. CPU operation is stalled during the memory access.

CPU resumes execution following each access.

Peek: Waits for an instruction cycle in which the CPU does not need to access the NVM (such as a branch instruction) and uses that cycle to do its own NVM access. It gives the lowest throughput. CPU operation is unaffected.

The Memory Scanner can automatically provide data to the CRC module when data is placed in the program memory. When Memory Scan is used in Peek mode, it has the advantage of freeing the CPU for other tasks, while the data is being checked for errors using CRC.

Interrupt interaction during memory scan: If the INTM bit is set, the interrupt will take precedence there by delaying the memory scan. If INTM is not set, the scanner will take precedence over the interrupt, resulting in increased interrupt response latency.

Configuration of the CRC and Memory Scan Peripheral

Some commonly used CRC generator polynomials are as follows:

TABLE 1: COMMONLY USED CRC GENERATOR POLYNOMIALS

Name	Polynomial	Polynomial Presentation	Seed Value
SDLC (CRC-16-CCITT)	$X^{16} + X^{12} + X^5 + 1$	0x1021	0xFFFF
CRC-16-ANSI	$X^{16} + X^{15} + X^2 + 1$	0x8005	0
CRC12	$X^{12} + X^{11} + X^3 + X^2 + X + 1$	0x80F	0

Configuring the CRC

This section provides the configuration sequence for the CRC in the form of a code snippet.

EXAMPLE 1: CODE SNIPPET FOR CRC-CCITT STANDARD FOR DIRECT MODE CRC

```
unsigned char data_buffer[] = {0x31,0x32,0x33,0x34,0x35,0x36,0x37,0x38,0x39};
CRCCON0bits.EN = 1; // enable the CRC module
CRCACC = 0xFFFF; //seed a starting CRC value
CRCXOR = 0x1021; //CRC generator polynomial for CRC-CCITT
CRCCON1bits.DLEN = 0b0111; //length of the data word = 8 bits
CRCCON1bits.PLEN = 0b1111; //order of the polynomial = 16
CRCCON0bits.ACCM = 1; //Direct CRC algorithm, zero augmentation not required
CRCCON0bits.SHIFTM = 0; // MSb of the data will be shifted first
CRCCON0bits.CRCGO = 1; //start the CRC module
data_size = sizeof(data_buffer); // data_buffer is the array containing data
for (data_index=0; data_index < data_size; data_index++  )
{
    while (CRCCON0bits.CRCFULL); // wait until the data registers are full
    if (CRCCON1bits.DLEN <8){ // data has < 8 bits; load data in CRCDATL
        CRCDATL = data_buffer[data_index];}
    else {// data has> 8 bits; load CRCDATAH register first and then CRCDATL
        CRCDATH = (data_buffer[data_index] & 0xFF00)>>8;
        CRCDATL = (data_buffer[data_index] & 0xFF);    }
}
while(CRCCON0bits.BUSY);// check if CRC calculation is completed
crc = CRCACC; // read the CRC check value ( = 0x29B1 for given data sequence)
```

Configuring the Memory Scan

According to the IEC 60730 standard to support the Class B certification, the memory tests are performed periodically during system run time. At the system start-up, the CRC checksum of the data stored in the program memory (Flash) is calculated and can be used as a reference checksum. It can be stored in the Flash memory. During run time, the CRC and Memory Scan functions can be called periodically. The calculated checksum during run time can be compared with the reference checksum. If both the checksums are equal, then the memory test is considered to have passed.

EXAMPLE 2: CODE SNIPPET FOR MEMORY SCAN USING CRC-CCITT STANDARD FOR NON-DIRECT MODE CRC

```
SCANCON0bits.EN = 1; // enable the Memory Scan module
SCANCON0bits.MODE = 0; // Concurrent mode
SCANCON0bits.INTM = 0; //Interrupts do not prevent NVM access
SCANLADR = STARTADR; // load beginning location of the memory to be scanned
SCANHADR = STOPADR; //load the end location of the memory to be scanned

CRCCON0bits.EN = 1; // enable the CRC module
CRCACC = 0xFFFF; //seed a starting CRC value
CRCXOR = 0x1021; //CRC generator polynomial for CRC-CCITT
CRCCON1bits.DLEN = 0b0111; //length of the data word = 8 bits
CRCCON1bits.PLEN = 0b1111; //order of the polynomial = 16
CRCCON0bits.ACCM = 1; //zeroes equal to order of polynomial will be augmented
CRCCON0bits.SHIFTM = 0; // MSb of the data will be shifted first
CRCCON0bits.CRCGO = 1; //start the CRC module
SCANCON0bits.SCANGO = 1; //Begin the scan
while(SCANCON0bits.SCANGO); // wait for scanner to finish pushing data in to
//the CRC data registers
while(CRCCON0bits.BUSY); //check if CRC calculation is completed
crc = CRCACC;// read the CRC check value
```

Using MPLAB® Code Configurator (MCC) for CRC and Memory Scan Modules

The MPLAB® Code Configurator, which is a plug-in tool for MPLAB X IDE, generates the drivers for controlling and driving the CRC and Memory Scan modules based on the settings and selections made in the GUI, as shown in Figure 2.

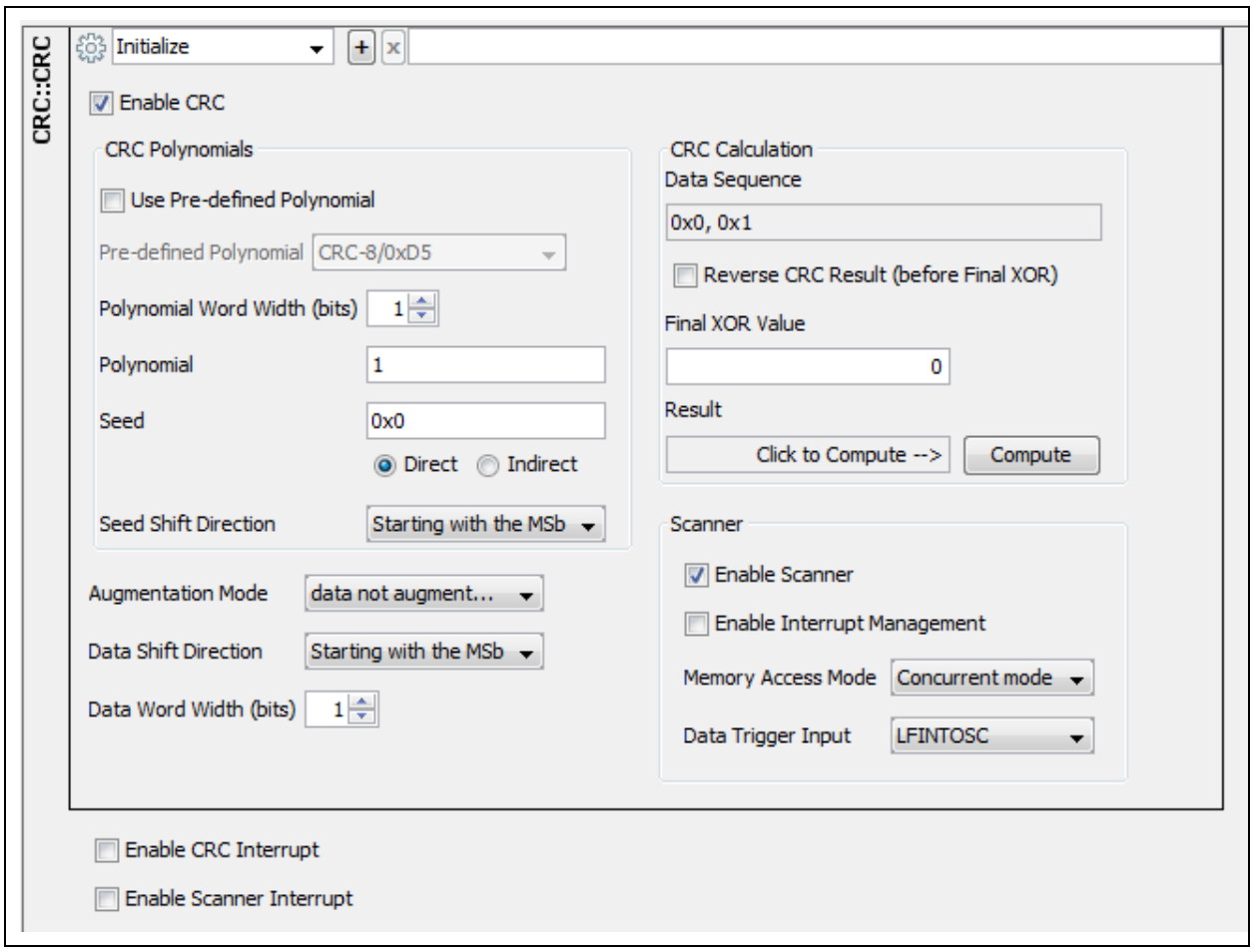
After clicking the Generate Code button, the project in MPLAB X generates all the APIs for CRC and memory scan as listed in the below Table 2:

TABLE 2: LIST OF MCC APIs FOR CRC AND MEMORY SCAN

Function	Description
void CRC_Initialize(void)	Initializes the CRC as per settings done in the MCC.
void CRC_Start(void)	Sets the CRCGO bit of the CRCCON0 register to begin the shifting process.
bool CRC_8BitDataWrite(uint8_t data)	Writes data into CRCDATHL register pair.
uint16_t CRC_CalculatedResultGet(bool reverse, uint16_t xorValue)	Reads and returns the normal or reverse value.
bool CRC_IsBusy(void)	Returns the status of the BUSY bit of the CRCCON0 register to check CRC calculation is over or not.
void CRC_SCAN_StartScanner(void)	Starts the scanning process.
void CRC_SCAN_StopScanner(void)	Stops the scanning process.
void CRC_SCAN_SetAddressLimit(uint16_t startAddr,uint16_t endAddr)	Loads the address limits into the SCANLADRH/L and SCANHADRH/L register pairs.
bool CRC_SCAN_HasInvalidAddressOccured(void)	Checks the occurrence of invalid address in scanning process.
bool CRC_SCAN_IsScannerBusy(void)	Returns the status of BUSY bit of SCANCON0 register.
bool CRC_SCAN_HasScanCompleted(void)	Returns the status of the SCANIF interrupt flag.

Note 1: For the latest version of the MCC GUI for CRC, visit Microchip's web site.

FIGURE 2: MPLAB® CODE CONFIGURATOR (MCC) FOR CRC AND MEMORY SCAN MODULES



Conclusion

The CRC can be used to detect the errors in the data transmission in various digital communication systems. Most of the popular communication protocols like USB, Modbus, CAN and Ethernet employ CRC for error detection. The CRC along with the Memory Scan peripheral is useful while performing the memory tests required in the IEC 60730 standard to support the Class B certification. This technical brief covers the CRC peripheral on 8-bit PIC microcontrollers. It also provides the usage of the Memory Scan module in conjunction with CRC and its configuration.

APPENDIX A: EXAMPLE REGISTER SUMMARY FOR CRC AND MEMORY SCAN

TABLE A-1: SUMMARY OF REGISTERS ASSOCIATED WITH CRC AND MEMORY SCAN MODULES

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CRCACCH	ACC<15:8>							
CRCACCL	ACC<7:0>							
CRCCON0	$\overline{EN}$	CARGO	BUSY	ACCM	—	—	SHIFTM	FULL
CRCCON1	DLEN<3:0>				PLEN<3:0>			
CRCDATH	DATA<15:8>							
CRCDATL	DATA<7:0>							
CRCSHIFTH	SHIFT<15:8>							
CRCSHIFTL	SHIFT<7:0>							
CRCXORH	X<15:8>							
CRCXORL	X<7:1>							—
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF
PIR4	SCANIF	CRCIF	SMT2PWAIF	SMT2PRAIF	SMT2IF	SMT1PWAIF	SMT1PRAIF	SMT1IF
PIE4	SCANIE	CRCIE	SMT2PWAIE	SMT2PRAIE	SMT2IE	SMT1PWAIE	SMT1PRAIE	SMT1IE
SCANCON0	EN	SCANGO	BUSY	INVALID	INTM	—	MODE<1:0>	
SCANHADRH	HADR<15:8>							
SCANHADRL	HADR<7:0>							
SCANLADRH	LADR<15:8>							
SCANLADRL	LADR<7:0>							
SCANTRIG	—	—	—	—	—	—	TSEL<1:0>	

Legend: — = Unimplemented location, read as '0'. Shaded cells are not used by the Timer0 module.

* Page provides register information.

APPENDIX B: CONVERSION OF SEED IN NON-DIRECT MODE OF CRC

If Non-Direct mode for CRC seed is used, the user can pre-convert the seed value and directly load it into the CRCACC<15:0> registers to reduce the time taken for calculations.

For example, in SDLC (CCITT) standard, the initial seed value used in direct algorithm is 0xFFFF. This can be pre-converted to a 0x84CF using the code snippet:

Code snippet for converting from direct algorithm seed values to non-direct algorithm seed values, as shown in Example B-1.

EXAMPLE B-1: CONVERTING DIRECT ALGORITHM SEED VALUES TO NON-DIRECT ALGORITHM SEED VALUES

```
crcinit_direct = crcinit;
crc = crcinit;
for (i=0; i<order; i++) //order of CRC polynomial e.g. for CCITT order = 16
{
    bit = crc & 1;
    if (bit) crc^= polynom;
    crc >>= 1;
    if (bit) crc|= crchighbit;//crchighbit for 16 bit CRC polynomial= 0x8000
}
crcinit_nondirect = crc;
```

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