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DCR-Based Droop Current Sharing Method Applied to the MCP16502 PMIC

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INTRODUCTION

This application note demonstrates the feasibility and performance of a DCR-based droop current sharing technique applied to two Buck channels of the MCP16502 PMIC using the inductor's DCR as a current sensing element. A detailed design procedure is illustrated, corroborated by statistics based on production data. Experimental measurements are also provided.

PMICs are often regarded as special purpose devices, tied to a particular processor, FPGA, or other digital loads, and therefore they are seldom used outside their originally targeted application.

One of the most frequent hurdles to expanding the market for a given PMIC is the limited individual current capability of the Buck channels the PMIC was designed with. In some cases it may be desirable to increase the current capability by paralleling two (or more) Buck channels such that larger loads can be supported. For this reason, many PMICs in the industry are designed to natively support the parallel combination of Buck channels, either through multi-phase techniques or, for smaller total load currents, through directly paralleled power stages.

This application note will demonstrate how, with the use of a suitable inductor and a few inexpensive external components, even a PMIC which is NOT natively designed for Buck channel paralleling such as the MCP16502, can parallel two Buck channels to support larger load currents using a DCR-based droop current sharing method provided that:

1. The targeted load voltage range is wide enough to accommodate the "load line" slope required.
2. The voltage setting accuracy and matching of the Buck channels is adequate to support the needed accuracy of the output voltage, i.e., it is a small fraction of the load voltage range.

DROOP CURRENT SHARING METHOD

The droop method for implementing current sharing among paralleled power supplies is well known in the industry, [1] and [2]. The droop-share method artificially increases the output impedance of each paralleled Buck channel such that as the total load current increases, the different units will share the load thanks to a predictable and finite load regulation characteristic. Figure 1 illustrates the basic principle of droop-based current sharing. The factors governing the accuracy of the current sharing are thoroughly analyzed in [2].

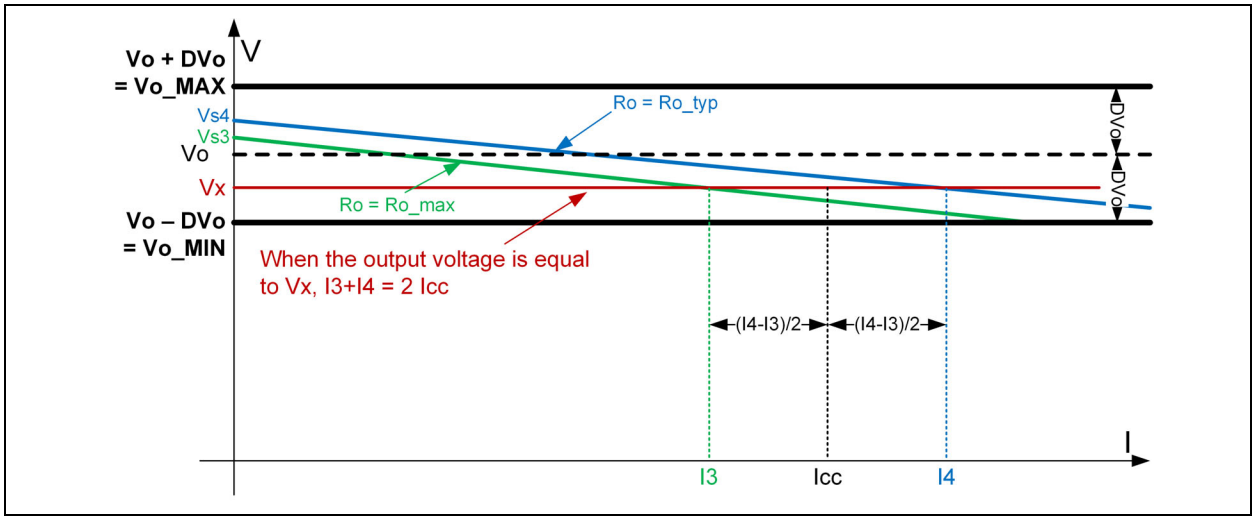


FIGURE 1: *Principle of Droop Current Sharing Method.*

In Figure 1, the boundaries $V_O + DV_O = V_{O\_MAX}$ and $V_O - DV_O = V_{O\_MIN}$ represent the upper and lower limits of the load voltage range respectively. Those limits are typically symmetrical with respect to the nominal value for the output voltage of V_O.

The no-load output voltages, V_{SX} of the respective Buck channels, must be within the V_{O_MAX} and V_{O_MIN} boundaries. As the Buck3 and Buck4 channels of the MCP16502AB (or MCP16502AD) will be used for this example, those have been designated as Vs3 and Vs4 respectively. Since the output voltage accuracy of each Buck channel has its own tolerance, a tighter voltage tolerance specification facilitates the task of staying within the operating condition limits.

If $V_S + DV_S = V_{S\_MAX}$ is the upper (i.e. MAX) limit of the output voltage accuracy specification, the condition of Equation 1 must be satisfied:

EQUATION 1:

$$V_{S\_MAX} < V_{O\_MAX} - dV_{OVS}$$

Additional margin for accommodating residual voltage overshoot, dV_{OVS} (see Figure 10 for definition), upon abrupt load releases should be considered since the programmed output impedance characteristic may not be perfectly flat over the frequency range of interest for the load current [3]. Once the nominal V_S is selected, the load line slope must be selected such that at full load, the output voltage is above the minimum of the load voltage range.

In the case of a single channel supporting the maximum load current, I_{CC}, this condition is simply stated as shown in Equation 2 where $V_S - DV_S = V_{S\_MIN}$ is the lower limit (i.e. MIN) of the output voltage accuracy specification.

EQUATION 2:

$$V_{S\_MIN} - R_O \times I_{CC} > V_{O\_MIN} + dV_{UNS}$$

R_O is a generic load line slope having the same units of resistance as a resistor, Ohms (Ω). R_O may also be affected by some tolerance and temperature coefficient, depending on the current sensor chosen for the application. Also, in the case of Equation 2, some extra margin must be taken for accommodating some residual voltage undershoot (dV_{UNS}, also see Figure 10 for definition) upon abrupt load steps. The margins for undershoot and overshoot do not need to be the same. If the load change dynamics are slow, they can be neglected.

If two channels are connected in parallel to support a total output current of 2 x I_{CC}, the accuracy of the current sharing is determined by the differences between their V_S values and by the load line slopes, which may be either convergent or divergent such as those shown in Figure 1. This yields a difference (I4 - I3) in the values of the respective currents at the output voltage V_X where the required total output current 2 x I_{CC} is reached.

It should be noted that since the Buck channels (Buck3 and Buck4) belong to the same device, it is reasonable to expect that the Vs difference (voltage mismatch, dV_S) would be better than the output voltage accuracy data sheet specification. This is because the reference voltages for Buck3 and Buck4 regulation loops are derived from the same physical bandgap reference cell. Indeed, it will be shown using statistics from production data that the voltage mismatch is significantly tighter.

It is generally more difficult to make assumptions on the R_O difference. If current sense resistors are used, their tolerance can be as good as 1% but they come with increased cost and conduction losses. Recently specialized inductor families where the DCR is accurately controlled have become available for current sensing applications (5%, with 3% tolerance available). In that case, the well-known loss-less DCR current sensing method represents an attractive alternative because only a handful of inexpensive passives are required to implement the sharing circuit.

For inductor families which are not purpose-built for DCR current sensing, the one-sided MAX to TYP tolerance of the DCR is a good indicator of the production process spread. Some inductor manufacturers may even share internal data on the DCR spread in production if those are not stated in the data sheet. Moreover, if the load line slope is only used for current sharing purposes, DCR temperature compensation [4] may not be necessary. For this experiment inductor DCR sensing without temperature compensation is used, a conceptual application schematic is shown by Figure 2. Also, Buck3 and Buck4 must always be operated in forced PWM mode (FPWM) such that a constant switching frequency is maintained across the entire load range.

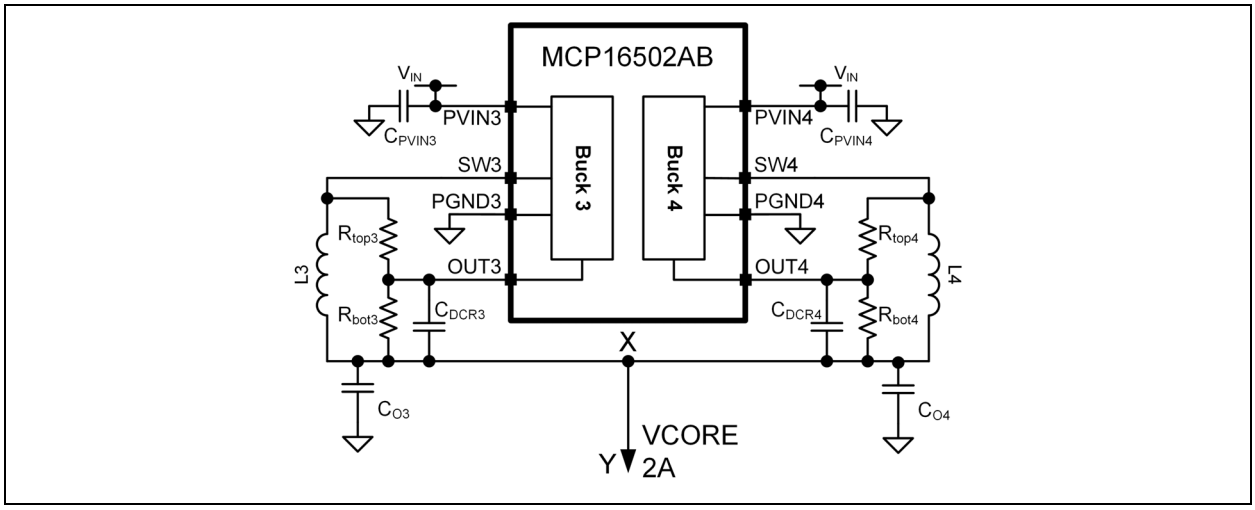


FIGURE 2: *Conceptual Arrangement of Buck3 and Buck4 Paralleled with DCR-Based Droop Current Sharing Method.*

DCR-BASED DROOP CURRENT SHARING DESIGN PROCEDURE

The design procedure always starts by considering the amplitude of the allowable load voltage range. If this amplitude is not significantly wider than the band determined by the output voltage accuracy of the power supply, the procedure either fails (i.e. once Equation 1 is satisfied, it is impossible to also satisfy Equation 2 with some positive R_O value) or the resulting load line slope, R_O, will be insufficient to ensure a reasonable amount of current sharing between the paralleled channels.

The output voltage accuracy specification of Buck2, 3, and 4 of the MCP16502 is ±1% over temperature in the output voltage range 0.9V to 1.3V, and ±1.5% over temperature outside that range. This excellent specification allows the applicability of the droop-based current sharing method using Buck3 and Buck4 in parallel to a wide variety of digital cores (e.g. https://www.socionext.com/en/download/gcc/ds-SC1701BK3-BH5-100-10N-rev1-2.pdf where core currents up to 1.8A can be expected).

The design steps are summarized below:

1. Position the no-load voltage towards the upper limit of the allowable load voltage range, with adequate design margin to accommodate some amount of residual voltage overshoot at load release, dV_{OVS}. For estimation of dV_{OVS}, a good criterion is to rely on the MCP16502 data sheet Typical Performance Curves, keeping in mind that the load-line slope will also help in reducing the overall peak-to-peak voltage deviation upon load steps/releases. This design step leads to the selection of the Vs voltage using Equation 3.

EQUATION 3:

$$V_{S\_MAX} = V_S(1 + tol) < V_{O\_MAX} - dV_{OVS}$$

Where tol is the absolute value of the output voltage accuracy specification i.e. 1% (0.01) or 1.5% (0.015), depending on which range the Vs voltage falls into. Then by rearranging Equation 3 we get Equation 4:

EQUATION 4:

$$V_S = (V_{O\_MAX} - dV_{OVS})/(1 + tol)$$

With V_{O_MAX} = 1.32V, tol = 0.01, and dV_{OVS} = 10 mV, it is found that V_S can't be greater than 1.297V. The output voltage setting for Buck3 and Buck4 in the MCP16502 is in 25 mV steps, thus the closest available voltage setting is V_S = 1.275V. This value is consistent with the assumption of 1% tolerance, as it falls in the range 0.9V to 1.3V.

Note that 1.275V is not the default voltage setting for Buck3 and Buck4 of the MCP16502AB or MCP16502AD. To achieve this voltage setting, registers OUT3-A and OUT4-A (assuming only Active power state is used) must be loaded with the corresponding VSET[5:0] code prior to initiating power delivery. If this is not possible in the end user system, the creation of a dedicated part number with the appropriate default voltage setting can be considered by contacting the nearest Microchip Sales Office.

2. At the maximum expected inductor temperature T_{MAX}, determine the maximum acceptable load line slope for the combined channels. It is reasonable to assume that the inductor temperature rise will be 20°C

or less above ambient using a suitable inductor. This can be verified once the target inductor is selected. Thus:

EQUATION 5:

$$V_{S\_MIN} - R_{O\_MAX\_Troom} \times (1 + T_C \times (T_{MAX} - T_{room}))2I_{CC} > V_{O\_MIN} + dV_{UNS}$$

The maximum allowable load line slope at room temperature is:

EQUATION 6:

$$R_{O\_MAX\_Troom} = (V_{S\_MIN} - V_{O\_MIN} - dV_{UNS}) / (2I_{CC} \times (1 + T_C \times (T_{MAX} - T_{room})))$$

Where:

- $R_{O\_MAX\_Troom}$ is the maximum load line slope at room temperature
- T_C is the temperature coefficient of copper (0.00393/°C)
- T_{ROOM} = 25°C
- T_{MAX} = maximum ambient temperature (105°C) + 20°C = 125°C
- dV_{UNS} = margin for undershoot = 10 mV

Therefore, $R_{O\_MAX\_Troom}$ = 18.8 mΩ

Note that due to parallel operation, the load-line slope (output resistance) of the two channels combined is one-half of the programmed output resistance of each individual channel.

3. Choose an inductor with suitable ratings and DCR and calculate the DCR sensing components.

Since the feedback pins OUT3, OUT4 of the MCP16502 are single-ended and referred to the SGND pin, the resulting feedback signal with DCR sensing will combine several contributions, which consist of:

a) the voltage across the load (which may not be in the immediate vicinity of the MCP16502);

b) the DCR drop (or a fraction of it, if a divider is used as in Figure 2);

c) the drop from the load negative terminal to the SGND pin; and

d) the drop from the common inductors' connection point to the load positive terminal, i.e., the drop across the copper trace resistance from points X to Y in Figure 2.

Contributions a) and b) are the intended ones. Contribution c) can be eliminated by star-routing the SGND net to the load negative terminal, but due to the fact that the inductors must be placed in close proximity of the MCP16502 for well-known reasons (e.g. to minimize the switching noise due to the high dV/dt of the SW nets), contribution d) cannot be completely eliminated. It can be minimized with a suitable layout but not reduced to zero like contribution c).

Therefore, some reduction factor must be accounted for in the calculation of the inductor DCR from the $R_{O\_MAX\_Troom}$, and later verified against the real layout.

Also note that due to parallel operation, the load-line slope (output resistance) of the two channels combined is one-half of the programmed output resistance of each individual channel. The maximum load-line slope for each individual channel is found using Equation 7:

EQUATION 7:

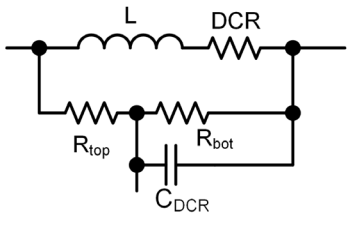
$$R_{oDCR\_MAX\_Troom} = 2 \times factor \times R_{O\_MAX\_Troom}$$

Where:

- factor is the reduction factor (assumed 0.95)

This calculates to $R_{oDCR\_max\_Troom}$ = 35.6 mΩ

It is generally very easy to find a suitable inductor to meet this requirement with maximum DCR greater than or equal to $R_{oDCR\_max\_Troom}$. In most cases, the maximum DCR of the inductor will be larger than $R_{oDCR\_max\_Troom}$. This can be solved by introducing an attenuation with external resistors, R_{top} and R_{bot} into the feedback path. Since their power dissipation is very small, these resistors can be small form factor to save PCB space. The resulting schematic is shown in Figure 3.



$R_{oDCR} = DCR \cdot R_{bot} / (R_{top} + R_{bot})$

FIGURE 3: *DCR Signal Attenuation and Sensing Components R_{bot}, R_{top}, C_{DCR}.*

For experimental verification, an 1.5 µH inductor, SPM3015T-1R5M-LR from TDK, was chosen due to its low yet adequate DCR and reasonably tight MAX-to-TYP accuracy (MAX = 1.1 x TYP). This is found from the specification as DCR_max = 62.4 mΩ and DCR_typ = 56.7 mΩ at room temperature with more than adequate current handling. This allows us to calculate the required DCR attenuation, att_DCR using Equation 8 as att_DCR = 0.571.

EQUATION 8:

$$att\_DCR = R_{oDCR\_MAX\_Troom} / DCR\_max$$

In the selection of R_{top}, R_{bot}, and C_{DCR} keep in mind that the OUTx pins of the MCP16502 are also connected to the internal feedback divider, whose typical resistance to ground is 1.5 MΩ. With a low enough impedance level of the DCR sensing components, the loading effect caused by the internal feedback divider can be neglected.

Choosing R_{top} = 470Ω (standard value), we then use Equation 9 to calculate R_{bot} = 625.7Ω.

EQUATION 9:

$$R_{bot} = R_{top} \times att\_DCR / (1 - att\_DCR)$$

Choosing the closest E24 series standard value of R_{bot} = 620Ω, we get att_DCR = 0.569.

Since the only purpose of the load-line slope is to achieve current sharing, and Equation 6 is calculated in the upper temperature extreme, the temperature compensation techniques mentioned in [4] can be disregarded, and R_{bot} becomes just a simple resistor. Later it will be shown that at cold temperature, where the load-line slope is the shallowest, the current sharing performance is still acceptable.

From [4], it is known that if the time constant, C_{DCR} R_{top} R_{bot} / (R_{top} + R_{bot}), is much longer than the switching period, the slope and the peak-to-peak excursion of the voltage across the C_{DCR} capacitor is not affected by the presence of R_{bot}, but only depends on R_{top} and C_{DCR}. On the other hand, the DC and low-frequency components of the DCR drop appearing across C_{DCR} are indeed attenuated by a factor $R_{bot}/(R_{top} + R_{bot})$.
To maintain the same peak-to-peak/average ratio of the DCR voltage drop caused by the inductor current across C_{DCR}, it is necessary to choose the C_{DCR} capacitor using Equation 10.

EQUATION 10:

$$C_{DCR} \times R_{top} \times R_{bot} / (R_{top} + R_{bot}) = L/DCR$$

In other words, the parallel combination of R_{top} and R_{bot} should be included when calculating the time constant equality. From the above, C_{DCR} is calculated to = 99 nF so a standard value of 100 nF was used.

It has been shown [5] that the selection of C_{DCR} beyond the value calculated from Equation 10 (aka "overtuning") yields a lower output impedance at high frequencies than the static load-line slope and therefore helps in diminishing the voltage undershoot/overshoot upon load steps/releases. As such, the value of C_{DCR} could be increased to cope with the DCR increase at high temperature.

4. Verify that the current sharing is acceptable at the minimum inductor operating temperature using output voltage accuracy mismatch data.

The output voltage mismatch, dV_S, between Buck3 and Buck4 was evaluated from production data of the MCP16502AB at different temperatures. Data at -40°C is most important because this is the temperature extreme at which the inductor DCR, and thus the load-line slope, will be the smallest. The results are summarized in Table 1.

TABLE 1: %-MISMATCH OF BUCK4 VS. BUCK3

[V(OUT4)-V(OUT3)]\ [V(OUT4)+V(OUT3)] in %	Temperature		
	-40°C	25°C	125°C
Average	0.022%	0.002%	0.006%
Std. Dev. (Sigma)	0.029%	0.037%	0.042%
MAX (Average + 6 Sigma)	0.194%	0.226%	0.259%
MIN (Average - 6 Sigma)	-0.150%	-0.222%	-0.246%

With some additional margin, a ±0.25% mismatch can be assumed at -40°C.

Regarding the DCR mismatch, in lieu of using the actual manufacturer's data, the MAX - TYP difference is from the data sheet can be used. Referring to Figure 1, and neglecting the small error due to the voltage drop in the X-Y path, the worst-case current mismatch can be calculated at the minimum temperature, Tmin, using Equation 11 as:

EQUATION 11:

$$\frac{I_4 - I_3}{I_4 + I_3} = \frac{I_4 - I_3}{2I_{CC}} = \frac{dV_S}{I_{CC}(R_{o\_max} + R_{o\_typ})} + \frac{R_{o\_max} - R_{o\_typ}}{R_{o\_max} + R_{o\_typ}}$$

Where:

R_{o_typ} = att_DCR · DCR_TYP · [1 + T_C (T_{min}-T_{room})]

R_{o_max} = att_DCR · DCR_MAX · [1 + T_C (T_{min}-T_{room})]

And with:

- T_C is the temperature coefficient of copper (0.00393 /°C)
- T_{room} = 25°C
- T_{min} = minimum ambient temperature = -40°C
- I_{CC} = 1A

The following can be calculated:

(I4 - I3)/(2 I_{CC}) = 0.124;

I4 = 1.124 A;

I3 = 0.876 A

The worst-case current mismatch at -40°C while supporting the maximum load current (2 * I_{CC} = 2 A) is only 12.4%.

PROTOTYPE BUILD

To verify the procedure, a board was built and tested; Figure 4 shows the schematic of the relevant portion. In the layout, care has been taken in eliminating ground shifts by star-connecting the SGND plane in proximity of the point-of-load ground return. The board allows for direct probing of the voltage drop across the C_{DCR} capacitors C19 and C21 respectively for Buck3 and Buck4 at headers J33 and J34. The pinout arrangement of Buck3 and Buck4 facilitates a highly symmetric layout.

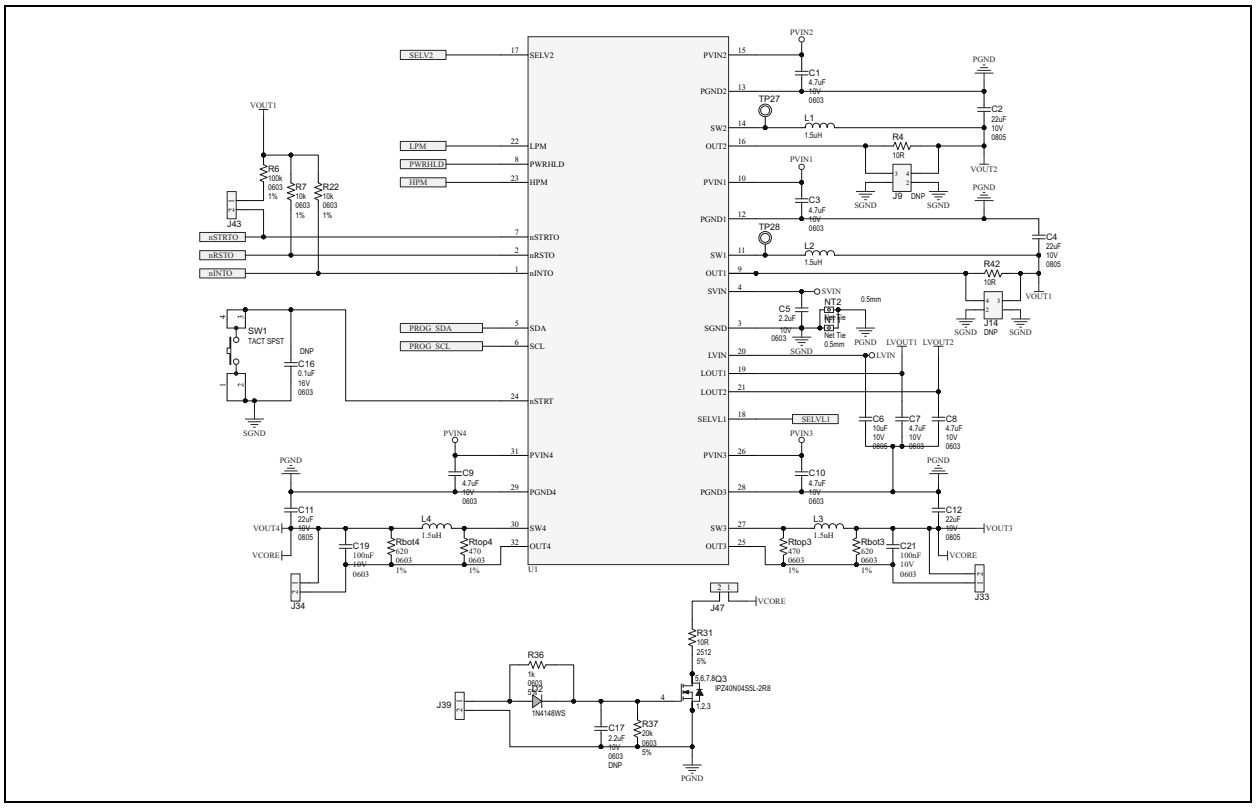


FIGURE 4: *Prototype Schematic.*

EXPERIMENTAL VERIFICATION

The current sharing performance was indirectly measured as the voltage drop at J33 and J34 in Figure 4, since the addition of current sensing wire loops may degrade the performance significantly.

The effective DCR was measured with the inductors soldered on the board by forcing 1A through inductors L3 and L4, resulting in DCR measurements at room temperature of 60.0 mΩ for L3 and 60.4 mΩ for L4 respectively.

Figure 5 shows the voltage drop across the C_{DCR} capacitors for Buck3 (VJ33) and Buck4 (VJ34) as a function of the total load current (V_{CORE} current), up to 2.5A, using a pulsed measurement method that minimizes inductor self-heating.

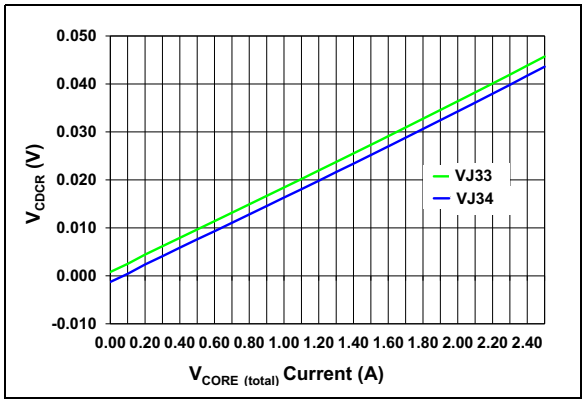


FIGURE 5: *Voltage Drop across C_{DCR} Capacitors for Buck3 (VJ33) and Buck4 (VJ34) vs. V_{CORE} Current.*

Figure 6 shows the V_{CORE} voltage as a function of load current, revealing the load-line slope. The linear interpolation shows that its linearity is nearly perfect. The parasitic resistance equivalent to the X-Y track segment in Figure 2 has been estimated from the layout at about 1.6 mΩ. Using this estimation and the measured DCR values, the design calculations would predict a V_{CORE} load line slope of 19 mΩ. Measurements yield a load line slope of 20 mΩ, which is in excellent agreement.

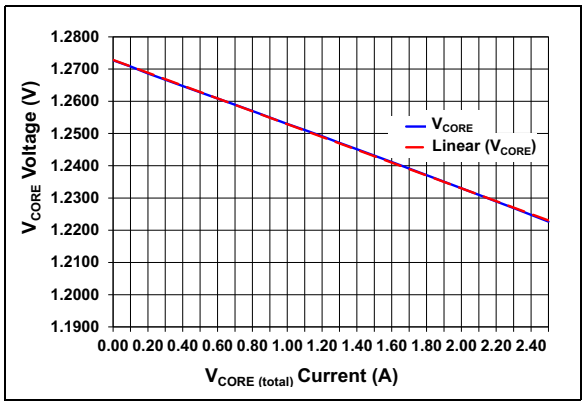


FIGURE 6: *V_{CORE} Load-Line Slope.*

Steady-state waveforms of the voltages at J33 and J34 at 2A total load are shown in the Figure 7 scope shot. The 180° phase shift between Buck3 and Buck4 can be seen. This results in a smaller output current and voltage ripple, just like in a dual-phase Buck configuration [6]. The small voltage offset between VJ33 and VJ34, which can be observed in Figure 5, is also clearly visible in the scope shot.

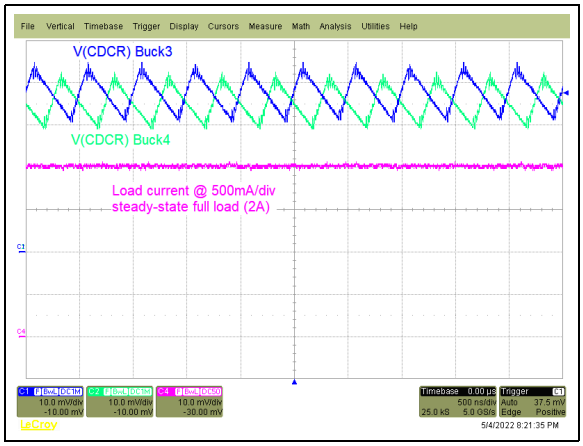


FIGURE 7: *Steady-State Waveforms at 2A Load on V_{CORE}.*

Load step and release transients from/to 25% (500 mA - Figure 8) and to/from 75% (1.5A - Figure 9) were first taken using an electronic load. The output voltage was measured with a differential probe since the scope ground was referred to point X in Figure 2. Some small amount of undershoot and overshoot is visible, indicating that the output impedance is not perfectly flat [5]. After the undershoot/overshoot is settled, the measured output voltage excursion for a 1A load change is very close to 20 mV, which is - once again - in excellent agreement with the expected load-line slope.

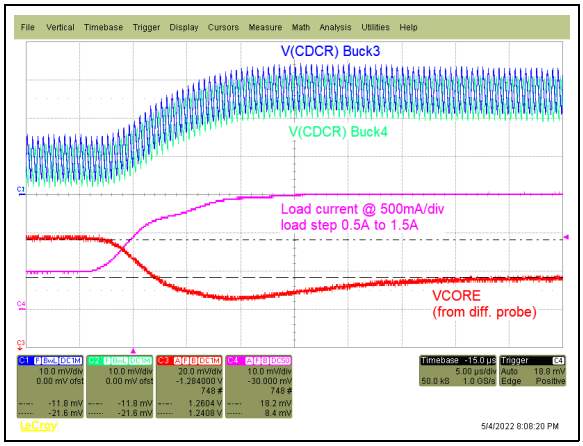


FIGURE 8: *1A Load Step (500 mA to 1.5A).*

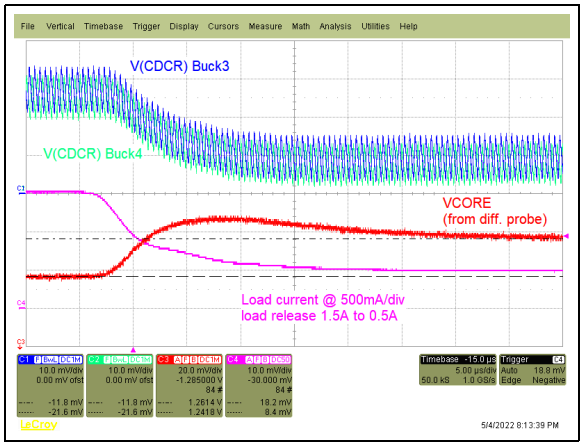


FIGURE 9: *1A Load Release (1.5A to 500 mA).*

Additional load transient testing was executed with a MOSFET-switched load resistor (0.91Ω), which yields a much faster current rise/fall time and reveals the less-than-perfect output impedance flatness in the higher frequency range, see Figure 10. As anticipated previously, by "over-tuning" the time constant of the DCR drop readout circuit, a lower high-frequency output impedance can be obtained. This yields a slightly lower yet noticeable undershoot/overshoot, see Figure 11.

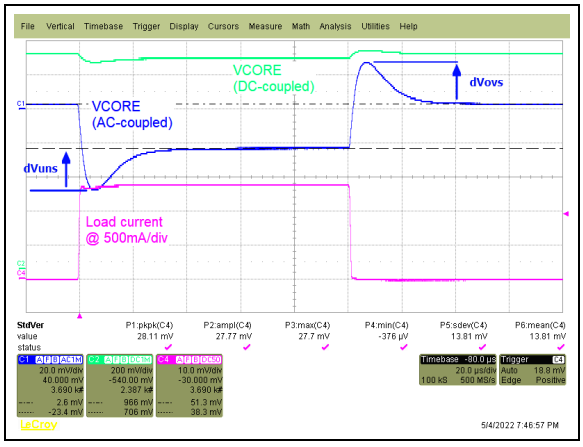


FIGURE 10: *Fast-Changing Load Transient Response, C_{DCR} = 100 nF (Perfectly Tuned Time Constant).*

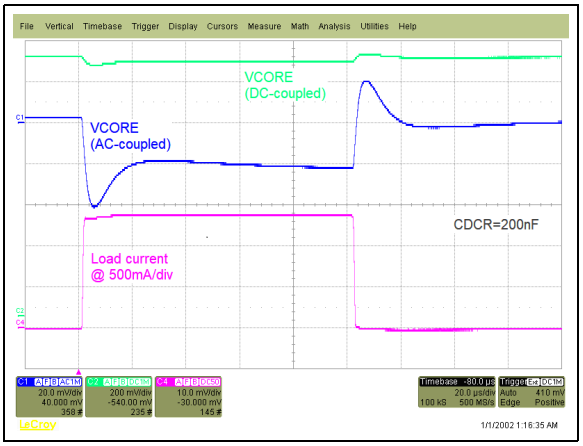


FIGURE 11: *Fast-Changing Load Transient Response, C_{DCR} = 200 nF ("Overtuned" Time Constant).*

Start-up is well behaved, with and without load, as seen in Figure 12 and Figure 13. This is because during execution of the soft-start ramp, the voltage references for the two Buck channels are generated by DACs which are clocked synchronously from the same logic and time base.

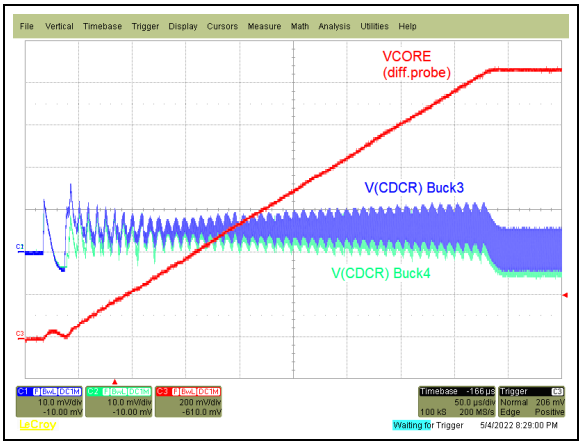


FIGURE 12: *V_{CORE} Start-Up - No Load.*

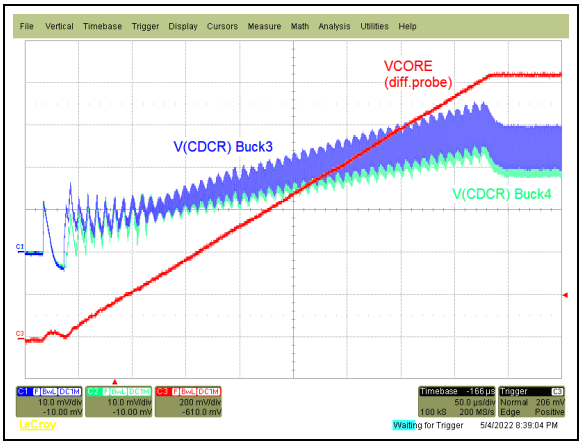


FIGURE 13: *V_{CORE} Start-Up, Load Resistance 0.91Ω.*

The conversion efficiency of the Buck3 and Buck4 power stages combined was evaluated as is shown in Figure 14. The input power for efficiency measurement is the total power entering the pins PVIN3 and PVIN4 only. The efficiency peaks at around 86.5% at a load current of 700 mA.

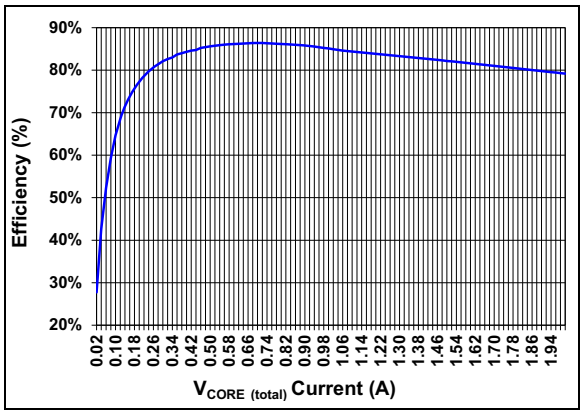


FIGURE 14: *Combined Buck3/Buck4 Power Conversion Efficiency, 5V Input, 1.275V Output Voltage Setting.*

The turn-off behavior in Figure 15 reveals the presence of the Active Discharge switches connected directly at OUT3 and OUT4. While the voltage spike is not harmful, it should be noted that the R_{bot} resistor is now connected in series in the output discharge path. As R_{bot} is generally much higher than the Active Discharge Resistance (25Ω typical value), the output discharge time is therefore significantly increased. If needed, some external tweaks can be adopted to circumvent this effect (e.g. a small diode in parallel with R_{bot} where the cathode is connected to the respective OUTx pin).

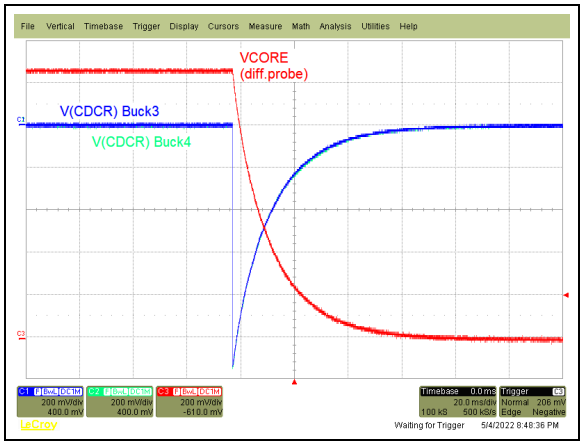


FIGURE 15: *Turn-Off Transient.*

Finally, the behavior in Hiccup-mode short circuit protection was investigated by setting the HCPEN bit for both Buck3 and Buck4, and then applying an overload (about 170 mΩ). If HCPEN='1' for a given Buck channel, a short circuit/overload event on that channel will cause a Hiccup mode response with unlimited soft-start retries, without shutting down the other channels and invoking another start-up sequence after 100 ms.

Like any other parameter, the High-side Peak Current Limit (I_{LIM_HSx}) value reported in the data sheet EC Table may exhibit some channel-to-channel mismatch. As a result, between the paralleled channels, one may enter Hiccup-mode protection before the other when their common output is overloaded. As soon as the first one enters Hiccup, the entire load current is diverted in the second channel, thus also driving it into hiccup. Since the Hiccup Wait Time (t_{HICCUP}) is generated precisely by a digital counter, the first channel entering Hiccup will also be the first initiating the subsequent soft-start retry. This can be seen in Figure 16, where Buck4 is the first channel entering Hiccup and initiating the retry soft-start ramp.

Different than Figure 12 and Figure 13, where the soft-start ramps of both channels begin at exactly the same time instant and some small offset in the voltage control loop causes the trace measured at J33 (VJ33 for Buck3) to be slightly above than the trace measured at J34 (VJ34 for Buck4), in Figure 16, the situation is reversed (VJ34 is above VJ33) because the soft-start ramp for Buck4 starts a bit before the ramp of Buck3. Still, even during this abnormal overload event, the resulting current sharing is good. Notably, if HCPEN='0' on either paralleled channel, the following automatic start-up sequence would release both soft-start ramps at exactly the same instant.

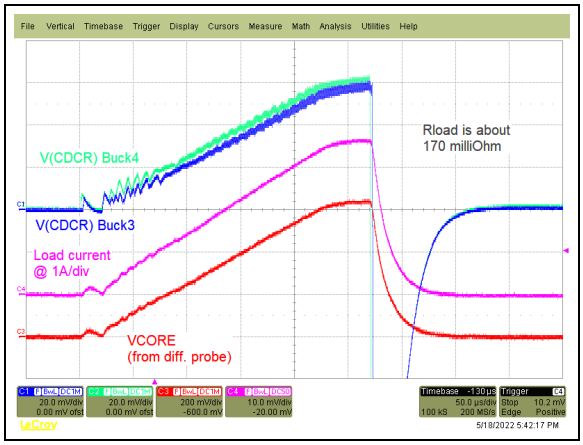


FIGURE 16: *Hiccup-Mode Short Circuit Protection Soft-Start Retry (HCPEN='1' for Buck3 and Buck4).*

CONCLUSIONS

A procedure for the implementation of droop-based current sharing method with DCR current sensing has been provided and evaluated on the MCP16502AB using a dedicated board.

The analysis of production data taken at different temperatures reveals that the matching of the output voltage for Buck stages belonging to the same unit in the MCP16502AB is significantly better that the output voltage accuracy specification which must consider the reference voltage variation across different units. This finding results in an improved and more realistic estimation of the achievable current sharing accuracy.

When the allowable load voltage range is sufficiently wide, and the inductor DCR tolerance is adequate, this method can be used to combine Buck3 and Buck4 in parallel, so that applications requiring load currents up to 2A can be covered.

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