

Using SDRAM on AT91SAM7SE Microcontrollers

1. Scope

The Atmel® AT91SAM7SE Series ARM®Thumb®-based microcontroller family features an ASB high-performance SDRAM controller for connecting 16-bit or 32-bit wide external SDRAM memories.

The purpose of this document is to help the developer in the design of a system using SDRAM memories. It describes the performance characteristics of the SDRAM controller and associated techniques to optimize SDRAM performance and power consumption.

The associated zip file, ***AN-SDRAM_SAM7SE_software_example.zip***, contains the elements required in [Section 7.4 "Software Initialization Example" on page 11](#).

2. SDRAM Controller Overview

The SDRAM Controller (SDRAMC) extends the memory capabilities of a chip by providing the interface to an external 16-bit or 32-bit SDRAM device. The page size ranges from 2048 to 8192 and the number of columns from 256 to 2048. It supports byte (8-bit), half-word (16-bit) and word (32-bit) single accesses.

The SDRAM Controller supports a read or write burst length of one location. It does not support byte read/write bursts or half-word write bursts. It keeps track of the active row in each bank, thus maximizing SDRAM performance, e.g., the application may be placed in one bank and data in the other banks. So as to optimize performance, it is advisable to avoid accessing different rows in the same bank. (Open Bank Policy).

The SDRAM controller supports a CAS latency of 2.

Self refresh and low power mode features minimize the consumption of the SDRAM device in power down mode.

The SDRAM Controller also supports low-voltage Mobile SDRAM addressing (but does not support low-power consumption extended mode).



AT91 ARM Thumb-based Microcontrollers

Application Note



3. SDRAM Controller Signals Definition

The SDRAM Controller is capable of managing up to four banks of 32-bit wide SDRAM devices. The signals generated by the controller are defined in [Table 3-1](#). Refer to the chapter: “External Bus Interface (EBI)” in the [AT91SAM7SE Series](#) product datasheet for further details.

Table 3-1. SDRAM Controller Signals

Controller Name	Description	Microcontroller Signal	Type	Active Level
SDCK	SDRAM Clock	SDCK	Output	
SDCKE	SDRAM Clock Enable	SDCKE	Output	High
SDCS	SDRAM Controller Chip Select	NCS1/SDCS	Output	Low
BA[1:0]	Bank Select Signals	A17/BA1 A16/BA0	Output	
RAS	Row Signal	RAS	Output	Low
CAS	Column Signal	CAS	Output	Low
SDWE	SDRAM Write Enable	SDWE	Output	Low
NBS[3:0]	Data Mask Enable Signals	A0/NBS0 NWR1/NBS1/CFIOR A1/NB2 NBS3/CFIO	Output	Low
A[9:0]	Address Bus	A[11:2]	Output	
A10	Address Bus	SDA10	Output	
A[12:11]	Address Bus	A[14:13]	Output	
D[31:0]	Data Bus	D[31:0]	I/O	

- **SDCK** is the clock signal that feeds the SDRAM device and to which all the other signals are referenced. All SDRAM input signals are sampled on the positive edge of SDCK.
To reach a speed of 48 MHz on the pin SDCK, loaded with 30 pF equivalent capacitor, a dedicated high speed pin is necessary and so the SDCK pin is not multiplexed with a PIO line (lower frequency). SDCK is tied low after reset.
- **SDCKE** activates (high) and deactivates (low) the SDCK signal. Deactivating the clock provides precharge power down and self refresh operation (all banks idle), active power-down (row active in any bank) or clock suspend operation (burst/access in progress). SDCKE is synchronous except after the device enters power down and self refresh modes, where SDCKE becomes asynchronous until after exiting the same mode. The input buffers, including SDCK, are disabled during power down and self refresh modes, providing low standby power. For more information, refer to the sections “Self-refresh Mode” and “Low-power Mode” in the chapter: “SDRAM Controller (SDRAMC)” in the [product datasheet](#).
- **SDCS**: When the chip select SDCS is low, command input is valid. When high, commands are ignored but the operation continues.
- **RAS, CAS, SDWE**: The row address strobe (RAS), column address strobe (CAS) asserts to indicate that the corresponding address is present on the bus. The conjunction with write enable (SDWE) and chip select (SDCS) at the rising edge of the clock (SDCK) determines the SDRAM operation.
- **BA0, BA1** selects the bank to address when a command is input. Read/write or precharge is applied to the bank selected by BA0 and BA1.

- **NBS[3:0]:** Data is accessed in 8, 16 or 32 bits by means of NBS[3:0] which are respectively, highest to lowest mask bit for the SDRAM data on the bus.
- **A[12:0]:** SDRAM controller address lines are bound, respectively, to [A2:A14] of the microcontroller except for A10 which is not bound to A12. A[12:0] addresses up to 11 columns and 13 rows.
- **SDA10:** Acts as a dedicated SDRAM address line because A10 is used for SDRAM refresh. SDA10 signal allows the system to enable the auto-refresh operation without holding the address bus.

4. SDRAM Connection on AT91SAM7SE Microcontrollers

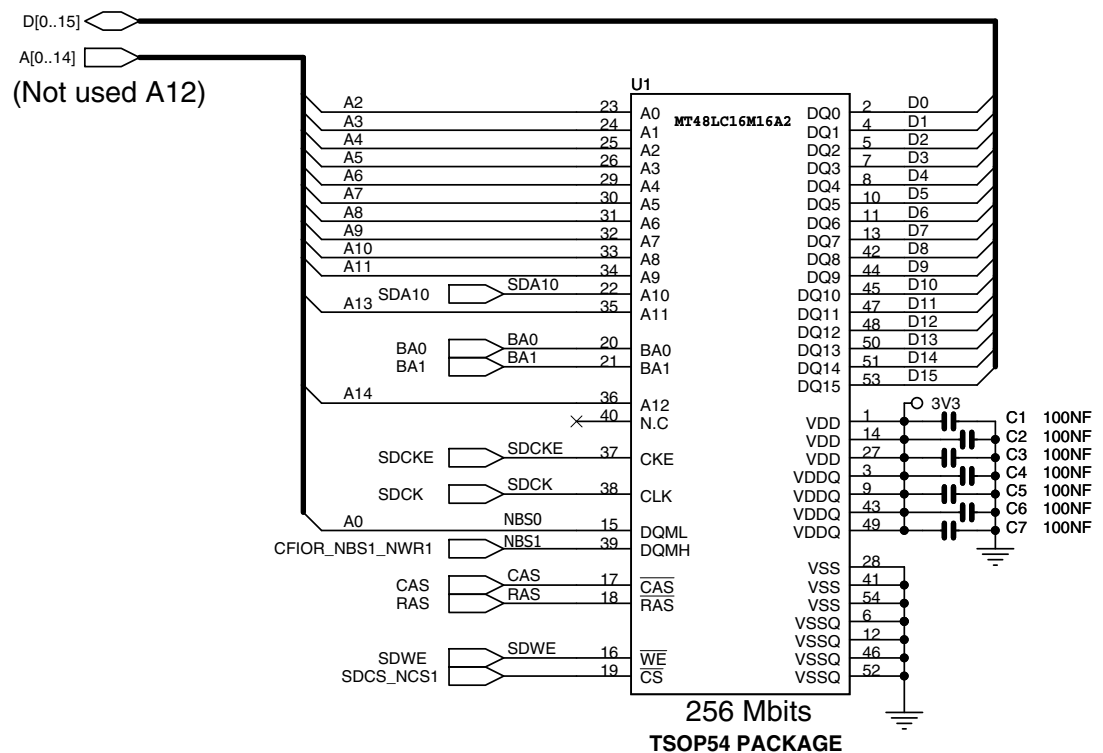
The AT91SAM7SE microcontrollers support 16-bit and 32-bit SDRAM devices on one Chip Select area (NCS1). The bit DW located in the SDRAM configuration register selects 16-bit or 32-bit bus width.

The 32-bit interface can be achieved by a single 32-bit SDRAM device or two 16-bit SDRAM devices.

Each SDRAM device must use sufficient decoupling to provide efficient filtering on the power supply rails as shown in the following sections.

4.1 SDRAM 16-bit Connection

Figure 4-1. 16-bit Hardware Configuration



4.1.1 Software Configuration

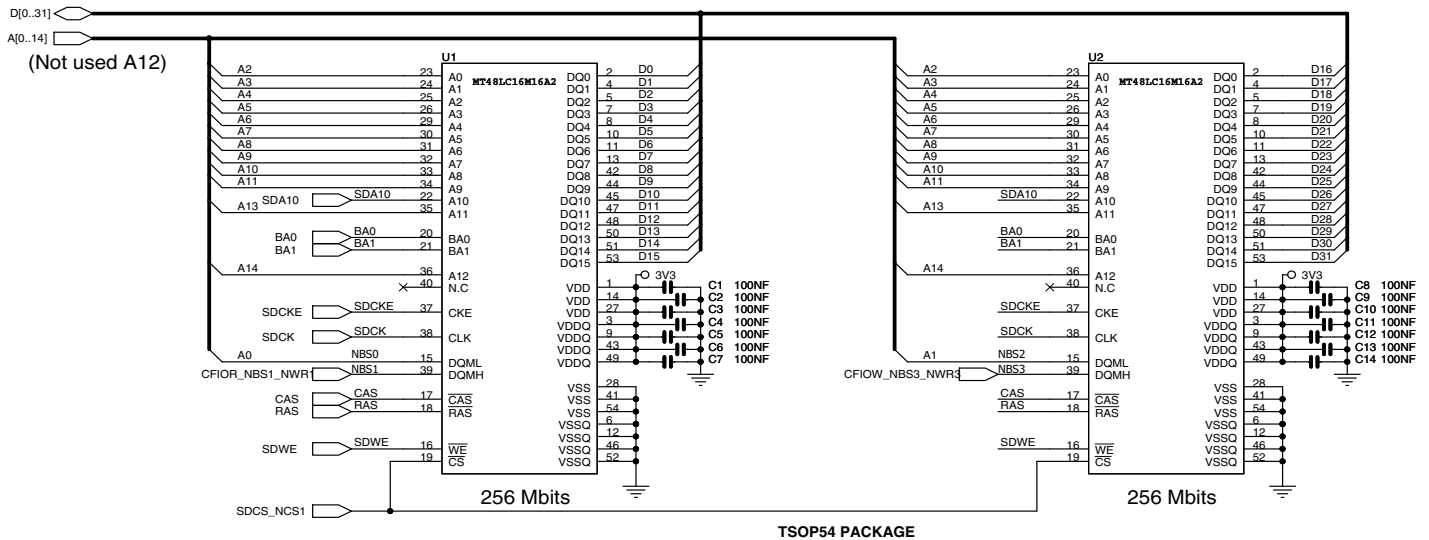
The following configuration must be respected:

- Setup Master clock and PLL clock through Power Management Controller registers.
- Address lines A0, A2–A11, A13–A14, BA0, BA1, SDA10, SDCS_NCS1, SDWE, SDCKE, NBS1, RAS, CAS, and data lines D8–D15 are multiplexed with PIO lines and thus dedicated PIOs must be programmed in peripheral mode in the PIO controller.
- Assign the EBI CS1 to the SDRAM controller by setting the bit EBI_CS1A in the EBI Chip Select Assignment Register.
- Initialize the SDRAM Controller according to SDRAM device and system bus frequency.
- The Data Bus Width must be programmed to 16 bits.

The SDRAM initialization sequence is described in [Section 7.1 "Initialization Sequence"](#).

4.2 SDRAM 32-bit Connection

4.2.1 32-bit Hardware Configuration



4.2.2 Software Configuration

The following configuration must be respected:

- Setup Master clock and PLL clock through Power Management Controller registers.
- Address lines A0–A11, A13–A14, BA0, BA1, SDA10, SDCS_NCS1, SDWE, SDCKE, NBS1, RAS, CAS, and data lines D8–D15 are multiplexed with PIO lines and thus dedicated PIOs must be programmed in peripheral mode in the PIO controller.
- Assign the EBI_CS1 to the SDRAM controller by setting the bit EBI_CS1A in the EBI Chip Select Assignment Register.
- Initialize the SDRAM Controller according to SDRAM device and system bus frequency.
- The Data Bus Width is programmed to 32 bits.

The SDRAM initialization sequence is described in the [Section 7.1 "Initialization Sequence"](#).

5. SDRAM Signal Routing Considerations

The critical high-speed signal is associated with the SDRAM. The following are general guidelines for designing an SDRAM interface with AT91SAM7SE products with a targeted speed of 48 MHz on SDCK.

- Layout for the SDRAM should begin by placing the SDRAM devices as close as possible to the processor. A longer trace increases the rise and fall time of the signals.
- Keep the SDRAM clock (SDCK) and the SDRAM control lines as short as possible.
- Keep the address and data lines as short as possible.
- To support maximum speeds, reasonable SDRAM loading constraints must be followed. SDCK pin is not multiplexed with a PIO line in order to reach the maximum frequency of 48.2 MHz. The data bus can reach a maximum frequency of 25 MHz but this cannot be considered as speed limitation since the maximum data toggling rate is half the clock speed. For high-speed operation, the maximum load cannot exceed 40 pF on address and data buses and 30 pF on SDCK. The user must consider all the devices connected on the different buses to calculate the system load.
- Use sufficient decoupling scheme for memory devices. It is recommended to use low ESR 0.01 μ F and 0.1 μ F decoupling capacitors in parallel. An additional 0.001 μ F decoupling capacitor is recommended to minimize ground bounce and to filter high frequency noise.
- In the case of Mobile SDRAM supplied at 1.8V, VDDIO must be set to the correct voltage and the user must set SDCK to the correct frequency (refer to the Electrical Characteristics section of the [AT91SAM7SE Series](#) datasheet).

6. SDRAM Access Definition

6.1 SDRAM Controller Write Cycle

The SDRAM Controller allows single location burst access. The SDRAM controller keeps track of the active row in each bank, thus maximizing performance. To initiate an access, the SDRAM Controller uses the transfer type signal provided by the master requesting the access. If the next access is a sequential write access, writing to the SDRAM device is carried out. If the next access is a sequential write access, but the current access is to a boundary page, or if the next access is in another row, then the SDRAM Controller generates a precharge command, activates the new row and initiates a write command. To comply with SDRAM timing parameters, additional clock cycles are inserted between precharge/active (tRP) commands and active/write (tRCD) commands.

6.2 SDRAM Controller Read Cycle

The SDRAM Controller allows single location burst access. The SDRAM Controller keeps track of the active row in each bank, thus maximizing performance. If row and bank addresses do not match the previous row/bank address, then the SDRAM controller automatically generates a precharge command, activates the new row and starts the read command. To comply with SDRAM timing parameters, additional clock cycles on SDCK are inserted between precharge and active commands (tRP) and between active and read commands (tRCD). These two parameters are set in the configuration register of the SDRAM Controller. After a read command, additional wait states are generated to comply with the CAS latency (2 clock delays specified in the configuration register).

6.3 Border Management

When the memory row boundary has been reached, an automatic page break is inserted. In this case, the SDRAM controller generates a precharge command, activates the new row and initiates a read or write command. To comply with SDRAM timing parameters, an additional clock cycle is inserted between the precharge/active (tRP) command and the active/read (tRCD) command.

Figure 6-1. Read/Write General Access

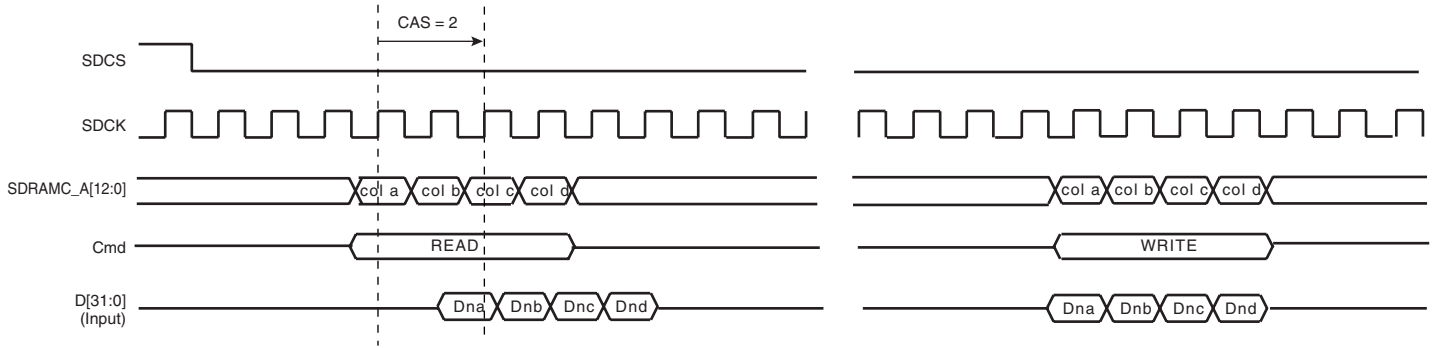


Figure 6-2. Read/Write Access After a Refresh

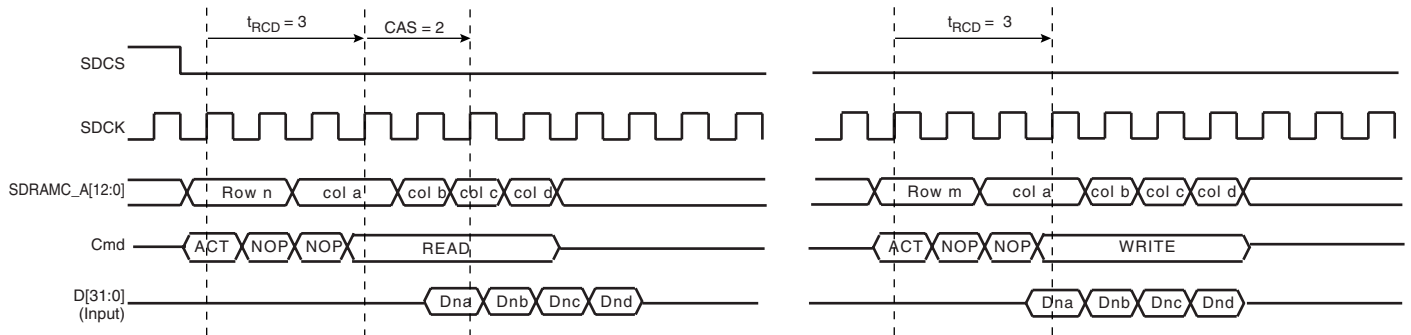
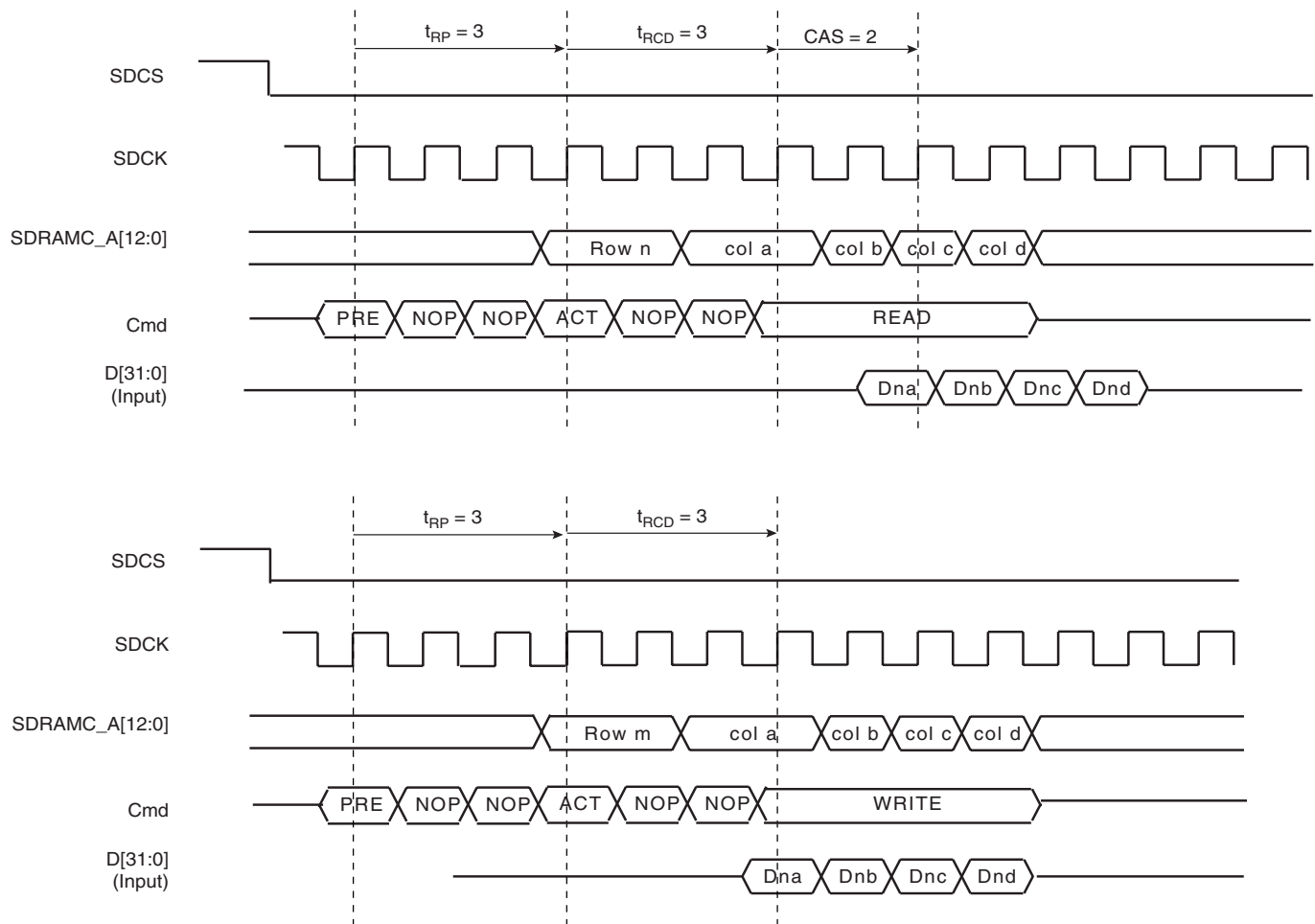


Figure 6-3. Read/Write Access After a Bank Opening



7. AT91SAM7SE Microcontroller SDRAM Controller Configuration

7.1 Initialization Sequence

The initialization sequence is generated by software. The SDRAM device is initialized by the following sequence:

1. SDRAM Characteristics must be set in the Configuration Register: asynchronous timings (TRC, TRAS, etc.), number of columns, rows, and CAS latency. The data bus width must be set in the Mode Register depending on the hardware configuration. Refer to the manufacturer's datasheet for SDRAM characteristics.
2. A minimum pause of 200 μ s is executed to precede any signal toggle.
3. A NOP command is issued to the SDRAM device. The application must set Mode to 1 in the Mode Register and perform a write access to any SDRAM address.
4. An All Banks Precharge command is issued to the SDRAM device. The application must set Mode to 2 in the Mode Register and perform a write access to any SDRAM address.
5. Eight auto-refresh (CBR) cycles are provided. The application must set the Mode to 4 in the Mode Register and perform a write access to any SDRAM location eight times.
6. A Mode Register set (MRS) cycle is issued to program the parameters of the SDRAM device, in particular CAS latency and burst length. The application must set Mode to 3 in the Mode Register and perform a write access to the SDRAM.
7. The application must go into Normal Mode, setting Mode to 0 in the Mode Register and performing a write access at any location in the SDRAM.
8. Write the refresh rate into the count field in the SDRAM Refresh Timer Register. (Refresh rate = delay between refresh cycles).

After initialization, the SDRAM device is fully functional. The initialization sequence can only be carried out once.

All memory accesses to the external SDRAM are handled automatically by the SDRAM controller. The maximum external SDRAM allocated memory space is 256 Mbytes, thus all accesses are done between 0x20000000 and 0x2FFFFFFF.

7.2 Micron® 48LC16M16A2-75 Characteristics

The Micron 48LC16M16A2-75 is a 256-Mbit device arranged as 4 Mbits x 16 x 4 banks with a CAS latency of 2 at 100 MHz. This device is mounted on the AT91SAM7SE-EK evaluation kits.

Table 7-1 summarizes Micron 48LC16M16A2-75 useful parameters for SDRAM Controller software settings.

Table 7-1. Micron 48LC16M16A2-75 Parameters

Parameter	Symbol	Value
Number of Columns	NC	9
Number of Rows	NR	13
Number of Banks	NB	4
CAS Latency	CAS	2 cycles
Write recovery time	TWR	15 ns
ACTIVE-to-ACTIVE command period	TRC	66 ns
PRECHARGE command period	TRP	20 ns

Table 7-1. Micron 48LC16M16A2-75 Parameters (Continued)

Parameter	Symbol	Value
ACTIVE-to-READ or WRITE delay	TRCD	20 ns
ACTIVE-to-PRECHARGE command	TRRS	44 ns
Exit SELF REFRESH to ACTIVE command	TXSR	75 ns
Refresh period (8,192 rows)	TR	64 ms

For further parameter checking, refer to the Micron 48LC16M16A2-75 product datasheet.

7.3 Software Initialization Parameters

The following table gives the software initialization parameters for running the program example on the AT91SAM7SE-EK evaluation kit at 48 MHz frequency.

Table 7-2. Software Initialization Parameters on AT91SAM7SE-EK Evaluation Kit

Description		Register/Field	Settings	Value
Board Oscillator			18.432 MHz	
PLL Output Frequency		CKGR_PLLR	96 MHz	0x1048100E
Processor/Master Clock		PMC_MCKR	48 MHz	0x00000007
EBI Chip Select Assignment		EBI_CSA	SDRAM	0x00000002
SDRAM Device	48LC16M16A2-75			
		SDRAMC_CR		0x21912159
Databus Width	16 bits	DBW	16 bits	b1
Number of Column	9	NC	9	b01
Number of Rows	13	NR	13	b10
Number of Banks	4	NB	4	b1
CAS Latency	2 cycles	CAS	2 cycles	b10
Write Recovery Delay	15 ns	TWR	2 cycles	2
Row Cycle Delay	66 ns	TRC	4 cycles	4
Row Precharge Delay	20 ns	TRP	2 cycles	2
Row to Column Delay	20 ns	TRCD	2 cycles	2
Active to Precharge Delay	44 ns	TRAS	3 cycles	3
Exit Self Refresh to Active Delay	75 ns	TXSR	4 cycles	4
SDRAMC Refresh Timer Register	7.8 μs (64/8192)	SDRAMC_TR	7.8 μs	0x180

It is highly recommended to check electrical and timing parameter compatibility between the SDRAM device and AT91SAM7SE SDRAM Controller. Refer to SDRAM product manufacturer's datasheet and to the chapter: "Electrical Characteristics" in the [AT91SAM7SE Series](#) product datasheet.

7.4 Software Initialization Example

```

/*-----
/* \fn      AT91F_InitSdram
/* \brief Init EBI and SDRAM controller for MT48LC16M16A2
/*-----
void AT91F_InitSdram (void)
{
    volatile unsigned int i;
    AT91PS_SDRDRC psdrc = AT91C_BASE_SDRDRC;

    // Init the EBI for SDRAM
    AT91C_BASE_EBI -> EBI_CSA = AT91C_EBI_CS1A_SDRAMC; // Chip Select is assigned to SDRAM
                                                         // controller

    //Configure PIO for EBI CS1
    AT91F_EBI_SDRAM_CfgPIO();

    /*** Step 1 ***/
    // Set Configuration Register
    psdrc->SDRDRC_CR = AT91C_SDRDRC_NC_9           | // 9 bits Column Addressing: 512 (A0-A8)
                                                             // AT91C_SDRDRC_NC_9
                    AT91C_SDRDRC_NR_13           | // 13 bits Row Addressing      8K (A0-12)
                                                             // AT91C_SDRDRC_NR_13
                    AT91C_SDRDRC_CAS_2           | // Micron MT48LC16M16A2-75(100MHz) needs CAS 2
                    AT91C_SDRDRC_NB_4_BANKS     | // 4 banks
                    AT91C_SDRDRC_TWR_2          |
                    AT91C_SDRDRC_TRC_4           |
                    AT91C_SDRDRC_TRP_2           |
                    AT91C_SDRDRC_TRCD_2          |
                    AT91C_SDRDRC_TRAS_3          |
                    AT91C_SDRDRC_TXSR_4          ;

    /*** Step 2 ***/
    // Wait 200us (not needed since the system starts on slow clock)

    /*** Step 3 ***/
    // NOP Command
    psdrc->SDRDRC_MR = AT91C_SDRDRC_DBW_16_BITS | AT91C_SDRDRC_MODE_NOP_CMD; // Set NOP
    *AT91C_SDRAM_BASE = 0x00000000; // Perform NOP

    /*** Step 4 ***/
    //All Banks Precharge Command
    psdrc->SDRDRC_MR = AT91C_SDRDRC_DBW_16_BITS | 0x00000002; // Set PRCHG AL
    *AT91C_SDRAM_BASE = 0x00000000; // Perform PRCHG

```

```
//*** Step 5 ***
//8 Refresh Command
psdrc->SDRC_MR = AT91C_SDRD_DBW_16_BITS | AT91C_SDRD_MODE_RFSH_CMD; // Set 1st CBR
*AT91C_SDRAM_BASE = 0x00000000; // Perform CBR

psdrc->SDRC_MR = AT91C_SDRD_DBW_16_BITS | AT91C_SDRD_MODE_RFSH_CMD; // Set 2nd CBR
*AT91C_SDRAM_BASE = 0x00000000; // Perform CBR

psdrc->SDRC_MR= AT91C_SDRD_DBW_16_BITS | AT91C_SDRD_MODE_RFSH_CMD; // Set 3rd CBR
*AT91C_SDRAM_BASE = 0x00000000; // Perform CBR

psdrc->SDRC_MR= AT91C_SDRD_DBW_16_BITS | AT91C_SDRD_MODE_RFSH_CMD; // Set 4th CBR
*AT91C_SDRAM_BASE = 0x00000000; // Perform CBR

psdrc->SDRC_MR= AT91C_SDRD_DBW_16_BITS | AT91C_SDRD_MODE_RFSH_CMD; // Set 5th CBR
*AT91C_SDRAM_BASE = 0x00000000; // Perform CBR

psdrc->SDRC_MR= AT91C_SDRD_DBW_16_BITS | AT91C_SDRD_MODE_RFSH_CMD; // Set 6th CBR
*AT91C_SDRAM_BASE = 0x00000000; // Perform CBR

psdrc->SDRC_MR= AT91C_SDRD_DBW_16_BITS | AT91C_SDRD_MODE_RFSH_CMD; // Set 7th CBR
*AT91C_SDRAM_BASE = 0x00000000; // Perform CBR

psdrc->SDRC_MR= AT91C_SDRD_DBW_16_BITS | AT91C_SDRD_MODE_RFSH_CMD; // Set 8th CBR
*AT91C_SDRAM_BASE = 0x00000000; // Perform CBR

//*** Step 6 ***
//Mode Register Command
psdrc->SDRC_MR= AT91C_SDRD_DBW_16_BITS | AT91C_SDRD_MODE_LMR_CMD; // Set LMR operation
*AT91C_SDRAM_BASE = 0x00000000; // Perform LMR burst=1,
// lat=2

//*** Step 7 ***
//Normal Mode Command
psdrc->SDRC_MR= AT91C_SDRD_DBW_16_BITS | AT91C_SDRD_MODE_NORMAL_CMD; // Set Normal mode
// 16 bits
*AT91C_SDRAM_BASE= 0x00000000; // Perform Normal mode

//*** Step 8 ***
// Set Refresh Timer
psdrc->SDRC_TR= AT91C_SDRD_TR_TIME;

}
```

8. Software Access Optimization

8.1 Software General Description

The whole SDRAM memory space is initialized, then the code reads each address memory location in the first half space and writes it to an address memory location in the second half space. LED1 is turned on during the entire copying process. Once finished, the software compares the values between every first half and second half memory space location. If this operation is successful, LED2 is turned on, otherwise it remains off.

8.2 Data Transfer Methods

8.2.1 Single Location

The following code allows single-location data transfer:

```
for(i = 0; i < AT91C_SDRAM_SIZE/2; i++)
{
    *(AT91C_SDRAM_BASE + (0x1000000/4) + i) = *(AT91C_SDRAM_BASE + i);
}
```

The time to copy the data from the first half memory space to the second half is measured by probing the signal driving LED1 with an oscilloscope.

The measurement gives: 1.432s.

8.2.2 Multi Location

The following code allows four-location data transfer:

Note: Since the multi-transfer instructions are not available in C-language, the code in this instance is written in Assembly.

```
stmfd    sp!, {r4-r7} ; Save R4, R5, R6 and R7 in User Stack
loop
ldmia    r1!, {r4-r7} ; R4=*R1, R5=*(R1+4), R6=*(R1+8), R7=*(R1+12)
stmia    r2!, {r4-r7} ; R2=R4, *(R2+4)=R5, *(R2+8)=R6, *(R2+12)=R7

subs     r0, r0, #4 ; R0=R0-4 (4 address locations transfered at once)

bne      loop ; If R0 != #0 goto loop

ldmia    sp!, {r4-r7} ; Restore R4, R5, R6 and R7 registers from User Stack
bx       r14 ; If R0 == #0 return
```

The time to copy the data from the first half memory space to the second half is measured by probing the signal driving LED1 with an oscilloscope.

The measurement gives: 1.1280s.

8.3 Conclusion

Significant data transfer optimization can be done by using load and store multiple instructions. The results obtained in the [“Data Transfer Methods”](#) section above, give a time reduction of almost 22% for read/write access over the half memory space. External SDRAM access software optimization should be taken into account in applications where access time is critical.

9. SDRAM Controller Power Consumption

9.1 VDDIO Power Consumption

AT91SAM7SE device SDRAM controller power consumption on VDDIO depends on clock frequency, percentage of read/write accesses, number of accesses per second and data line transitions.

Table 9-1 gives AT91SAM7SE device SDRAM controller typical power consumption on VDDIO (measurements made in full time access at 48 MHz on the AT91SAM7SE-EK kit).

Table 9-1. VDDIO Power Consumption

Data value	0x00000000	0xAAAAAAAA	0xFFFFFFFF
100% read	7.2 mA	7.2 mA	7.2 mA
100% write	8 mA	22.8 mA	33.4 mA
50% Write/50% read	10.7 mA	19.4 mA	36 mA

Since power consumption depends on data lines transitions, measurements have been made with significant write and read data different values.

9.2 VDDCORE Power Consumption

AT91SAM7SE device SDRAM controller power consumption on VDDCORE is not significantly affected by the percentage of read/write accesses and data line transitions.

Table 9-2 gives AT91SAM7SE device SDRAM controller typical power consumption on VDDCORE (measurements made in full time access at 48 MHz on the AT91SAM7SE-EK kit)

Table 9-2. VDDCORE Power Consumption

Data value	0x00000000	0xAAAAAAAA	0xFFFFFFFF
100% read	24.7 mA	24.7 mA	24.7 mA
100% write	25.6 mA	26.2 mA	26.8 mA
50% Write/50% read	24.5 mA	25.1 mA	25.7mA

10. Conclusion

- As the SDRAM clock influence is essential, it must be set appropriately.
- SDRAM CAS latency impacts the throughput. The CAS latency must be set to a value matching the SDRAM frequency.
- SDRAM refresh register is to be set with an optimal value. A refresh delay shorter than necessary only penalizes the throughput without any positive influence.
- Software should take advantage of the SDRAM open-bank policy by locating code, data, etc. on separate SDRAM bank and row boundaries.
- Software optimization should be taken into account for best performance.
- Power consumption on VDDIO can be optimized by minimizing the number of accesses.



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