VSC8558/VSC8658/VSC8664
Application Note
Dual SerDes Advantages

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Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.01

Revision 1.01 was released in January 2008. Updated document to add VSC8658 and VSC8664.

1.2 Revision 1.00

Revision 1.00 was the first release of this document. It was published in December 2005.

2 Introduction

This application is intended to outline the advantages of using the VSC8558/VSC8658/VSC8664's Dual SerDes architecture for SGMII-to-Fiber applications.

2.1 Audience

The target audiences for this document are hardware and system engineers evaluating an Octal/Quad Gigabit PHY for fiber applications.

2.2 References

2.2.1 Vitesse Documents

- VSC8558 Product Datasheet
- VSC8658 Product Datasheet
- VSC8664 Product Datasheet

2.2.2 External Documents

- Cisco Serial-GMII Specification v1.7
- IEEE 802.3z (1000Base-X) Clause 36, 37

3 Overview

The increase in the use of SGMII MAC interfaces within Switches and MAC devices has created many challenges to Gigabit PHY ASIC Design. One specific issue is the support for the PHY operating mode: SGMII-to-1000BASE-X Fiber. This document describes the advantages for using two SerDes blocks to minimize issues such as jitter transfer.

3.1 The Need for SerDes Blocks in Gigabit Ethernet

The majority of Gigabit Ethernet PHYs have Copper Front End interfaces to connect to Category 5e cabling. Many Gigabit Ethernet PHYs also have 1000BASE-X fiber frontend interfaces for long-haul transmission over fiber-optic cabling. The PHYs that support 1000BASE-X fiber contain a SerDes to serialize/deserialize the data across the fiber cable. Also note that many PHYs such as the VSC8211, VSC8224, VSC8558, VSC8658, and VSC8665 also support Auto-Media-Sense, which allows a given PHY to actively change between copper and fiber links based on link-up/down events and media priority.

A traditional Gigabit Ethernet PHY also has a MAC Interface that is either GMII or RGMII. The demand for more ports within a board design has created the need to lower pin-count easing PCB routability and alleviating cross-talk issues associated with densely packed traces within a confined area. SGMII was conceived to help reduce the pin-count from 12 pins per port with RGMII, down to 8 pins per port with SGMII. Most PHYs also support a 4-pin version of SGMII that removed the requirement for separate transmit and receive differential clock pins. SGMII also requires a SerDes to serialize/deserialize the GMII data stream into two differential pairs that can interface with a MAC.

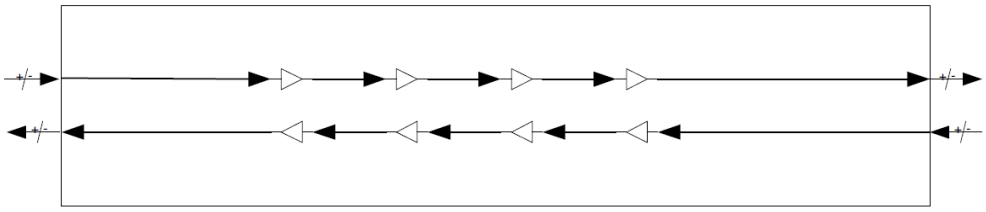
3.2 Supporting 1000BASE-X with SGMII-Based PHYs

The combination of SGMII and Fiber applications within a PHY operating at the same time has created design tradeoffs.

3.2.1 Pass-Through Mode with no SerDes

One method for supporting 1000BASE-X within a PHY is if the MAC can support both SGMII and 1000BASE-X, to have the MAC set to 1000BASE-X and the PHY set to a mode in which there is a direct pathway to the PHY's 1000BASE-X front end. This mode is generically referred to as "pass-through" mode where the MAC's I/O is directly connected to the 1000BASE-X module through very little logic inside of the PHY. See the following figure.

Figure 1 • Pass-Through Mode with no SerDes



The advantages to this method are simpler ASIC design and savings in valuable die area. In this manner, no SerDes is required as the data is passed through without any conversion. The disadvantages are any timing jitter brought in from the MAC side is transmitted out on the fiber-end and vice versa. Also, the cascading buffer design with pass-through mode could accumulate additional jitter and further push timing to potentially outside the jitter specifications for fiber modes. This can lead to potentially failing interoperability issues. Another disadvantage is link/activity indication via register settings and/or LEDs may not be possible as additional logic such as energy and packet activity detectors are required. Finally, the MAC must support and change between SGMII and 1000BASE-X modes.

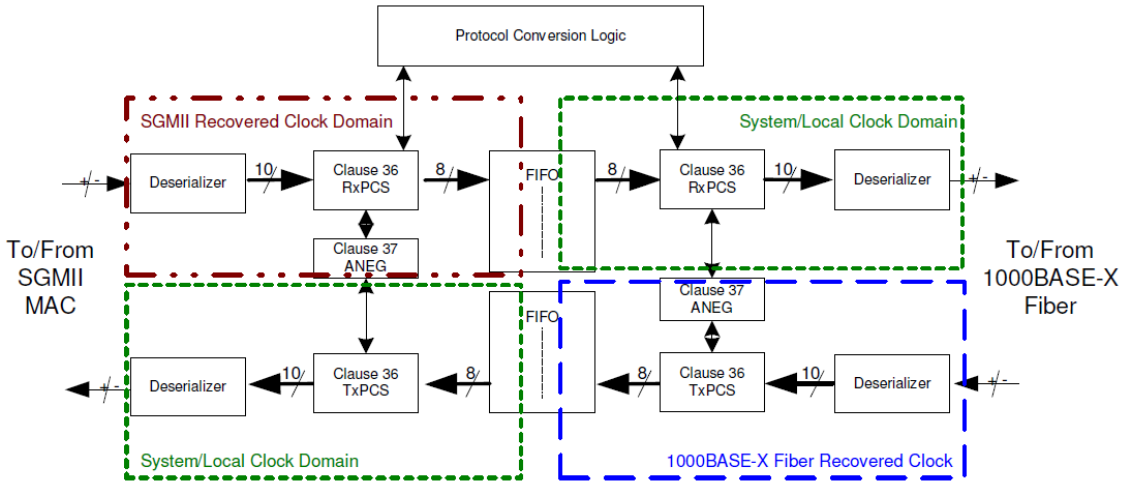
3.2.2 SGMII-to-1000BASE-X Using One SerDes

There are various methods for using one SerDes block to perform SGMII-to-1000BASE-X fiber conversion, but all methods require having to utilize at least one recovered clock as a transmitter. With only one CDR (Clock Data Recovery) unit, either the transmit data to the remote PHY or the receive data from the remote PHY to the MAC can be retimed. The disadvantage in this situation is the same as the pass-through mode in the previous section where accumulated jitter on this clock can cause an interoperability issue.

3.2.3 SGMII-to-1000BASE-X Using Two SerDes

Another method is to integrate two SerDes blocks within a Gigabit Ethernet PHY. The MAC SerDes can perform conversion between SGMII to an 802.3 standard, GMII format. The Fiber MDI SerDes can then perform conversion to 1000BASE-X fiber. See the following figure.

Figure 2 • Dual SerDes Architecture



With the addition of an asynchronous FIFO, this method has the advantage that each SerDes block has unique transmitter and receiver clocks. The transmitter clocks in both directions are derived from the local system clock as opposed to retransmitting data on a remote system clock which will suffer from accumulated jitter as it passes through the local PHY. The disadvantages are a more complex PHY design with additional die area dedicated to the additional SerDes, PCS, and FIFO blocks and slightly increased system latency. But given the 1000BASE-X jitter transmit and receive specifications can be difficult to meet in many applications, using a dual SerDes architecture to properly decouple timing is a sensible advantage to ensure meeting the IEEE specification for jitter across fiber networks.

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