

LAN9xxx Series Migration

INTRODUCTION

This application note details the differences one should be aware of when migrating from older to newer generation Microchip Ethernet Controllers. The discussion is broken down into factors concerning hardware, software and, when required, system level considerations. Information provided herein should facilitate migration from, for example, LAN9118 to LAN9221 in a manner devoid of complications or confusion.

Microchip's LANCheck design support service is available for validation of schematics and layout. This service may be accessed via your local Microchip contact or the Microchip web site.

The following is a list of SRAM style host bus Ethernet controllers in chronological order:

- LAN9118, LAN9117, LAN9116, LAN9115
- LAN9218, LAN9217, LAN9215
- LAN9210, LAN9211
- LAN9220, LAN9221

FIGURE 1: DEVICE PROGRESSION

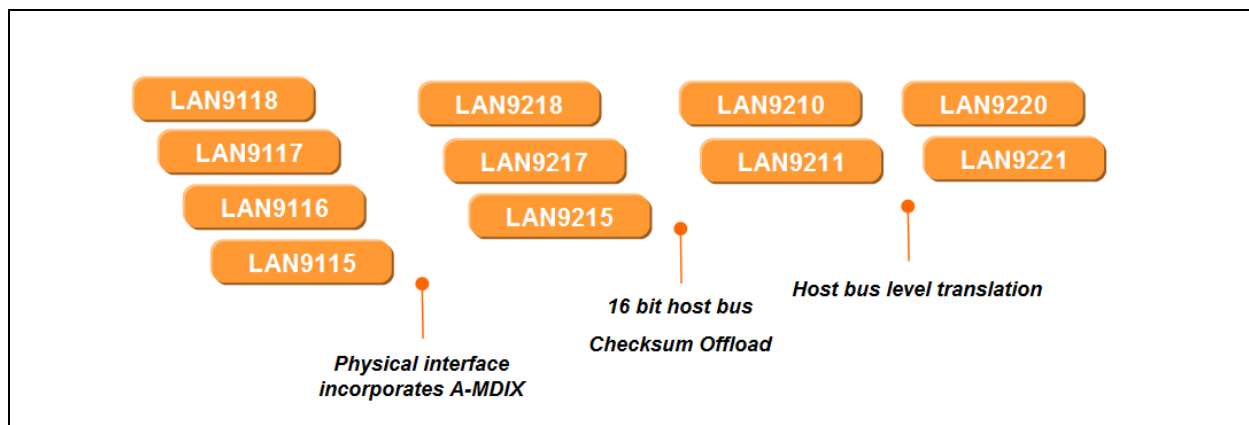


Table 1 provides a summary of the feature differences between devices. A high level overview of each device family is provided in the following sections.

TABLE 1: DEVICE DIFFERENCES SUMMARY

Part Number	ID_REV Bits 31:16	Cycle Time (ns)	Bus Width	Package	External MII	Auto-MDIX	CRC Checksum offload	Variable Voltage I/O
LAN9115	0x0115	165	16	100-TQFP	X			
LAN9116	0x0116	165	16	100-TQFP	X			
LAN9117	0x0117	45	32	100-TQFP				
LAN9118	0x0118	45	32	100-TQFP				
LAN9215	0x115A	165	16	100-TQFP	X	X		
LAN9216	0x116A	165	16	100-TQFP	X	X		
LAN9217	0x117A	45	32	100-TQFP		X		
LAN9218	0x118A	45	32	100-TQFP		X		

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TABLE 1: DEVICE DIFFERENCES SUMMARY (CONTINUED)

Part Number	ID_REV Bits 31:16	Cycle Time (ns)	Bus Width	Package	External MII	Auto-MDIX	CRC Checksum offload	Variable Voltage I/O
LAN9210	0x9210	165	16	56-QFN		X	X	
LAN9211	0x9211	45	16	56-QFN		X	X	
LAN9220	0x9220	165	16	56-QFN		X	X	X
LAN9221	0x9221	45	16	56-QFN		X	X	X

LAN9118, LAN9117, LAN9116, LAN9115

The devices discussed within the scope of this document form a progression which started in 2004 with LAN9118. This device offers a 32-bit wide SRAM style interface with a combined MAC and PHY for 10/100 Ethernet. The market soon demanded variants of this device for different applications. LAN9117 followed with a 16-bit wide host bus interface and an MII port, on what would in the case of LAN9118, have been the pinning for the upper 16 data lines. The packaging remained common, utilizing a 100-TQFP. LAN9116 followed, offering a 32-bit host bus interface with slightly relaxed timing for less intensive applications. LAN9115 was the final family element, with relaxed bus timing and a 16-bit wide interface. This family of devices has a common software abstraction, FIFO mechanism and Ethernet physical interface.

LAN9218, LAN9217, LAN9215

Following a market requirement for automatic cable crossover (HP Auto-MDIX), the device portfolio was upgraded with this change. By default, cable crossover is enabled. This does require consideration within the analog nets – as symmetry must exist between the transmit and receive pairs. All other aspects remain common to the preceding family of parts. For example – LAN9218 offers identical functionality to LAN9118, despite the fact that it contains an enhanced physical interface. At the time these parts were introduced, some other PHY related changes were made that resulted in enhanced line reach (150 meters) and lower emissions.

LAN9210, LAN9211

A market demand for smaller packaging and faster host bus cycle timing was answered with the next device progression. LAN9210 was released in a 56-QFN package and utilizes a 16-bit host bus interface. The cycle time was reduced to arrive at real world throughput near identical to the previous 32-bit implementation. Additional features such as CRC Checksum offload were also integrated. This feature is disabled by default to maintain compatibility with previous generation devices. The physical interface is largely common between the LAN9218 series and LAN9210 series, although the LAN9210 series does offer an enhancement in line reach toward 170 meters.

LAN9220, LAN9221

The most recent additions to the Microchip Ethernet controller family address the need for host bus voltage levels other than 3.3V. Utilizing what was previously a test pin on the LAN9210 and LAN9211, these devices permit setting I/O levels between 1.6 and 3.6V.

HARDWARE CONSIDERATIONS

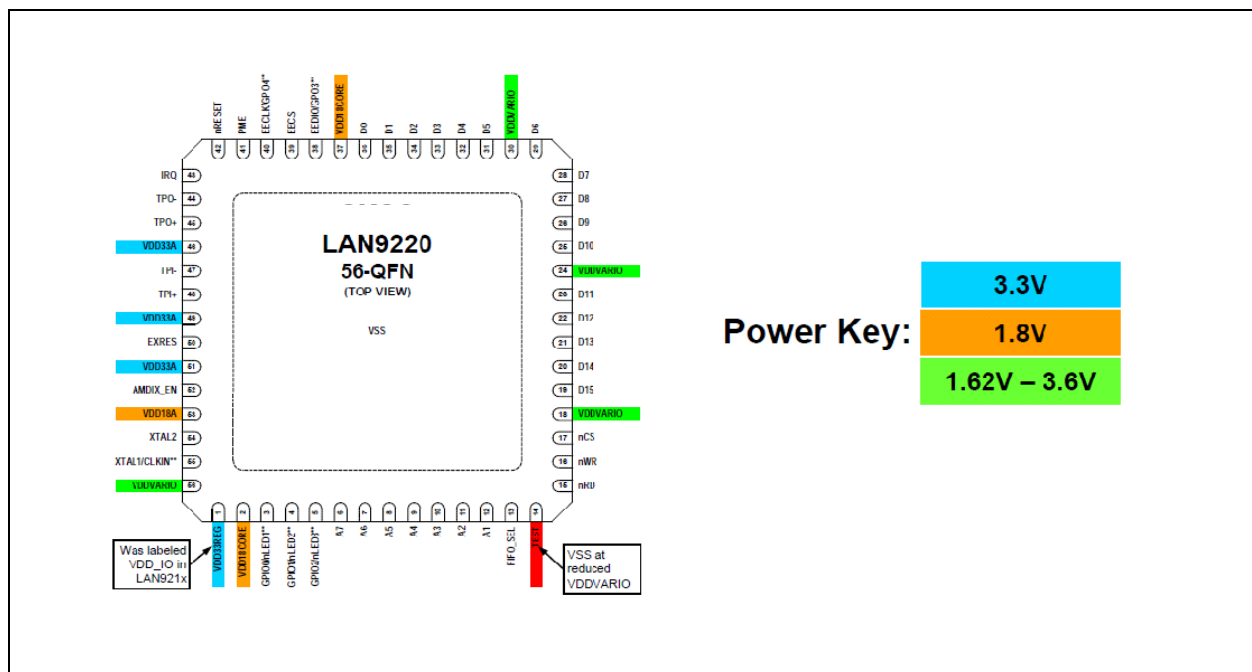
In this application note, it is assumed that the targeted device for migration is LAN9221 and the starting point is any part preceding it in the roadmap. Each of the following sections are discussed in greater detail in the device data sheet, which should be used as the authoritative reference source. The most applicable aspects are summarized and supported with a basic requirements outline.

Host Bus Voltage Level

LAN9220/LAN9221 offers an integrated level translator such that direct connection can be made to busses operating at levels other than 3.3 volts. The level is set via a dedicated pin. The value can be in the range of 1.62 to 3.6 volts. The reader is invited to become familiar with this feature by consulting the LAN9220/LAN9221 schematic checklist and Data Sheet.

Note: With a reduced IO voltage, the bus will become more sensitive towards load capacitance.

FIGURE 2: VARIABLE VDDIO



Internal Pull-up / Pull-down

Internal resistors may not allow sufficient current for the host bus voltage intended for operation. If operating at 1.8V, consider placing a 4.7k resistor externally, in lieu of relying on the pin drivers internal PU/PD.

EEPROM

The EEPROM circuit operates at VDDIO. Therefore, if utilizing 1.8V, consider that the EEPROM must also be compatible with this voltage.

Host Bus Width

If moving from any of the devices using a 32-bit interface, consider the target is 16-bits wide. This has more implications for software than hardware and they are discussed in the software section of this document. Any host bus straps used to indicate the peripheral bus width should be set accordingly, and be little endian.

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Clock Circuit

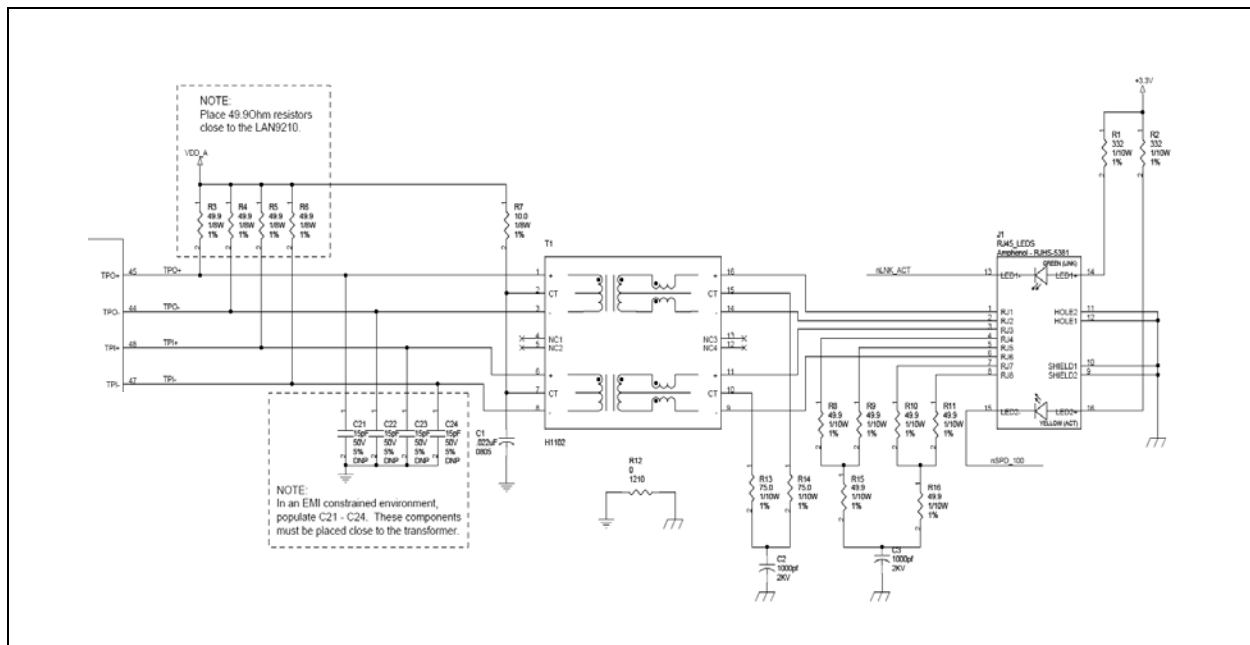
Ensure that a 25 MHz crystal is used. The crystal should exhibit 50 PPM accuracy and have no less than 300 uW drive capability. The maximum drive level is related to the physical size of the crystal. Particular attention should be paid to very small SMT devices which may be hard pressed to reach this figure.

Physical Interface - Analog Nets

The target device offers Auto-MDIX automatic cable crossover. This feature enables negotiation between link partners to enable use of either line pair for TX or RX. The analog nets supporting these signals must therefore be symmetrical. If migrating from a device that did not offer this feature, attention should be paid to this fact. Refer to [Figure 3](#) for an example of a typical physical interface.

Note: When migrating from a LAN911x device to a LAN92xx device, the same physical interface cannot be used. The physical interface components, including the magnetics, must be updated.

FIGURE 3: PHYSICAL INTERFACE ANALOG NETS



Impedance Controlled Traces

Only the differential PHY signals shall fall into this category. Both pairs should be routed with 100 Ohm differential impedance. Pairs should be length matches and not exceed 50 mils difference. High speed signals should be avoided within 300 mils of this routing. Vias should be avoided, although if present, they should be balanced so the symmetry is maintained between signals.

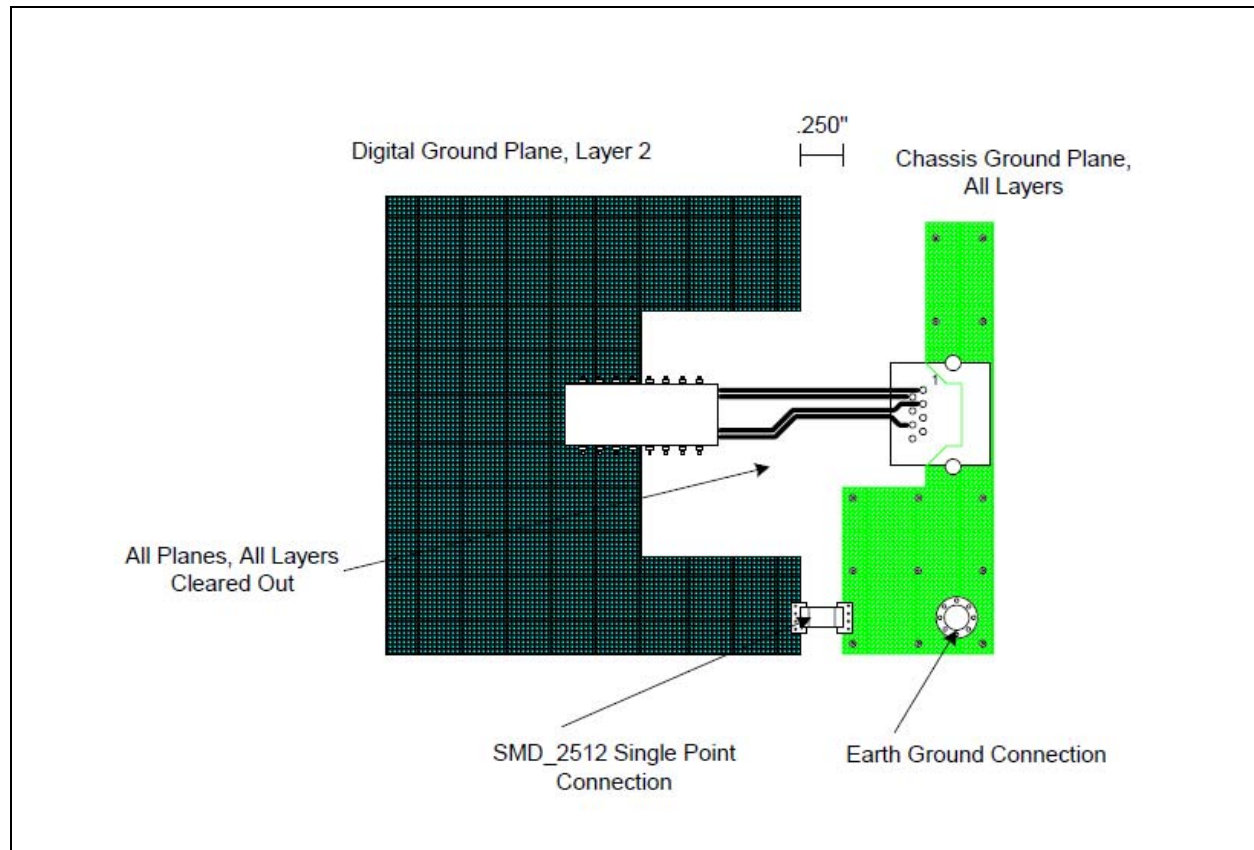
EMC - DNP Additions for Testing

It's often useful to make provisions for populating components that may assist during EMC testing. 0402 footprints from each of the analog differential signals to analog VSS are recommended for this purpose. These should be placed near to the line magnetic. Absolute values for population shall depend upon layout, although typically no more than 22pF should be added to avoid infringing on the 802.3 pulse mask.

EMC - Layout Considerations

Maintain two separate grounds for the line buildout. These should be joined together at one point only, using a single high voltage capacitor. A 2512 footprint is recommended. The chassis ground pour should extend from this termination point to the RJ45 connector. Using the 2512 capacitor, a 25mil minimum keepout can be maintained between the analog return and chassis ground up to the line transformer. The transformer, being the point of separation, should be 50% filled with the respective analog VSS.

FIGURE 4: ESD GROUND CONSIDERATIONS



Analog Reference

Ensure the external biasing resistor is 12.4k, 1%. This is used within the device to set all analog references. Placement close to LAN9221 is desirable, as any induced noise shall propagate the internal analog nets.

SOFTWARE CONSIDERATIONS

Host Bus Width

The LAN9221 has a 16-bit host bus. Users transitioning from a 32-bit bus LAN9118 should ensure that the device is always accessed in pairs of 16-bit operations. These must be done consecutively and must not be interrupted until the pair has completed.

Some host bus interfaces are capable of handling this automatically, so software can just perform a 32-bit read operation. The bus interface will ensure the two reads happen consecutively and are not interrupted. This is the preferred configuration.

If the host bus does not perform this function and the driver initiates pairs of 16-bit reads/writes manually, it is very important to implement some form of locking to ensure the two 16-bit operations cannot be interrupted. Problems occur if the driver's Interrupt Service Routine (ISR) can run in the middle of a pair of 16-bit reads, as the ISR will likely then start a new pair of reads. Both the ISR and the interrupted code will read invalid register contents in this scenario.

There is no difference between this and the 16-bit interface on earlier products (such as LAN9115). However, it is a potential pitfall to be aware of when transitioning from a 32-bit interface to a 16-bit interface. Refer to [Table 1](#) for a list of host bus cycle times for each Microchip device.

Device ID and Revision Register

Microchip parts return different values in their ID_REV registers. Drivers use this field to identify the device, so the driver may have to be updated to accept the value present in LAN9221. Current versions of drivers provided by Microchip for all operating systems correctly support all ID_REV returned values. Refer to [Table 1](#) for a list of device IDs for each Microchip device.

HP Auto-MDIX PHY

All LAN92xx parts have an HP Auto-MDIX PHY. In most cases, no software configuration is required to support this feature. The default power-on configuration uses the AMDIX_EN strap to enable or disable Auto-MDIX. If required, it is possible to override the default via software and force the MDIX feature to either the crossed or non-crossed state by setting PHY register 27 (Special Control/Status Indications).

Checksum Offload

LAN9210, LAN9211, LAN9220 & LAN9221 all have a checksum offload feature for both TX and RX. Drivers can use this to offload TCP segment checksum processing.

By default, both TX and RX checksum engines are disabled, so the transmit and receive interfaces are compatible with existing LAN9118 drivers. If a driver wants to use the checksum offload engines, it needs to explicitly enable them.

APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level and Date	Section/Figure/Entry	Correction
DS00003004A (03-19-19)	Replaces previous SMSC version Rev. 1.0 (11-19-12).	
Rev. 1.0 (11-19-12)	Document co-branded: Microchip logo added; modification to legal disclaimer.	
Rev. 1.0 (06-28-11)	All	Initial release

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ISBN: 9781522442929

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