

## Introduction [\(Ask a Question\)](#)

This document describes the Microchip JESD204B stand-alone interface design and how to run the demo on a PolarFire Evaluation kit.

The main components of the demo design are as follows:

- CoreJESD204BTX and CoreJESD204BRX IP cores implement the transmitter and receiver interfaces of the JESD204B standard. These IP cores are easy to integrate with the JESD204B- based data converters to develop high-bandwidth applications such as wireless infrastructure transceivers, software-defined radios, medical imaging systems, and radar and secure communications. They support link widths from x1 to x8, and link rates from 250 Mbps to 12.5 Gbps per lane using subclass 0, 1, and 2.
- PolarFire transceiver interface can handle data rates ranging from 250 Mbps to 12.5 Gbps. It integrates several functional blocks to support multiple high-speed serial protocols within the FPGA.

The design operates in the loopback mode by sending the CoreJESD204BTX data to the CoreJESD204BRX IP core through one or more transceiver lanes, which are looped back on the board. A user-friendly GUI is provided for selecting the input data and error injection, and for monitoring the JESD204B link status.

For Evaluation kit, two designs are provided as follows:

- SMA-based loopback design that runs at 6.25 Gbps lane rate (with single XCVR lane for TX and RX).
- PCB-based loopback design that runs at 5 Gbps lane rate (with two XCVR lanes, where one lane is for TX and the other for RX).

For more information about the JESD204B interface design implementation, and all the necessary blocks and IP cores instantiated in Libero SoC, see [3. Demo Design](#).

The JESD204B design can be programmed using any of the following options:

- **Using the job file:** To program the device using the job file provided along with the design files, see [9. Appendix: Programming the Device Using FlashPro Express](#).
- **Using Libero SoC:** To program the device using Libero SoC, see [8. Running the Demo](#). Use this option when the demo design is modified.

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## 1. Design Requirements [\(Ask a Question\)](#)

The following table lists the resources required to run the demo:

**Table 1-1.** Design Requirements

Requirement	Version
Operating System	Windows 10 or 11
<b>Hardware</b>	
PolarFire Evaluation Kit (MPF300-EVAL-KIT)	Rev D or later
Two SMA-to-SMA cables (not provided with the kit) Optional: User can also test with on board loopback	Required for Evaluation kit.
<b>Software</b>	
FlashPro Express	<b>Note:</b> Refer to the readme.txt file provided in the design files for the software versions used with this reference design.
Libero SoC	

## 2. Prerequisites [\(Ask a Question\)](#)

Before you begin, perform the following steps:

- Download the design files from the following link: [www.microchip.com/en-us/application-notes/AN5341](http://www.microchip.com/en-us/application-notes/AN5341)
- Download and install the Libero® SoC Design Suite from [Libero SoC Software Downloads](#)



**Important:** A Libero Gold license is required to evaluate your designs on the MPF300 device.

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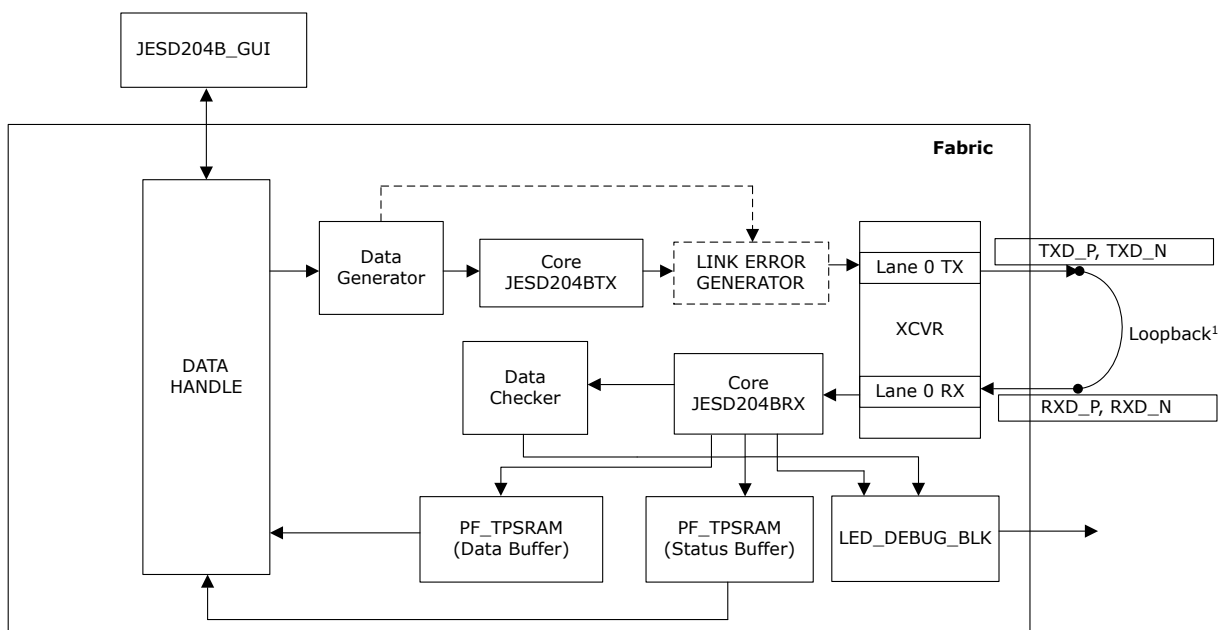
### 3. Demo Design (Ask a Question)

The PolarFire JESD204B demo design interfaces JESD204B compliant data converters with PolarFire devices. In this design:

1. The DATA\_HANDLE\_0 block interfaces with the GUI. The GUI enables the selection of PRBS or waveform input.
2. The DATA\_HANDLE\_0 block passes the input selection to the DATA\_GENERATOR\_0 block, which generates and sends the corresponding input data to the CoreJESD204BTX IP core.
3. The CoreJESD204BTX IP core performs the JESD204B transmitter functions based on the configuration, and sends the data to the PF\_XCVR (transceiver) IP core.
4. The encoded data is received by the CoreJESD204BRX IP core because the TX and RX lanes of the PF\_XCVR block are looped back. The CoreJESD204BRX IP core performs the JESD204B receiver functions based on the configuration, and sends the data to the GUI for viewing the selected input.
5. The JESD204B GUI displays data and status received from the JESD204BRX IP.

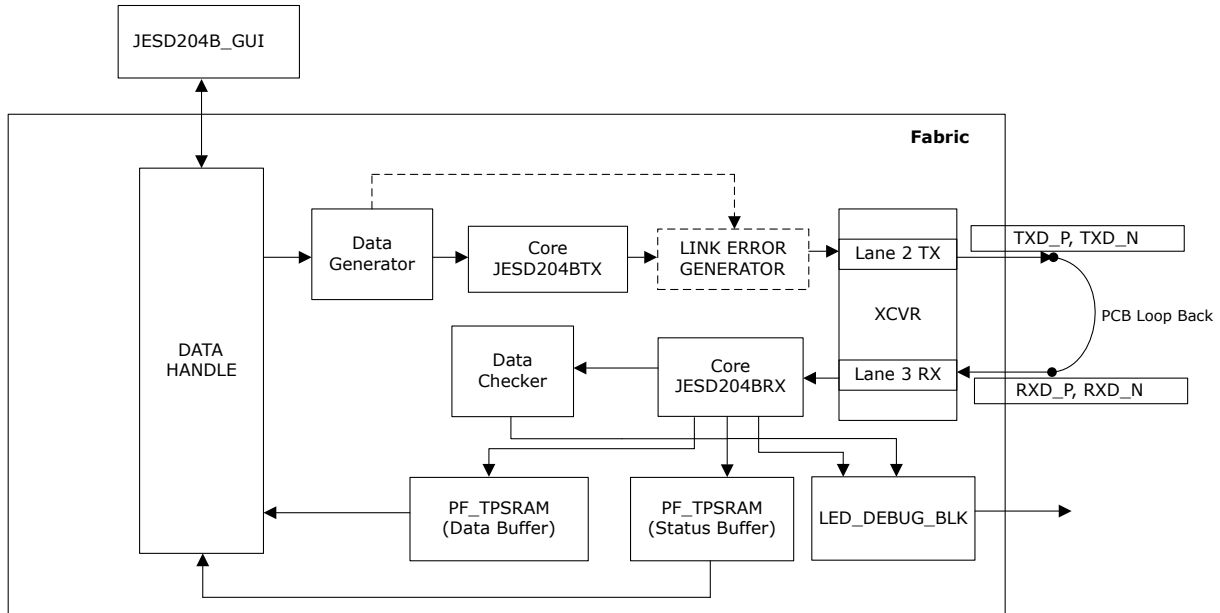
**➔ Important:** When a data error or link error is selected on the GUI, the error generator block generates that error and displays it on the GUI.

**Figure 3-1.** SMA Loop Back (Evaluation kit) Block Diagram



1. On Evaluation kit the loopback is SMA-based.

Figure 3-2. PCB Loop Back Block Diagram

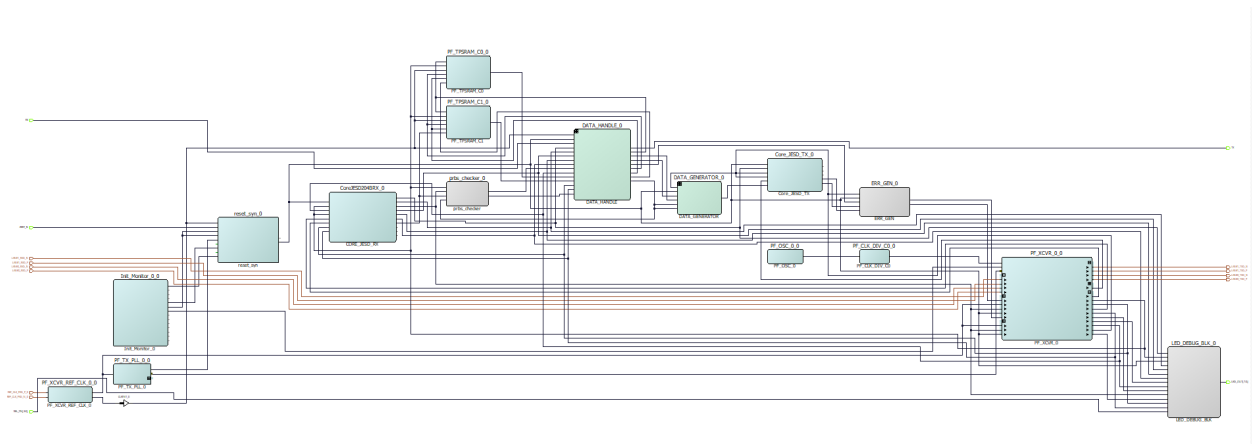


### 3.1 Design Implementation [\(Ask a Question\)](#)

This section shows the Libero design implementation, describes the IPs used and their configurations, and important input/output signals.

The following figure shows the design implementation of JESD204B interface in Libero:

Figure 3-3. JESD204B Interface Design



As shown in the figure, the design consists of the following parts:

- 3.1.1. Transmit
- 3.1.2. Receive

#### 3.1.1 Transmit [\(Ask a Question\)](#)

The following IPs form the transmit part of the design:

1. **DATA\_GENERATOR**— This block has a PRBS generator and a waveform generator. The PRBS generator generates PRBS7, PRBS15, PRBS23, and PRBS31 patterns. An error insertion mode implemented in the PRBS generator, inserts an error into the PRBS sequence. The waveform

generator generates sine, sawtooth, triangle, and square waveforms. The data generator feeds the 64-bit test pattern to the JESD204BTX core, which then transmits data to the transceiver.

2. **CoreJESD204BTX**— This IP is the transmitter interface of the JEDEC JESD204B standard. For the SMA-based loopback design, the Core Configuration of this IP core is as follows:
  - Encoder: Removed
  - Data Width: 32
  - Serdes Mode: 1
  - Scrambling: Disabled
  - Device Subclass version: Subclass0
  - JESD204 version: JESD204B
  - Number of Lanes:1
  - Number of octets per frame: 2
  - Number of frames for multi-frame: 9
  - Number of multi-frames in ILA sequence: 4The Link Configuration of CoreJESD204BTX is as follows:
  - Number of converters per device: 2
  - Converter resolution: 16
  - Total Number of bits per sample: 16
  - Number of samples per converter per frame cycle: 1

For more information about CoreJESD204BTX, see *CoreJESD204BTX Handbook* from Libero SoC catalog.

3. **ERR\_GEN\_0**— This block generates link errors by sending random data between CoreJESD204BTX and PF\_XCVR, when the link error generation is selected on the GUI.
4. **DATA\_HANDLE\_0**— This block receives the input data selection and link or data error generation information from the GUI. Also, the block sends the data output received from the CoreJESD204BRX core and the data or link status error to the GUI for viewing.
5. **PF\_XCVR\_ERM**— This is a hard IP block that supports high-speed data rates ranging from 250 Mbps to 12.5 Gbps. The following points summarize the configuration of the transceiver interface:
  - For the SMA loopback design, the transceiver block (PF\_XCVR) is configured in 8b10b mode with a CDR reference clock of 156.25 MHz and data-rate of 6.25 Gbps. XCVR configuration settings are as follows:
    - Number of Lanes: 1; Enhanced receiver management: Enabled; Receiver calibration: None (CDR)
    - Transceiver data-rate: 6.25 Gbps; TX clock division factor: 1; TX PPLL base data-rate: 6.25 Gbps; TX PLL bit lock frequency: 3.125 Gbps
    - CDR Lock Mode: Lock to data; CDR reference clock source: Dedicated; CDR reference clock frequency: 156.25 MHz
    - PCS-Fabric interface width: 32-bit; 8b/10b Encoding/Decoding: Enabled
    - FPGA interface frequency: 156.25 MHz
  - For PCB loopback demo, the transceiver block (PF\_XCVR) is configured for two lanes in 8b10b mode with a CDR reference clock of 125 MHz and data-rate of 5Gbps.
  - The PolarFire transmit PLL (PF\_TX\_PLL) send the reference clock feed to the transceiver. The dedicated reference clock (PF\_XCVR\_REF\_CLK) drives the PF\_TX\_PLL to generate the desired output bit clock for the 6.25 Gbps or 5 Gbps data-rate.

### 3.1.2 Receive [\(Ask a Question\)](#)

The following IPs form the receive part of the design:

1. **CoreJESD204BRX**—This is the receiver interface of the JEDEC JESD204B standard. For the SMA-based loopback design, the Core Configuration of this IP core is as follows:
  - Decoder: Removed
  - Data Width: 32
  - Serdes Mode: 1
  - Scrambling: Disabled
  - Device Subclass Version: Subclass 0
  - JESD204 version: JESD204B
  - No. of Lanes (L+1): 1
  - Checksum calculation type: Octet
  - Frame Alignment Correction: Enabled
  - Link Configuration Error: Enabled
  - RAM Implementation: In FPGA Fabric

The CoreJESD204BRX and CoreJESD204BTX IPs have the same Link configuration. For more information about CoreJESD204BRX, see *CoreJESD204BRX Handbook* from Libero SoC catalog.

2. **prbs\_checker\_0**— This block receives the 64-bit data from the CoreJESD204BRX IP core and checks if the received data is correct. It generates an error count and a status signal, which are sent to the GUI for status indication. The data checker checks only the PRBS sequences of the data generator.
3. **LED\_DEBUG\_BLK\_0**— This block debug the JESD204B link status and other errors. When the link is up, LEDs 4, 5, 6, 7, 8, 9 glow and LEDs 10 and 11 does not glow (with DIP 1, 2, 3, and 4 set low on the SW11 dip slide switch).

There are two instances of PF\_TPSRAM blocks, the PF\_TPSRAM\_C0\_0 block stores the JESD204B link status before sending it to the GUI. The PF\_TPSRAM\_C1\_0 block stores the data received from the CoreJESD204BRX before sending the data to the GUI.

PF\_INIT\_MONITOR and CoreReset\_PF IPs handle the reset mechanism as summarized in the following points.

- When the DEVICE\_INIT\_DONE signal from Init\_monitor block goes high, the transceiver is completely configured.
- CoreReset\_PF synchronizes resets to the respective user-specified clock domain. This ensures that when the assertion is asynchronous, the deassertion is synchronous to the clock.

The following table lists the important I/O signals of the JESD204B design.

**Table 3-1.** I/O Signals of the JESD204B Design

Signal	Description
<b>Input Signals</b>	
LANE0_RXD_P and LANE0_RXD_N	Receiver differential inputs of the transceiver
ARST_N	Reset signal obtained from the SW6 push button switch on the board
RX	Receiver of UART interface
REF_CLK_PAD_P_0 and REF_CLK_PAD_N_0	Differential reference clock obtained from the on-board 156.25 MHz oscillator
SEL_IN[3:0]	Signal mapped to DIPs 1, 2, 3, and 4 of SW11 dip slide switch used to debug the status and errors
<b>Output Signals</b>	

.....continued

Signal	Description
LANE0_TXD_P and LANE0_TXD_N	Transmitter differential outputs of the transceiver
LED_OUT[7:0]	LEDs 4, 5, 6, 7, 8, 9, 10, and 11 on the board that indicate whether link is up or down
TX	Transmitter of the UART interface

## 4. Simulating the PolarFire JESD204B Design [\(Ask a Question\)](#)

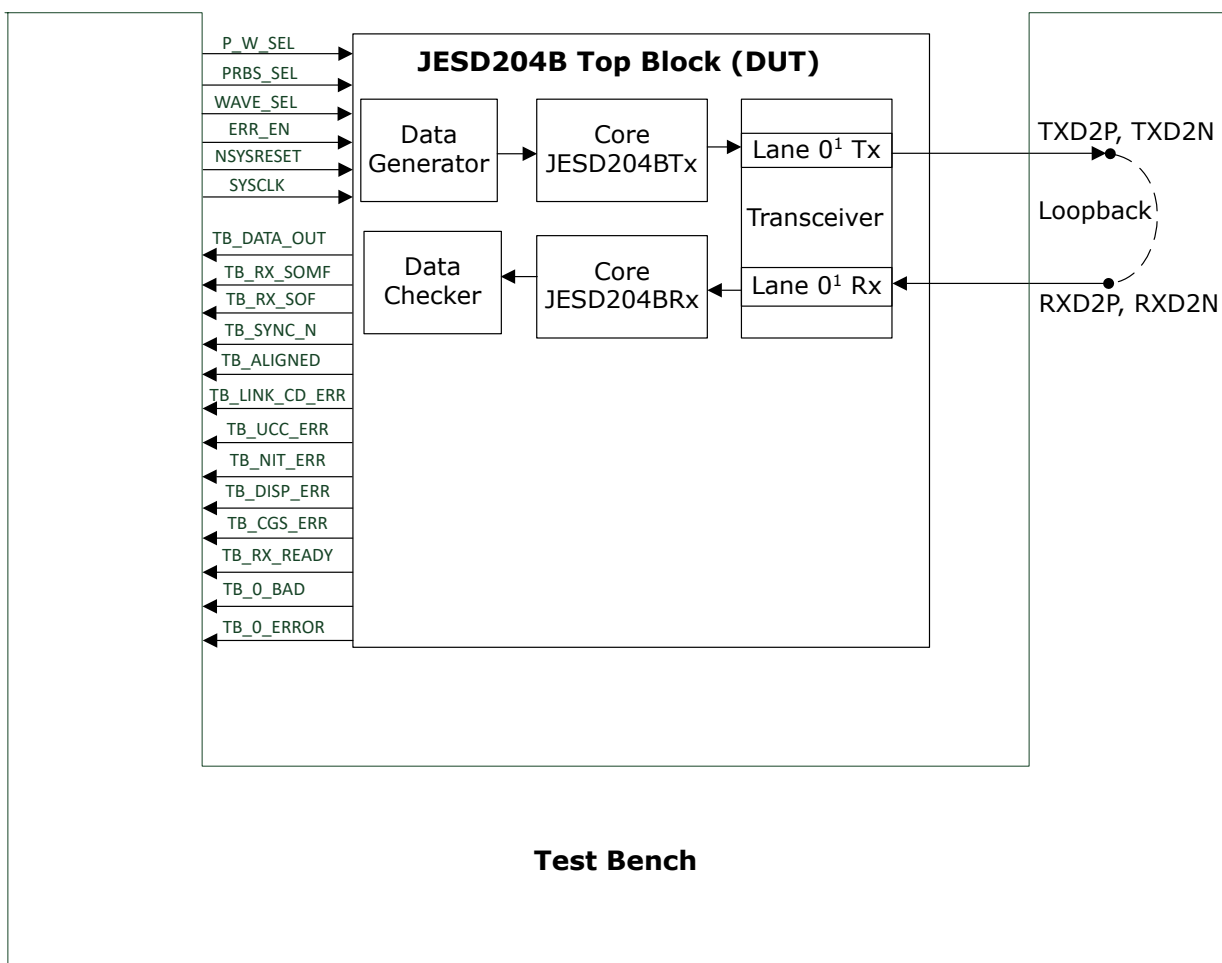
Before you begin:

1. Start Libero SoC and select **Project** -> **Tool Profiles**.
2. In the **Tool Profiles** window, select **Synthesis** and **Simulation** on the **Tools** panes and select the latest active installation directory paths for these two tools.

For Simulation, browse the design files folder, create Libero Project using provided TCL scripts, and click **Simulate** as shown in [Figure 4-1](#). See [10. Appendix B: Running the Tcl Script](#).

A testbench is provided to simulate the JESD204B PRBS pattern and waveform selection. [Figure 4-2](#) shows the interaction between testbench and the design.

**Figure 4-1.** Testbench and JESD204B Demo Design Interaction



1. In the PCB loopback design for Evaluation kit , Lane 2 and 3 are looped back.

The testbench generates the test selection for the PRBS input (PRBS7, PRBS15, PRBS23, and PRBS31) and waveform input (sine wave, sawtooth wave, triangle wave, and square wave). It also monitors the JESD204B output status signals (SYNC\_N, ALIGNED, and CGS\_ERR) for the verification of JESD204B phases, and PRBS checker output status signals O\_BAD and O\_ERROR[4:0].

The following table lists the simulation signals.

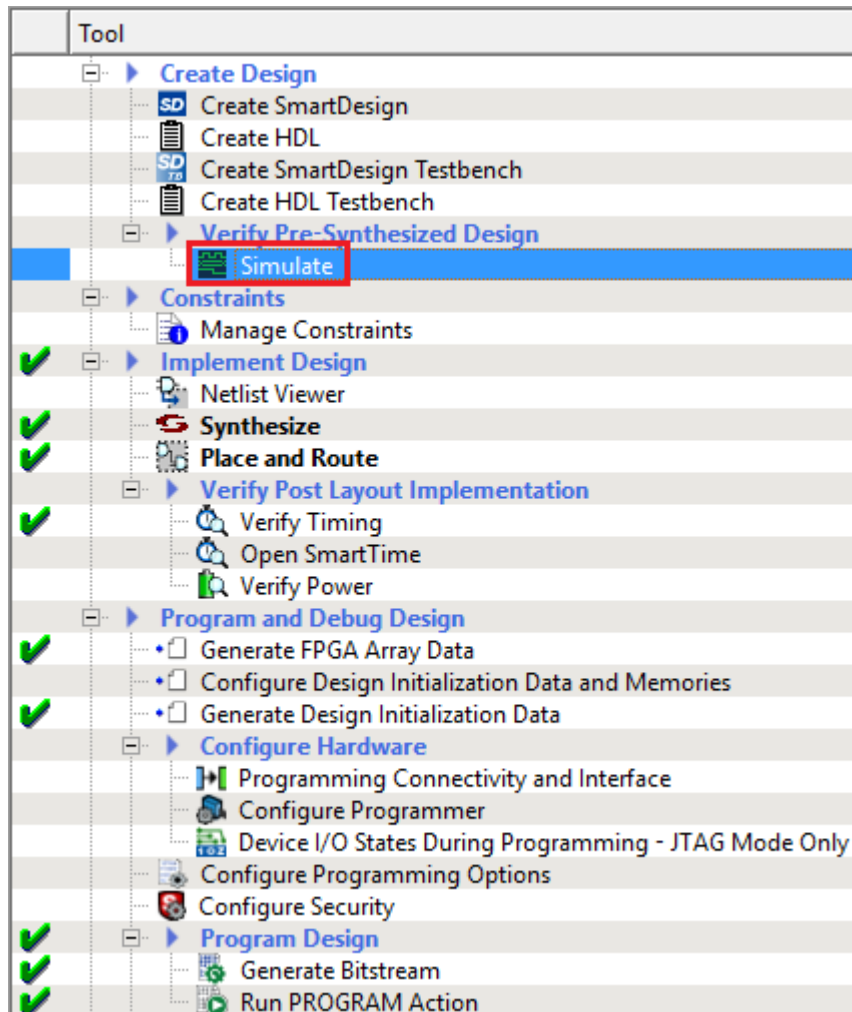
**Table 4-1.** Simulation Signals

Signal	Description
<b>Input Signals</b>	
P_W_SEL	Input to select the PRBS pattern or waveform
WAVE_SEL[1:0]	Input to select the type of waveform
PRBS_SEL[1:0]	Input to select the type of PRBS pattern
ERR_EN	Input to enable error in the PRBS pattern
NSYSRESET	Active low reset signal
SYSCLK	156.25 MHz generated clock for external loopback design. 125 MHz generated clock for internal loopback design.
<b>Output Signals</b>	
TB_DATA_OUT	Output data from CoreJESD204BRX
TB_RX_SOMF	SOMF_0[3:0] signal received from the CoreJESD204BRX block
TB_RX_SOF	SOF_0[3:0] signal received from the CoreJESD204BRX block
TB_SYNC_N	SYNC_N signal, which indicates the link status
TB_ALIGNED	ALIGNED signal, which indicates that all transceiver lanes are aligned
TB_LINK_CD_ERR	LINK_CD_ERR[0] signal, which indicates a link configuration data mismatch error
TB_UCC_ERR	UCC_ERR[0] signal, which indicates an unexpected control character error
TB_NIT_ERR	NIT_ERR[3:0] signal, which indicates the “not in table” error. This signal is controlled by LANE0_RX_CODE_VIOLATION[3:0]
TB_DISP_ERR	DISP_ERR[3:0] signal which indicates the disparity error. This signal is controlled by LANE0_RX_DISPARIITY_VIOLATION[3:0]
TB_CGS_ERR	CGS_ERR signal, which indicates the code group synchronization error. This signal is controlled by the CGS_ERR[0] signal.
TB_RX_READY	LANE0_RX_READY signal received from the transceiver block
TB_O_BAD	Error flag
TB_O_ERROR[4:0]	Number of errors occurred during PRBS check

To run the simulation, go to Stimulus Hierarchy and verify if PF\_JESD204B\_SA\_TOP\_TB\_8b file is set as active stimulus. If not set, right-click on the file and select Set as active stimulus.

In the **Design Flow** tab, under **Verify Pre-Synthesized Design**, double click **Simulate** to simulate the design. The **Simulate** option is highlighted in [Figure 4-2](#).

Figure 4-2. Simulating the Design



When the simulation is initiated, ModelSim compiles all the design source files, runs the simulation, and configures the waveform viewer to show the simulation signals.

#### 4.1 Simulation Flow [\(Ask a Question\)](#)

The following steps describe the JESD204B testbench simulation flow:

1. At the start, the NSYSRESET signal resets all of the components.
2. After the transceiver block is initialized, the TB\_RX\_READY signal is asserted high.
3. The JESD204BRX issues a synchronization request by asserting the TB\_SYNC\_N low.
4. The JESD204BTX responds to the request by sending k28.5 characters to the JESD204RX.
5. The JESD204BRX block checks the k28.5 characters and checks CGS\_ERR signal for any errors.
6. Once JESD204BRX block receives at least four k28.5 characters, Code Group Synchronization (CGS) is complete and TB\_SYNC\_N is deasserted.
7. After the successful completion of the CGS phase, the JESD204BTX block starts the ILA sequence by transmitting four multi-frames in the following sequence:
  - First frame at TB\_TX\_SOMF = 0x8
  - Second frame at TB\_TX\_SOMF = 0x2
  - Third frame at TB\_TX\_SOMF = 0x8



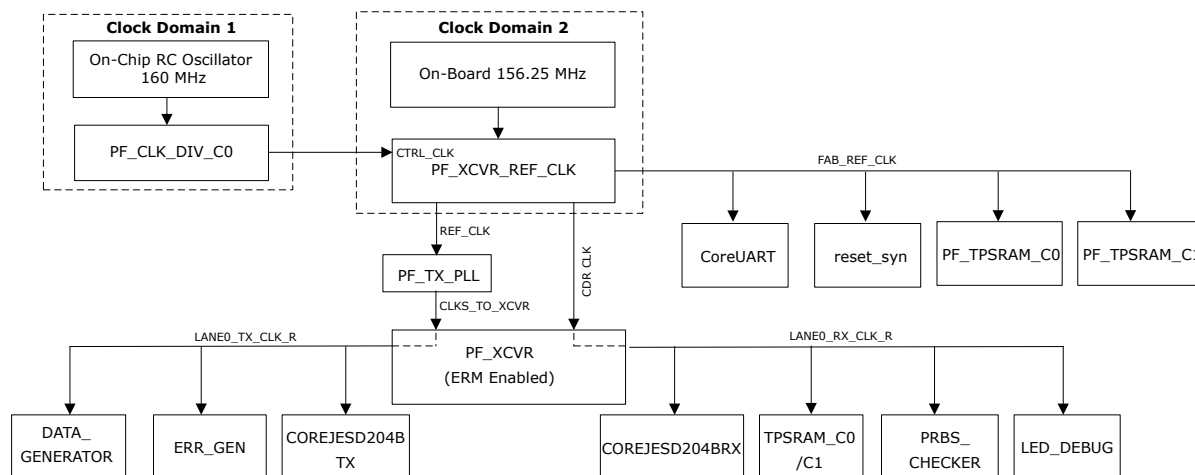
## 5. Clocking Structure (Ask a Question)

For the Evaluation Kit design, the on-board 156.25 MHz crystal oscillator (for the SMA loopback design) and the 125 MHz crystal oscillator (for the PCB loopback design) drive the XCVR reference clock. This clock provides the clock to the TX\_PLL and PF\_XCVR\_0 blocks. The FAB\_REF\_CLK of the XCVR\_REF\_CLK block drives reset\_syn, the read clock of TPSRAM\_C0 and TPSRAM\_C1, along with the UART block. The LANE0\_TX\_CLK\_R of the PF\_XCVR\_0 block drives the ERR\_GEN, CoreJESD204BTX, and DATA\_GENERATOR blocks. Also, the LANE0\_RX\_CLK\_R of the PF\_XCVR\_0 block drives the LED\_DEBUG, PRBS\_CHECKER, CoreJESD204BRX, and the write clock of TPSRAM\_C0 and TPSRAM\_C1 blocks.

An on-chip RC oscillator (PF\_OSC) drive the enhanced receiver management logic of the transceiver.

**➔ Important:** If there is any change in the data-rate or XCVR reference clock of the transceiver; reconfigure COREUART.

Figure 5-1. Clocking Structure



\*For Evaluation kit, 156.25 MHz oscillator is used for the SMA loopback design and 125 MHz oscillator is used for the PCB loopback design.

For the JESD204B design, LANE0\_TX\_CLK\_R and LANE0\_RX\_CLK\_R clocks are set to Regional (Deterministic) in the XCVR configurator.

The following table lists all of the clocks used in the design, their source, frequency, and purpose.

Table 5-1. Clocks

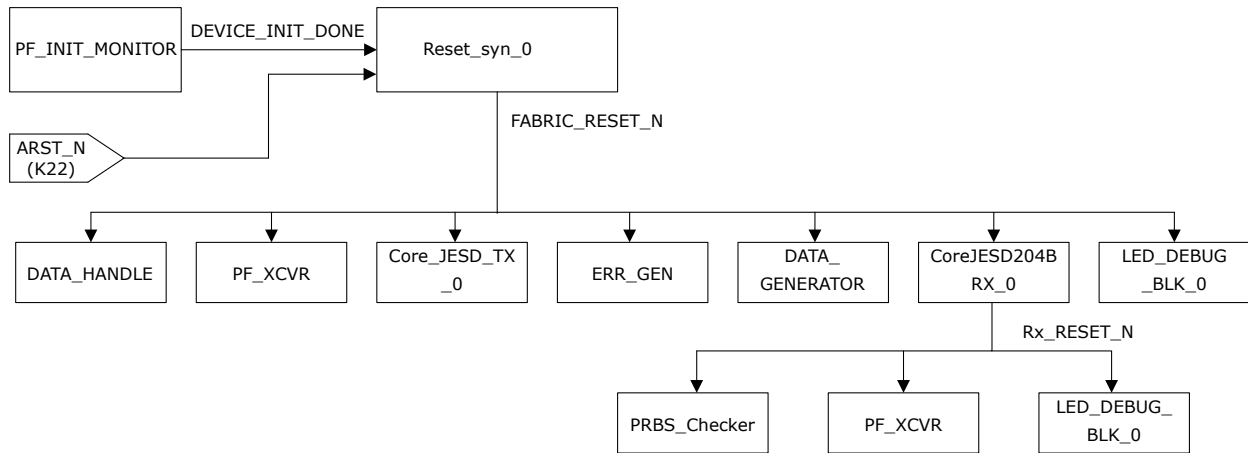
Clock Name	Source	Frequency	Purpose
FAB_REF_CLOCK	Reference clock from the oscillator	156.25 MHz/125 MHz <sup>1</sup>	Clock for the fabric logic that is, reset synchronizer, read clock of TPSRAM blocks, UART block.
REF_CLK	Reference clock from the oscillator	156.25 MHz/125 MHz <sup>1</sup>	CDR reference clock for the transceiver
LANE0_TX/RX_CLK_R	Transceiver generated TX/RX clock	156.25 MHz/125 MHz <sup>1</sup>	Clock for the transmit and receive modules in the fabric
CTRL_CLK	On-chip RC oscillator (PF_OSC)	40 MHz (through clock divider PF_CLK_DIV_C0)	Clock for the enhanced receiver management logic

<sup>(1)</sup> For SMA and PCB loopback designs (Evaluation kit), the frequency is 156.25 MHz and 125 MHz respectively.


## 6. Reset Structure [\(Ask a Question\)](#)

The DEVICE\_INIT\_DONE and external reset ARST\_N signal is mapped to K22 on the evaluation board and initiates the reset signal (FABRIC\_RESET\_N) from the res\_syn\_0 block. This provides a reset to the CoreJESD204BRX (RESET\_N of CoreJESD204BRX), UART block, DATA\_GENERATOR, ERR\_GEN, CoreJESD204BTX, LED\_DEBUG, and PF\_XCVR (LANE0\_PMA\_ARST\_N) modules of the design. The RX\_RESET\_N output from the COREJESD204BRX provides a reset to the LANE0\_PCS\_ARST\_N inputs of the PF\_XCVR\_0, PRBS\_CHECKER, and LED\_DEBUG modules. The PF\_INIT\_MONITOR provides a reset to the CTRL\_ARST\_N input of the PF\_XCVR\_0 module. The following figure shows the reset structure.

**Figure 6-1.** Reset Structure



## 7. Setting Up the Demo [\(Ask a Question\)](#)

 **Important:** To run the Libero design using TCL script, see [10. Appendix B: Running the Tcl Script](#).

After generating the bit stream, the PolarFire device must be programmed. To program the PolarFire device on Evaluation kit, perform the following steps:

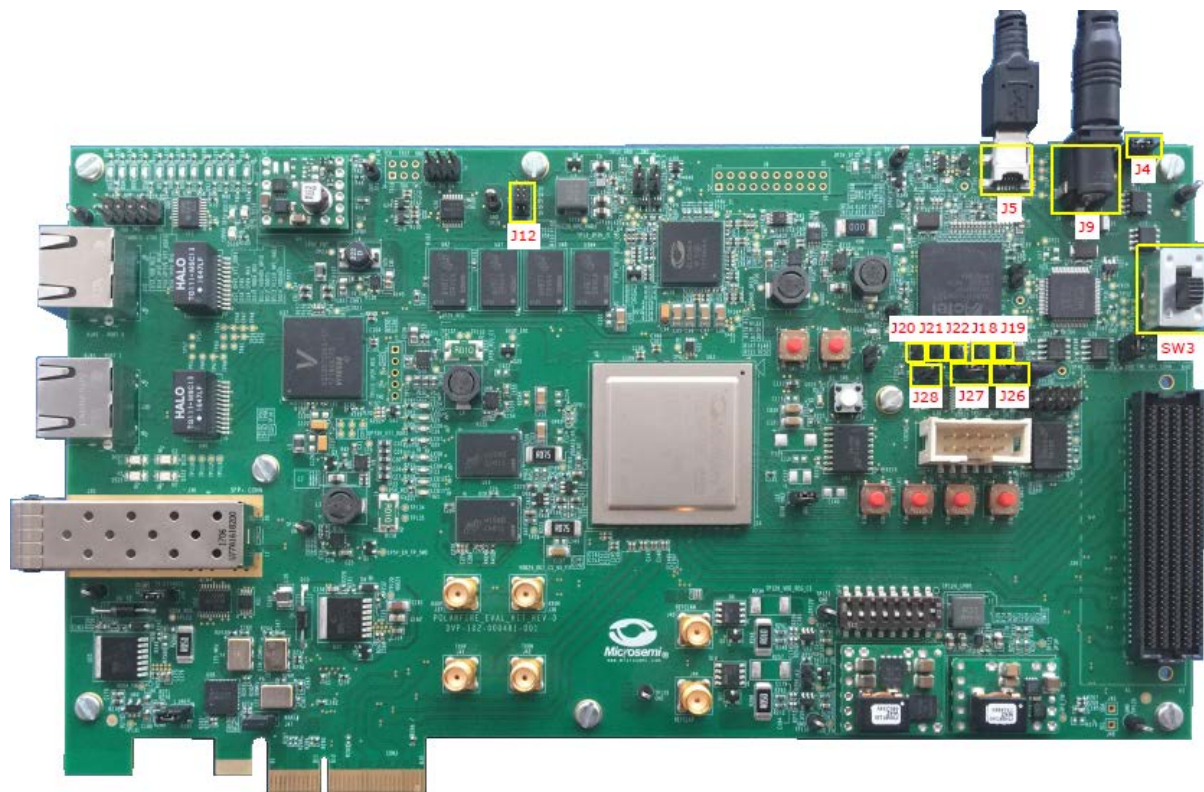
1. Ensure that the jumper settings on the board are same as listed in the following table.

**Table 7-1.** Jumper Settings

Jumper	Description
J18, J19, J20, J21, J22	Close pin 2 and 3 for programming the PolarFire FPGA through FTDI
J28	Close pin 1 and 2 for programming through the on-board FlashPro5
J26	Close pin 1 and 2 for programming through the FTDI SPI
J27	Close pin 1 and 2 for programming through the FTDI SPI
J4	Close pin 1 and 2 for manual power switching using SW3
J12	Close pin 3 and 4 for 2.5 V

2. Connect the power supply cable to the J9 connector on the board.
3. Connect the USB cable from the host PC to the J5 (FTDI port) on the board.
4. Power on the board using the **SW3** slide switch.
5. For external loopback demo, connect **TXN** to **RXN** and **TXP** to **RXP** using the 2 SMA to SMA cables as shown in the following figure.  
The following figure shows the board setup for external loopback demo.

**Figure 7-1.** Board Setup (Evaluation Kit)



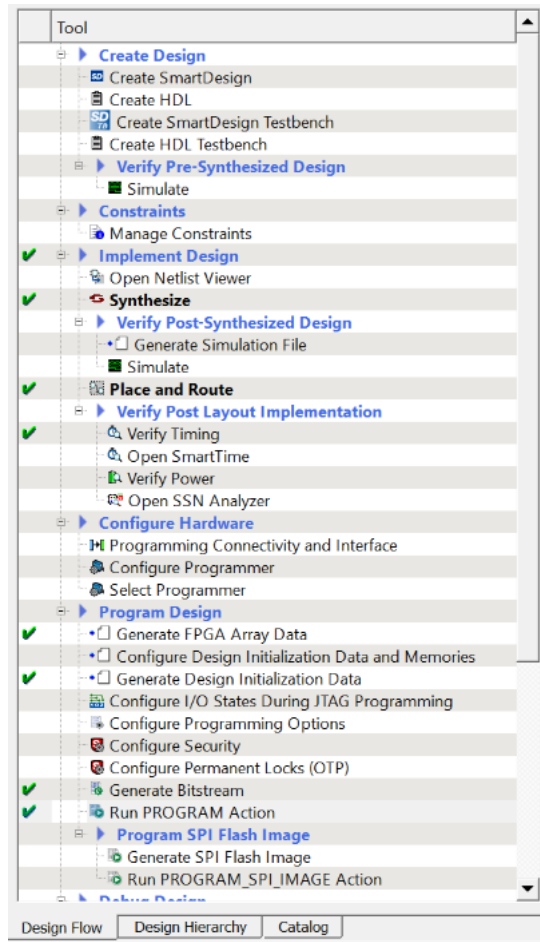
When the board is powered up, power supply LEDs DS3 to DS14 glow. For more information about LEDs on the PolarFire Evaluation Board, see [UG0747: PolarFire FPGA Evaluation Kit User Guide](#).

**➔ Important:** For PCB loopback demo, SMA cables are not required. User can skip Step 5.

6. Double-click **Run PROGRAM Action** from the **Libero > Design Flow** tab.
7. Right-click **Run Program Action** and select **View Report** to view the corresponding log file in the **Reports** tab.

When the device is successfully programmed, a green tick mark appears as shown in the following figure.

Figure 7-2. Programming the Device



After programming the device, see [8. Running the Demo](#) to run the JESD204B stand-alone demo.

## 8. Running the Demo (Ask a Question)

This chapter describes how to install and use the JESD204B GUI to select the test patterns and monitor the loopback data. The GUI enables the selection of different PRBS test patterns as input, and displays the JESD204B status signals and PRBS status received from the board. The Waveform tab displays the output waveform samples received from the board for each waveform selected as input.

The following procedure assumes that:

- The PolarFire Evaluation board is connected.
- The PolarFire FPGA is programmed with the JESD204B design.

To run the JESD204B demo, perform the following steps:

1. Install the **JESD204B\_GUI** application (setup.exe) from the following design files folder:  
mpf\_an5341\_v2024p1\_df\GUI
2. Double-click the JESD204B\_GUI application from the installation directory to start the GUI application.
3. Select the COM port number that is detected to configure the serial port.



**Important:** In **Device Manager** on the host PC, under Ports, select the COM port associated with the USB serial converter C. To determine the COM port, check the **Location** field in the properties of each COM port.

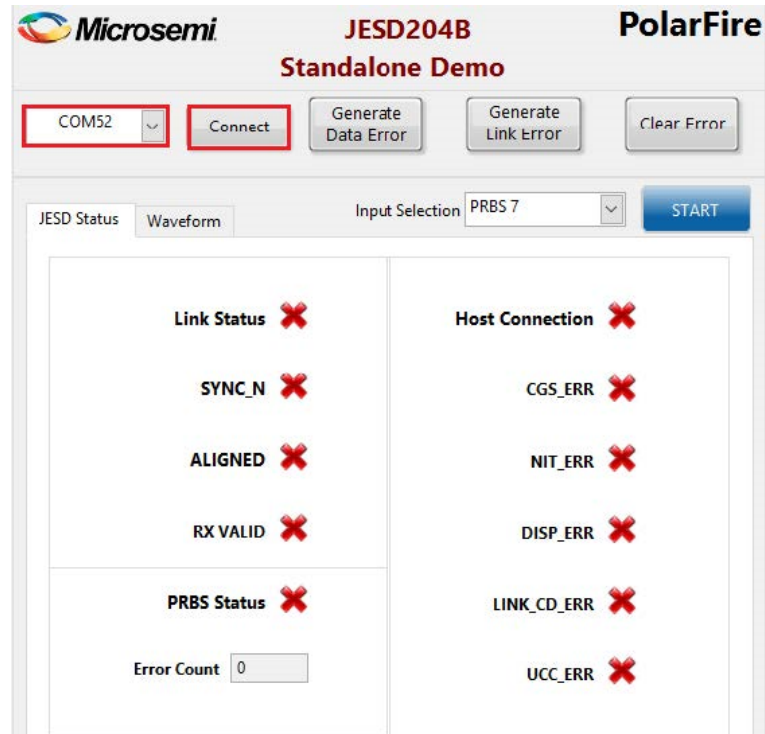
The following table lists the status signals displayed in the JESD204B GUI.

**Table 8-1.** Status Signals in JESD204B GUI

Status	Description
Host Connection	Status of the UART communication
Link Status	Communication link status between TX and RX
SYNC_N	Signal which indicates the JESD link status
ALIGNED	Indicates that all transceiver lanes are aligned
RX VALID	Indicates that the Rx data is valid. In 8b10b mode, the RX VAL is qualified, comma alignment has occurred and the CDR is locked.
PRBS status	Indicates the occurrence of PRBS error. If green tick mark then no PRBS error occurred.
Error count	Number of errors that occurred during PRBS check
CGS_ERR	Indicates status of the code group synchronization error. If green tick mark then no CGS error occurred.
NIT_ERR	Indicates the “not in table” error. If green tick mark then no NIT error occurred.
DISP_ERR	Indicates the disparity error. If green tick mark then no DISP error occurred.
LINK_CD_ERR	Indicates a link configuration data mismatch error. If green tick mark then no LINK_CD error occurred.
UCC_ERR	Indicates an “unexpected control character” error. If green tick mark then no UCC error occurred.

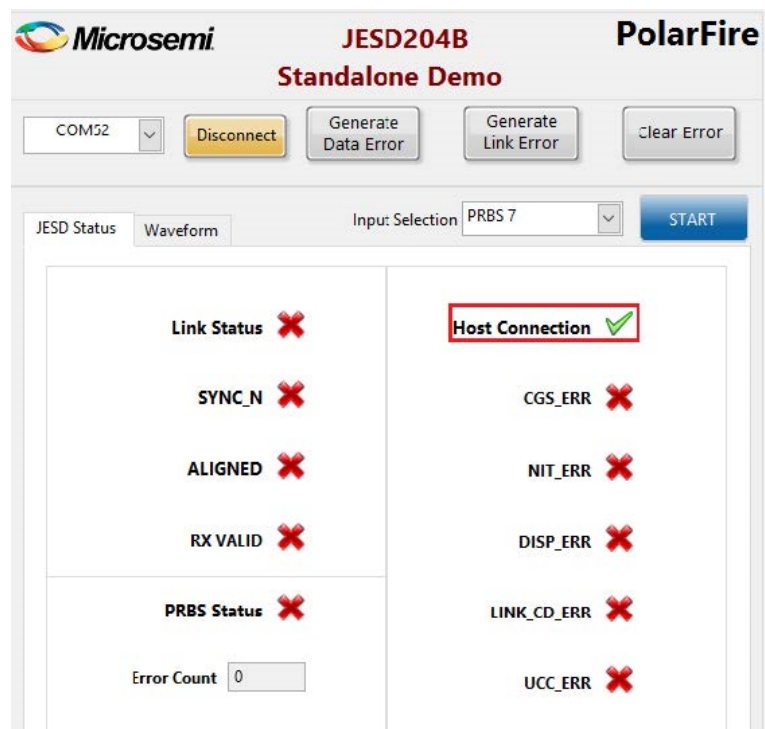
4. Click **Connect** to connect the GUI to the board through the selected port, as shown in the following figure.


Figure 8-1. Selecting COM Port and Connecting



After successfully connecting, the **Host Connection** status changes to a green tick mark as shown in the following figure.

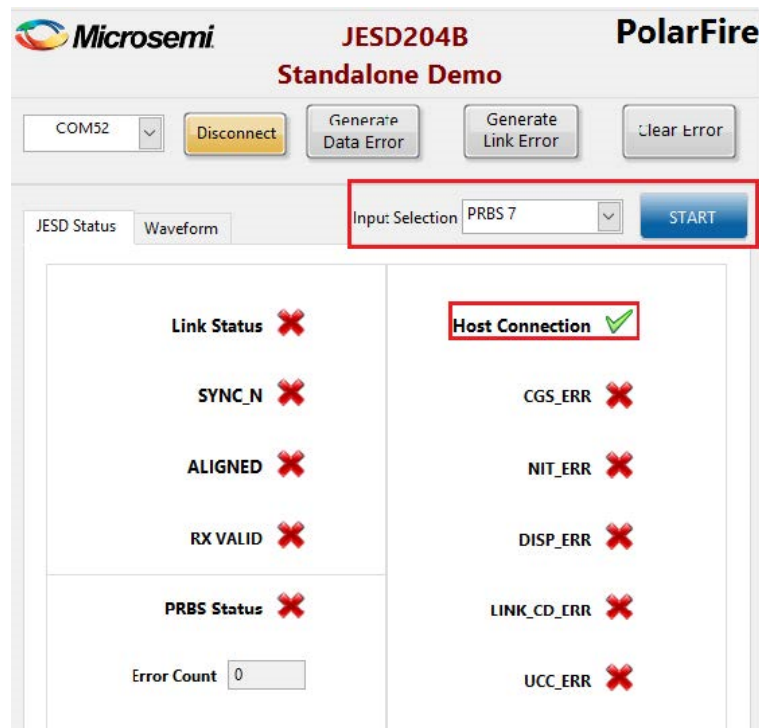
Figure 8-2. Host Connection Status



 **Important:** Port numbers may vary. Select the correct port number from the list.

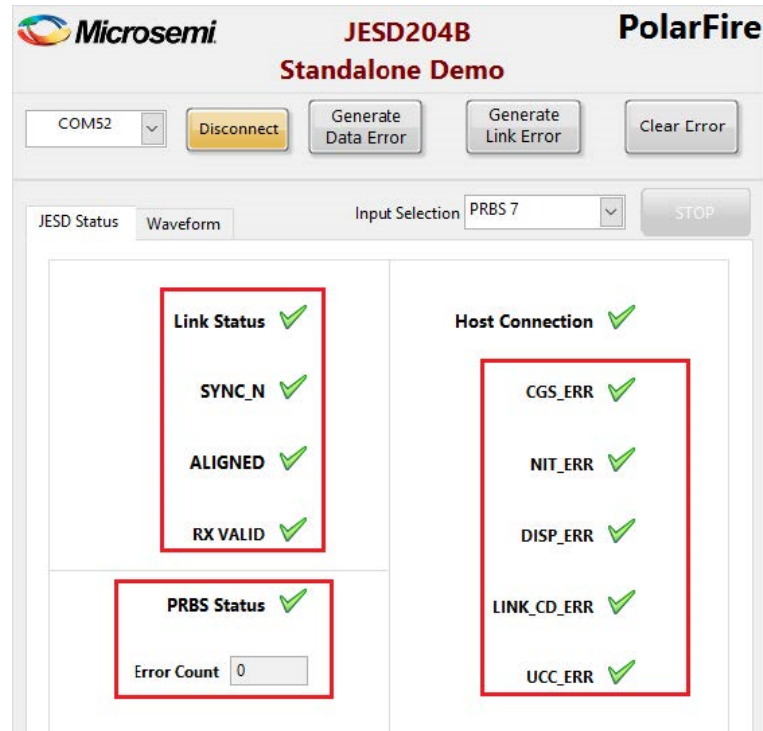
5. Reset the system using the push button K22 (Evaluation kit).
6. Select the pattern to be transmitted using the **Input selection** drop-down and click **START**. The following figure shows the PRBS7 selection.

Figure 8-3. PRBS7 Input Selection



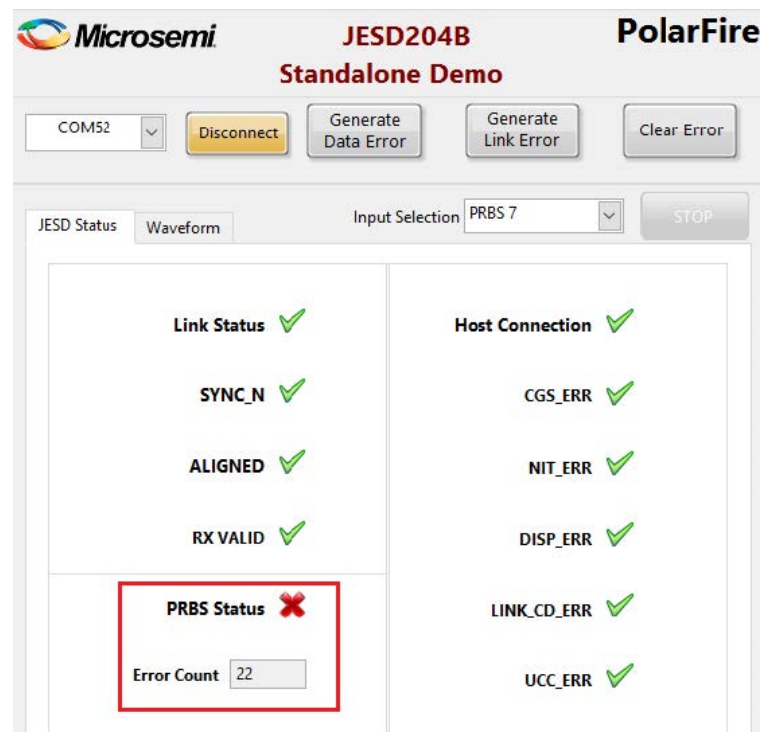
The selected pattern is sent over the serial transmit link. The looped back data is received by the receiver and checked for errors. The status can be monitored using the status signals on the GUI at any time as shown in the following figure.

Figure 8-4. Link Status and JESD204B Status



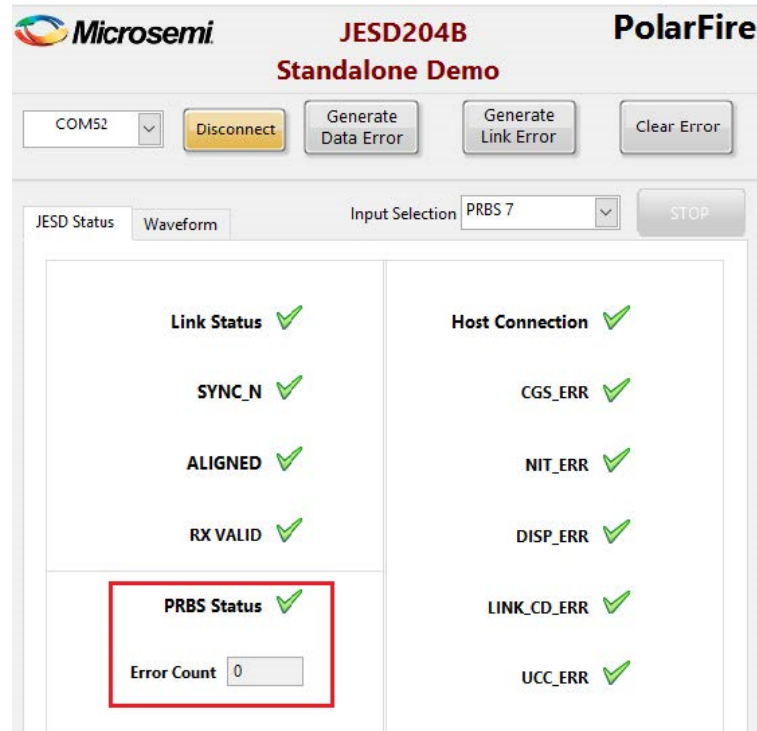
- Click **Generate Data Error** to generate error in the PRBS data and observe the error status using **PRBS Status** and **Error Count** as shown in the following figure.

Figure 8-5. Generate Data Error



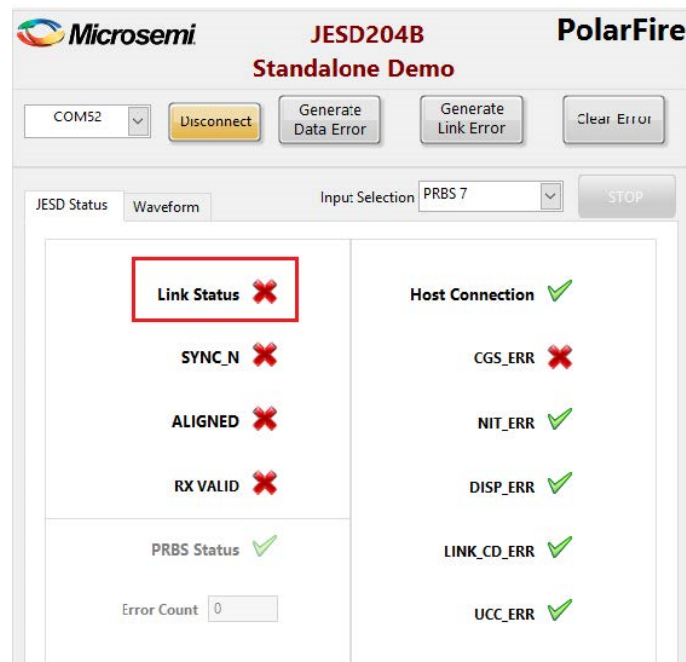
- Click **Clear Error** to stop generate error in the PRBS data and observe that **PRBS Status** turns green, and the **Error Count** is zero as shown in the following figure.

Figure 8-6. Clear Data Error



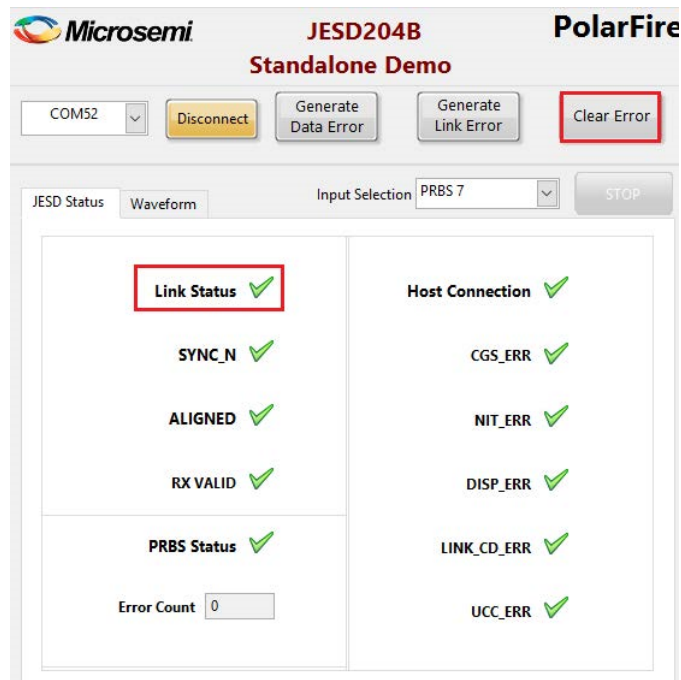
- Click **Generate Link Error** to generate error between the CoreJESD204BTX and the transceiver lane and observe Link Status, SYNC\_N, ALIGNED, RX VALID, and CGS\_ERROR indicators turn red as shown in the following figure.

Figure 8-7. Generating Link Error



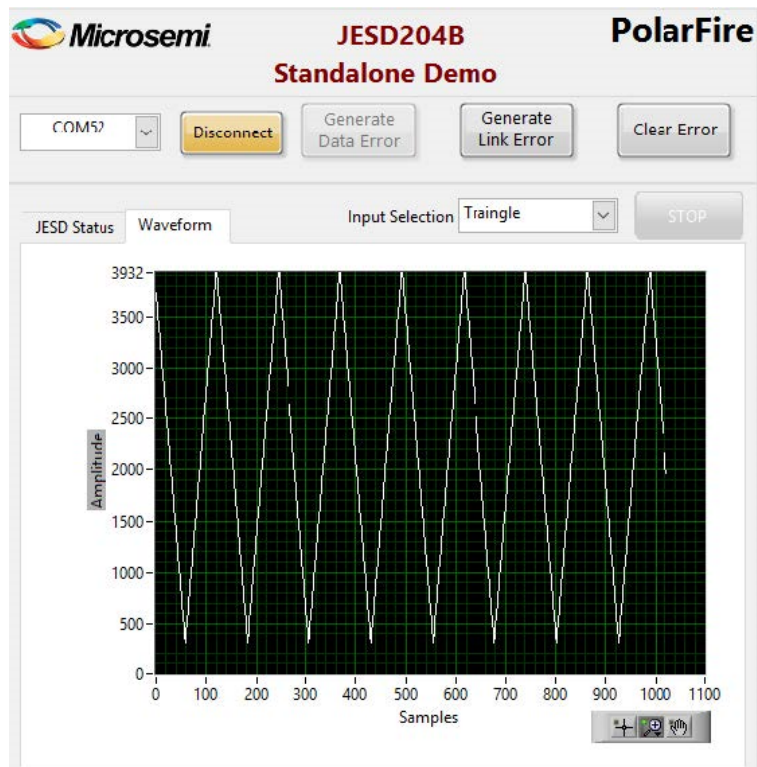
- Click **Clear Error** to stop generating the link error and observe the Link Status and JESD204B status signals change to green tick marks as shown in the following figure.

Figure 8-8. Clearing Link Error



11. Select **Triangle** from the **Input Selection** drop-down to change the pattern. The selected pattern is sent over the serial transmit link and received by the CoreJESD204BRX. The status can be monitored using the status signals on the GUI.
12. Click **Waveform** tab to view the Triangle waveform received from CoreJESD204BRX as shown in the following figure.

Figure 8-9. Triangle Waveform



13. Click **Stop** to end the demo and close the GUI.

This concludes the demo. The demo described the PolarFire JESD204B design and how to run the demo using the GUI.

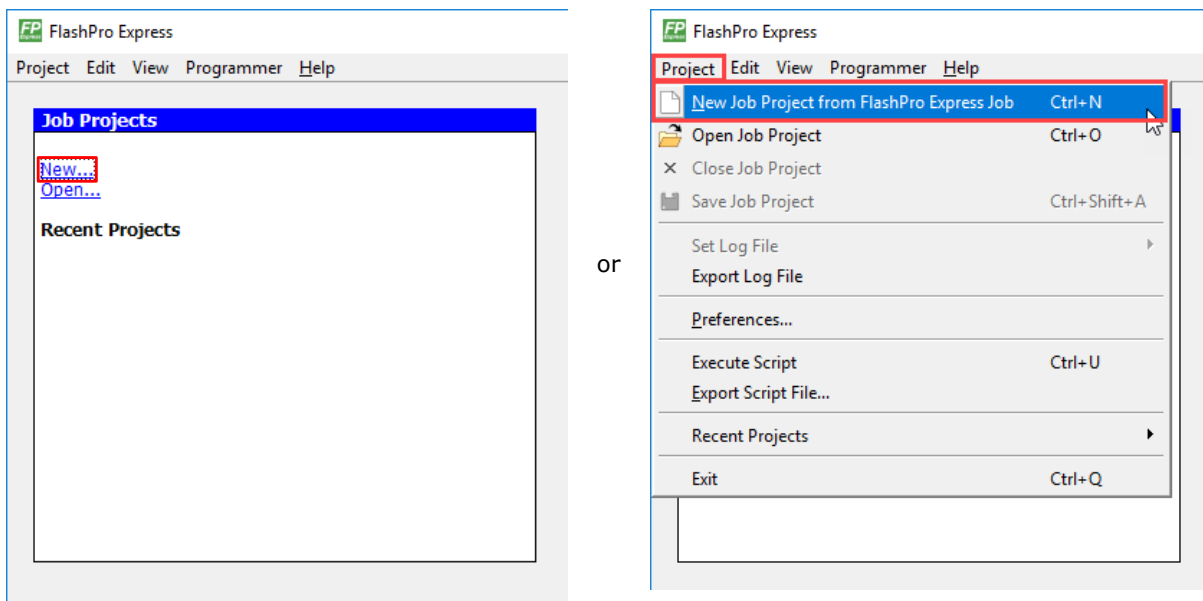
## 9. Appendix: Programming the Device Using FlashPro Express [\(Ask a Question\)](#)

This section describes how to program the PolarFire device with the programming job file using FlashPro Express. The job file is available at the following design files folder location:  
mpf\_an5341\_v2024p1\_df\Programming\_Job.

To program the device, perform the following steps:

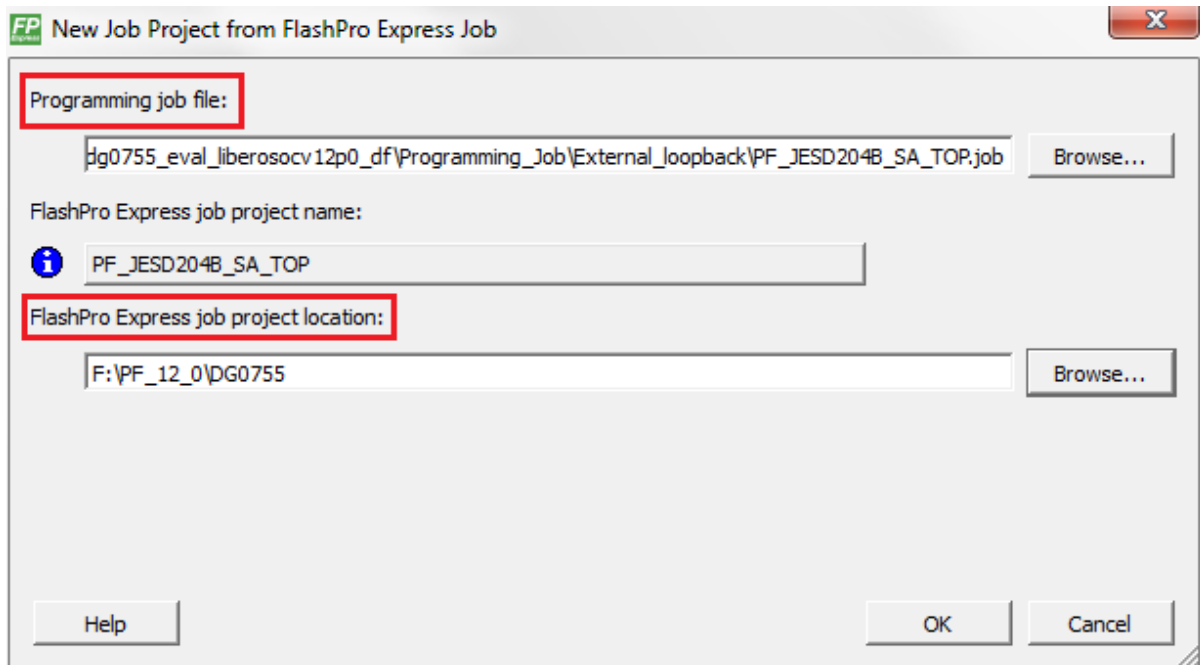
1. On the host PC, launch the **FlashPro Express software**.
2. Click **New** or select **New Job Project from FlashPro Express Job** from **Project** menu to create a new job project, as shown in the following figure.

**Figure 9-1.** FlashPro Express Job Project



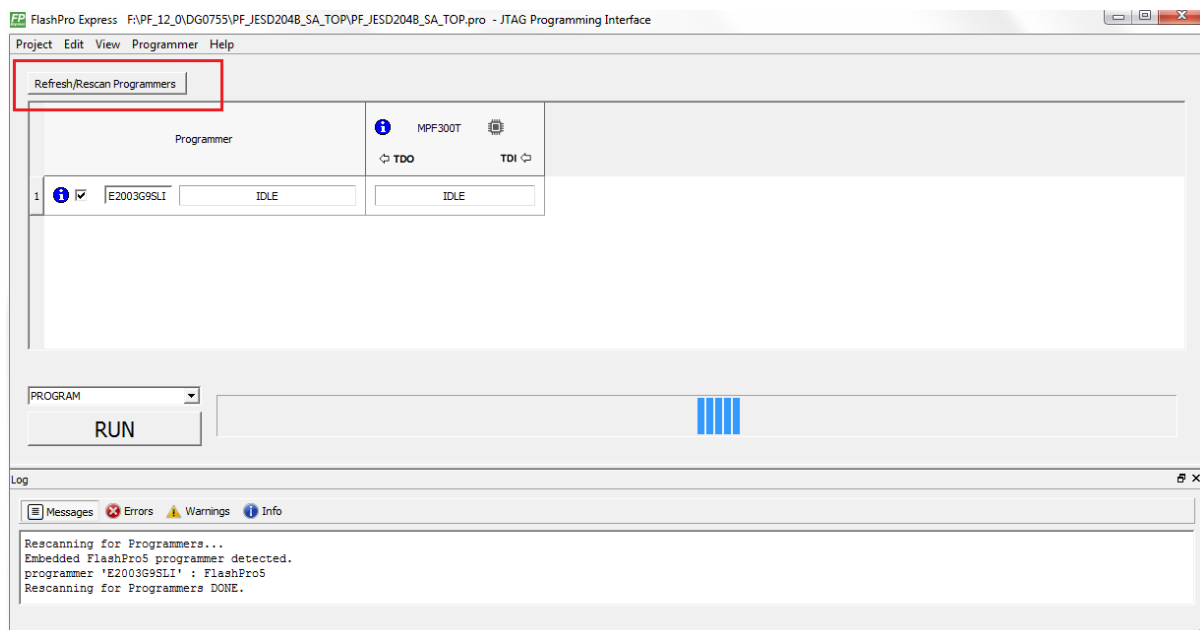
3. Enter the following in the **New Job Project from FlashPro Express Job** dialog box:
  - **Programming job file:** Click **Browse** and navigate to the location where the job file is located and select the file. The default location is:  
<download\_folder>\mpf\_an5341\_v2024p1\_df\Programming\_Job.
  - **FlashPro Express job project location:** Click **Browse** and navigate to the FlashPro Express project location.

Figure 9-2. New Job Project from FlashPro Express Job

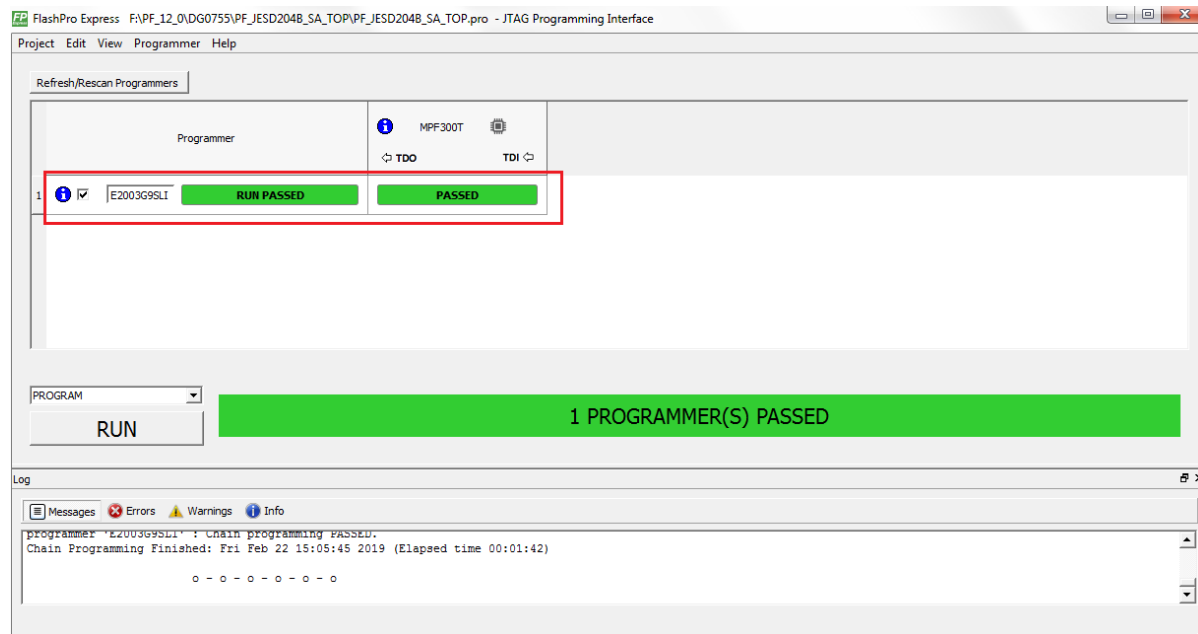


4. Click **OK**. The required programming file is selected and ready to be programmed in the device.
5. The **FlashPro Express** window appears as shown in the following figure. Confirm that a programmer number appears in the **Programmer** field. If not, confirm the board connections and click **Refresh/Rescan Programm**ers.

Figure 9-3. Programming the Device



6. Click **RUN**. When the device is programmed successfully, a **RUN PASSED** status is displayed as shown in the following figure.

**Figure 9-4.** FlashPro Express—RUN PASSED

7. Close **FlashPro Express** or click **Exit** in the **Project** tab.

## 10. Appendix B: Running the Tcl Script [\(Ask a Question\)](#)

TCL scripts are provided in the design files folder under directory TCL\_Scripts. If required, the design flow can be reproduced from Design Implementation till generation of job file.

To run Tcl, perform the following steps:

1. Launch the Libero software.
2. Select **Project > Execute Script**.
3. Click **Browse** and select `script.tcl` from the downloaded TCL\_Scripts directory.
4. Click **Run**.

After successful execution of the Tcl script, the Libero project is created within the top directory. For more information, see `mpf_an5341_v2024p1_df/TCL_Scripts/TCL_Scripts_readme.txt`.

For more information about Tcl scripts and commands, see `TCL_Scripts_readme.txt` file and [Tcl Commands Reference Guide](#). Contact Technical Support for any queries about running the Tcl script.

## 11. Appendix 3: References (Ask a Question)

This section lists the documents that provide more information about the JESD204B standard and IP cores used in the demo design.

- For more information about the JESD204B interface standard, see [JEDEC website](#).
- For more information about PolarFire transceiver blocks, PF\_TX\_PLL, and PF\_XCVR\_REF\_CLK, see [PolarFire FPGA and PolarFire SoC FPGA Transceiver User Guide](#).
- For more information about PF\_TPSRAM (Two-Port Large SRAM), see [PolarFire FPGA and PolarFire SoC FPGA Fabric User Guide](#).
- For more information about CoreJESD204BTX, see *CoreJESD204BTX Handbook* from Libero SoC catalog.
- For more information about CoreJESD204BRX, see *CoreJESD204BRX Handbook* from Libero SoC catalog.
- For more information about Libero, ModelSim, and Synplify, see [Libero SoC web page](#).
- For more information about PolarFire FPGA Evaluation Kit, see [UG0747: PolarFire FPGA Evaluation Kit User Guide](#).

## 12. Revision History [\(Ask a Question\)](#)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

**Table 12-1.** Revision History

Revision	Date	Description
A	06/2024	The following is the list of changes in revision A of the document: <ul style="list-style-type: none"> <li>The document was migrated to the Microchip template.</li> <li>The document number was updated from 50200755 to DS00005341.</li> <li>The document ID was updated from DG0755 to AN5341.</li> <li>Updated the document for Libero® v2024.1.</li> </ul>
13.0	—	The following is a summary of the changes made in this revision. <ul style="list-style-type: none"> <li>Updated the document for Libero SoC v2022.1.</li> <li>Removed information related to Splash kit.</li> </ul>
12.0	—	The following is a summary of the changes made in this revision. <ul style="list-style-type: none"> <li>Updated the document for Libero SoC v12.3.</li> <li>Replace .</li> <li>Added <a href="#">10. Appendix B: Running the Tcl Script</a>.</li> </ul>
11.0	—	Added <a href="#">10. Appendix B: Running the Tcl Script</a> .
10.0	—	The following is a summary of the changes made in this revision. <ul style="list-style-type: none"> <li>Updated the document for Libero SoC v12.2.</li> <li>Removed the references to Libero version numbers.</li> </ul>
9.0	—	Updated the document for Libero SoC v12.0.
8.0	—	The following is a summary of the changes made in this revision. <ul style="list-style-type: none"> <li>Updated the document for Evaluation and Splash kit.</li> <li>Updated the document for Libero SoC PolarFire v2.3.</li> </ul>
7.0	—	The document was updated for Libero SoC PolarFire v2.2.
6.0	—	The document was updated for Libero SoC PolarFire v2.1.
5.0	—	The following is a summary of the changes made in this revision. <ul style="list-style-type: none"> <li>The document was updated to include IP core.</li> <li><a href="#">1. Design Requirements</a> was edited to add CORERESSET_PF details and, JESD204B Interface Design, was updated with CORERESSET_PF IP core.</li> </ul>
4.0	—	The following is a summary of the changes made in this revision. <ul style="list-style-type: none"> <li>The document is updated to include features and enhancements introduced in the Libero SoC PolarFire v2.0 release.</li> <li>Updated the GUI screens and COM port details with respect to the Libero SoC PolarFire v2.0 release.</li> </ul>
3.0	—	The following is a summary of the changes made in this revision. <ul style="list-style-type: none"> <li>The document was updated to include features and enhancements introduced in the Libero SoC PolarFire v1.1 SP1 release.</li> <li>Information about resource utilization was updated.</li> <li>List of reference was added. For more information, see <a href="#">11. Appendix 3: References</a>.</li> </ul>
2.0	—	The following is a summary of the changes in this revision. <ul style="list-style-type: none"> <li>The document was updated for Libero SoC PolarFire v1.1 release.</li> <li>Information about resource utilization was added.</li> </ul>
1.0	—	Initial release.

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