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Building a 10-bit Bridge Sensing Circuit using the PIC16C6XX and MCP601 Operational Amplifier

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INTRODUCTION

Sensors that use Wheatstone bridge configurations, such as pressure sensors, load cells, or thermistors have a great deal of commonality when it comes to the signal conditioning circuit. This application note delves into the inner workings of the electronics of the signal conditioning path for sensors that use Wheatstone bridge configurations. Analog topics such as gain and filtering circuits will be explored. This discussion is complemented with digital issues such as digital filtering and digital manipulation techniques. Overall, this note's comprehensive investigation of hardware and firmware provides a practical solution including error correction in the data acquisition sensor system.

A sensor that is configured in a Wheatstone bridge typically supplies a low level, differential output signal. The application problem the designer is challenged with is to capture this small signal and eventually convert it to a digital format that gives an 8 to 12 bit representation of the signal.

The inexpensive design strategy shown in the block diagram in Figure 1 uses a low pass filter prior to digitization. The conversion from analog to digital is performed with the microcontroller (MCU). The MCU used in this circuit must have internal analog functions such as a voltage reference and a comparator. These internal analog building blocks are used to implement a first order modulator. This is combined with the MCU's computing power where a digital filter can be implemented.
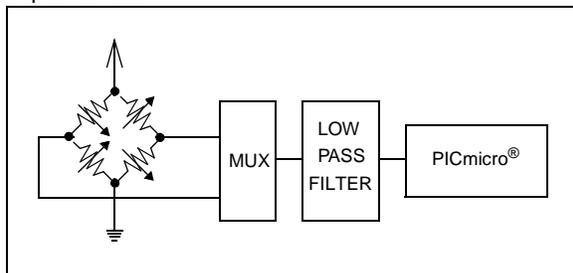

FIGURE 1: *The bridge sensor signal conditioning chain filters high frequency noise in the analog domain then immediately digitizes it with a microcontroller.*

BRIDGE SENSOR DATA ACQUISITION CIRCUIT IMPLEMENTATION

Figure 2 gives a detailed circuit for the block diagram shown in Figure 1. The analog portion of this circuit consists of the sensor (in this example a 1.2kΩ, 2mV/V load cell), an analog multiplexer, an amplifier and an R/C network. (A complete list of the load cell's specifications is given in Table 1.) An analog multiplexer is used to switch the two sensor outputs between a single ended signal path to the controller. The amplifier is configured as a buffer and used to isolate the sensor load from the R/C network. The R/C network implements the integrator function of a first order modulator. This network can also be used to adjust the input range to the MCU.

Rated Capacity	32 ounces (896 g)
Excitation	$5V_{DC}$ to $12V_{DC}$
Rated Output	2mV/V ±20%
Zero Balance	±0.3mV/V
Operating Temperature	-55 to 95°C
Compensated Temperature	-5 to 50°C
Zero Balance over Temperature	0.036% FS/°C
Output over Temperature	0.036% FS/°C
Resistance	1200Ω ±300Ω
Safe Overload	150%
Full-Scale Deflection	0.01" to 0.05"

TABLE 1: *Load Cell, LCL816G (Omega) Specifications.*
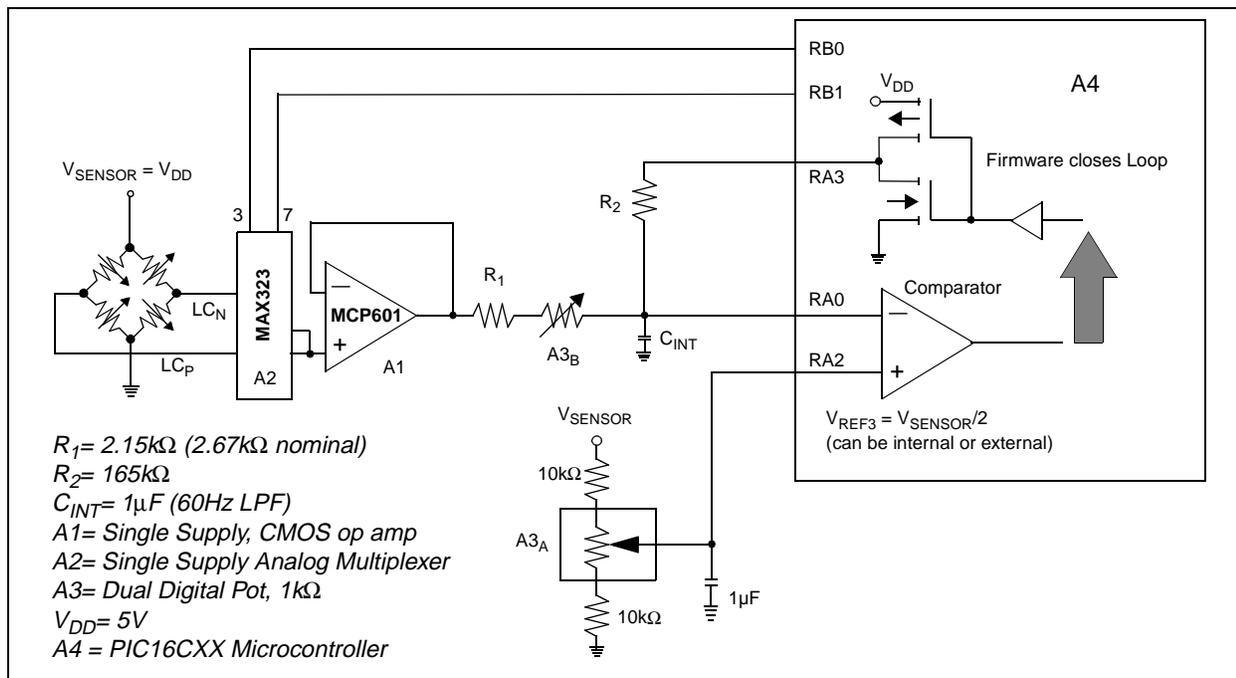
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FIGURE 2: *The combination of an R/C network and the microcontroller's analog peripherals can be used to perform an A/D conversion function.*

In this circuit, the integrator function of the modulator is implemented with an external capacitor, C_{INT}. When RA3 of the PIC16C6XX is set high, the voltage at RA0 increases in magnitude. This occurs until the output of the comparator (CMCON<6>) is triggered low. At this point, the driver to the RA3 output is switched from high to low. Once this has transpired, the voltage at the input to the comparator (RA0) decreases. This occurs until the comparator is tripped high. At this point, RA3 is set high and the cycle repeats. While the modulator section of this circuit is cycling, two counters are used to keep track of the time and of the number of ones versus zeros that occur at the output of the comparator. The firmware flow chart for this conversion process is shown in Figure 3.
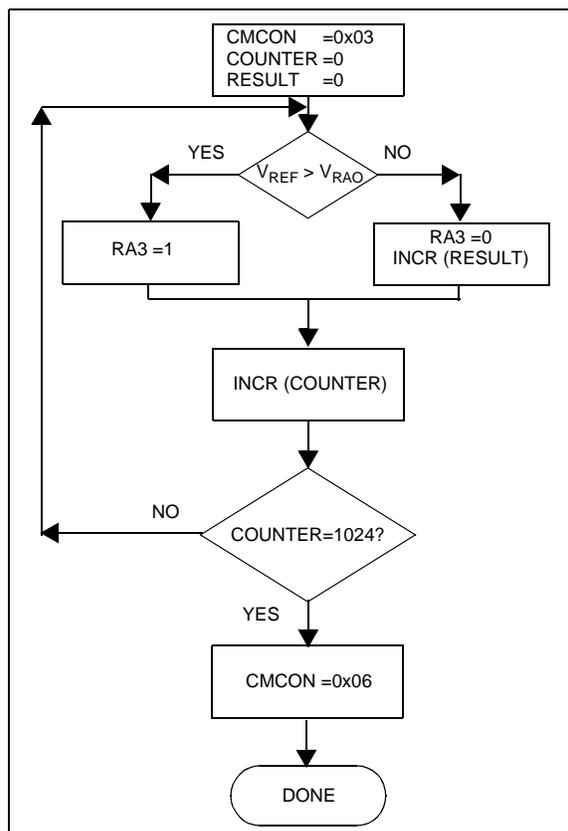

FIGURE 3: *This microcontroller A/D conversion flow chart is implemented with the circuit shown in Figure 2. Care should be taken to make the time that every cycle takes through the flow chart constant.*

After the timing counter goes to 1024 on one side of the Wheatstone bridge, the MCU switches the multiplexer (A2) to the leg of the other side of the sensor. With the voltage of the other leg of the sensor connected to the input of the amplifier, the controller cycles through another conversion for 1024 counts. The two results from these cycles are subtracted, giving the conversion results. This technique provides 10-bits of resolution with 9.9-bits of accuracy (rms).

The design equations for this circuit are:

$$V_{IN\ (CM)} = V_{REF3}$$

$$V_{IN\ (P\ to\ P)} = V_{RA3\ (P\ to\ P)}\ (R_1\ /\ R_2)$$

with $V_{IN\ (CM)}$ approximates V_{DD}/2 or is equal to $(LC_P + LC_N)$/2,

where:

V_{REF3} is the voltage reference applied to the comparator's non-inverting input and equal to approximately V_{SENSOR}/2. If made external, this reference voltage can be used to adjust offset errors

$V_{IN\ (P\ to\ P)}$ is equal to $(LC_{P(MAX)} - LC_{N(MIN)})$ or $(LC_{P(MIN)} - LC_{N(MAX)})$ which equals the sensor full scale range and $V_{RA3\ (P\ to\ P)}$ is equal to $V_{RA3\ (MAX)} - V_{RA3\ (MIN)}$ or approximately V_{DD}

The system in this application note has been designed to have a full-scale input range to the comparator of ± 40.5mV. Given 9.9-bit (rms) accuracy, the LSB size is 84.7μV.

The transfer function of the percentage of ones counted versus input voltage is shown in Figure 4. In this diagram, both the duty cycle between ones and zeros as well as the pulse width is modulated.
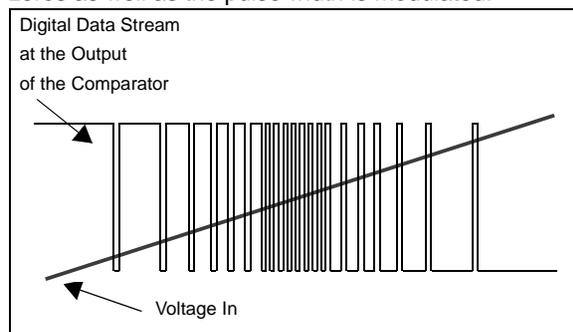

FIGURE 4: *The relationship between input voltage and the number of ones that are counted by the controller is shown conceptually with this diagram. At low input voltages, the output of the comparator produces very few zeros within the 1024 counts. At voltages in the center of the input range, the comparator quickly toggles between ones and zeros. At higher voltages, the comparator output produces mostly zeros and very few ones.*

ERROR SOURCES AND SYSTEM SOLUTIONS

A wheatstone bridge is designed to give a differential output rendering a small voltage that changes proportionally to the sensor's excitation, i.e. pressure or temperature, etc. The dominant types of errors that a sensor exhibits in its transfer function can be categorized as offset, gain, linearity, noise, and thermal. These sensors also produce other errors such as hysteresis, repeatability, stability and aging that are beyond the scope of this application note. An equal contributor to the overall system errors is the offset, gain, and linearity errors from the active components in the signal conditioning path.

OFFSET ERRORS

The offset error of a system can be mathematically described with a constant additive to the entire transfer function as shown in Figure 5.
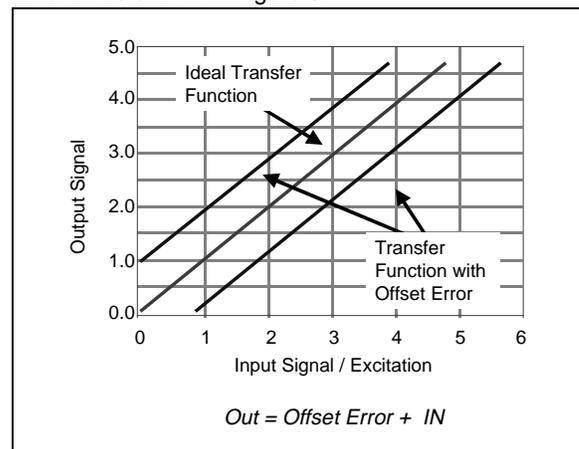

Out = Offset Error + IN

FIGURE 5: *The offset error of a system can be described graphically with a transfer function that has shifted along the x-axis.*

Typically, offset error is measured at a point where the input signal to the system is zero. This technique provides an output signal that is equal to the offset. This type of error can originate at the sensor or within the various components in the analog signal path. By definition, the offset error is repeatable and stable at a specified operating condition. If the operating conditions change, such as temperature, voltage excitation or current excitation, the offset error may also change.

The offset errors in this signal path come from the wheatstone bridge sensor, the operational amplifier (A1) offset, the port leakage current at RA0, the internal voltage reference (V_{REF3}) offset, the comparator offset, and the non-symmetrical output port of RA3. The only difference in the signal path of the two sensor outputs is the multiplexer channel, which interfaces directly with a high impedance CMOS operational amplifier. Otherwise, both sensor output signals are configured to travel down the same signal-conditioning path. Consequently, the conversion data taken from the positive leg

of the load cell sensor (LC_P) has the same offset and gain errors as the conversion data taken from the negative output of the load cell sensor (LP_N), with the exception of the bridge's offset error.

To accommodate these errors, the design equations for this circuit remains:

$$V_{IN\ (CM)} = V_{REF3}$$

$$V_{IN(P\ to\ P)} = V_{RA3\ (P\ to\ P)}\ (R_1 / R_2)$$

But, now the worst case variation of $V_{IN(P\ to\ P)}$ is equal to $(LC_{P(MAX)} - LC_{P(MIN)} + LC_{OFF} + A1_{OFF} + RA0_{OFF} + V_{REF3\text{-}OFF} + COMP_{OFF} + RA3_{OFF})$

where:

ΔLC_{OFF} is the maximum offset voltage that can be generated by the load cell bridge

$A1_{OFF}$ is the offset voltage of the operational amplifier

$RA0_{OFF}$ is the offset error caused by the leakage current of port RA0. This leakage current is specified at 1nA at room temperature and 0.5µA (max) over temperature. This leakage current causes a voltage drop across the parallel combination of R_1 and R_2

$V_{REF3\text{-}OFF}$ is the offset error of the internal voltage reference of the MCU or $V_{DD}/2$. This error can be reduced significantly with an external voltage reference

$COMP_{OFF}$ is the offset of the internal comparator of the MCU and

$RA3_{OFF}$ is caused by the inability of RA3 to go completely to the rails. It can be quantified by $RA3_{OFF} = ((V_{DD} - RA3_{HIGH}) - RA3_{LOW})/2$. This formula assumes $V_{REF3} = V_{DD} / 2$

The maximum magnitudes of these errors are summarized in Table 2.

Error Source	Offset Voltage over Temperature
Load Cell Bridge	±1.5mV in a 5V system
Op Amp	±2mV
Port Leakage, RA0	±1.3mV
Internal V_{REF}	±49mV
Comparator	±10mV
Output Port, RA3 (asymmetrical output swing)	5.5mV

TABLE 2: *Maximum offset errors over temperature for the circuit shown in Figure 3.*

Firmware Offset Calibration

The offset errors of the circuit can be calibrated in firmware. This is performed by subtracting the conversion code results of the positive leg of the sensor from the results of the negative leg of the sensor. The analog representation of the result of this calculation in firmware is:

$$V_{OUT} = LC_P + LC_{OFF} + A1_{OFF} + RA0_{OFF} + V_{REF3\text{-}OFF} + COMP_{OFF} + RA3_{OFF} - LC_N - A1_{OFF} - RA0_{OFF} - V_{REF3\text{-}OFF} - COMP_{OFF} - RA3_{OFF}$$

$$V_{OUT} = LC_P - LC_N + LC_{OFF}$$

This result illustrates the efficiency of using firmware to eliminate most of the offset errors, however, the trade-off for having offset adjustments performed by the MCU is dynamic range. In anticipation of these offset errors, the designer should increase the peak-to-peak analog input range of the conversion system. This will result in a conversion that has a wider dynamic range, consequently, lower accuracy.

To counteract this, the accuracy can be improved if more samples are taken in the conversion process. This technique will elongate the overall conversion time. Another technique that can be used is to perform a simple offset adjust in hardware which can be implemented with the digital potentiometer ($A3_A$).

Hardware Offset Calibration

Given the design equations for this circuit and the errors in Table 2, the total expected offset error over temperature for the electronics is ±69.3mV. With a sensor full-scale range of ±10mV, the dynamic range of the system would be ~7.9 times larger than the nominal, error free peak-to-peak range at the input of the comparator.

The 8-bit, 1kΩ digital potentiometer ($A3_A$) in Figure 2 is placed in series between the power supply (5V) with two 10kΩ, 1% resistors. This configuration provides a voltage reference range to the comparator of ±119mV centered around mid-supply (2.5V) with a resolution of 0.5mV. If an external reference is used with a ±0.5mV error range, the electronics will contribute ±20.8mV offset error over temperature. This changes the worst case full-scale peak-to-peak range of the system to ±30.8mV. This is only approximately three times larger than the nominal full-scale output (±10mV) of the sensor.

System Span (Gain) Errors

The span or gain of a system can be mathematically described as a constant, which is multiplied against the input signal. The magnitude of the span can easily be determined using the formula below:

Ideal Output = Input x Gain

Span error is the deviation of the span multiple from ideal and can be described with the formula below:

$$Actual\ Output = Input\ x\ Span\ (1 + Span\ Error)$$

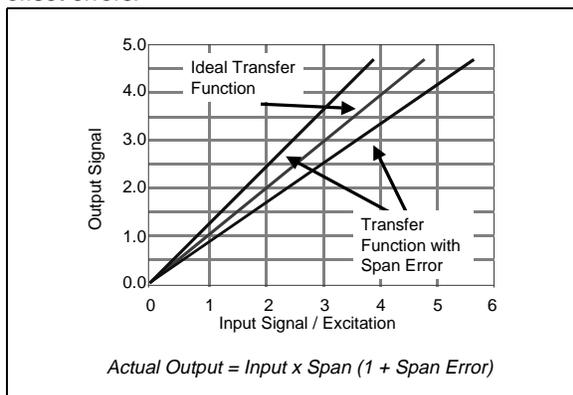Examples of transfer functions with span error are shown in Figure 6. The plots in Figure 6 do not have offset errors.

$$Actual\ Output = Input\ x\ Span\ (1 + Span\ Error)$$

FIGURE 6: *Span or gain errors can be described graphically as a transfer function that rotates around the intercept of the x and y-axis.*

Firmware Span (Gain) Calibration

For this circuit, the span error of the sensor is less influential than the offset errors on the system. Span errors come from the Load Cell ($\pm$20%), the resistors ($\pm$1%), capacitor ($\pm$10%), and the ON resistance of the RA3 port (0.2%). This circuit can rely on firmware calibration with a reduction in the dynamic range of the system. The combination of the sensor error and the capacitor error increases the requirements on the input range to the modulator configuration.

Hardware Span (Gain) Calibration

Span errors can most effectively be removed in the analog domain. For instance, the span error of the sensor can be adjusted with the sensor's excitation voltage. As a trade-off for this adjustment strategy, the common mode voltage of the sensor is changed, creating offset errors with respect to the reference voltage (V_{REF3}) of the comparator. This problem can be alleviated by making the voltage reference ratiometric to the sensor excitation source. Span errors can also be adjusted with either R_1 or R_2. In the circuit in Figure 2, the other half of the dual, 1kΩ digital potentiometer ($A3_B$) is configured to perform this function. This type of adjustment does not change the offset error of the system. Finally, span errors can be corrected with changes to the integration capacitor. Of all of the span adjustments, this one is the most awkward to implement.

SYSTEM LINEARITY ERRORS

Linearity error differs from offset or span errors in that it has a unique affect on each individual code of the digitizing system. Linearity errors are defined as the deviation of the transfer function from a straight line. Some engineers define this error using a line that stretches between the end points of the transfer curve while others define it using a line that is calculated using a "best fit" algorithm. In either case, the linearity errors can cause significant errors in translating the sensor input (pressure, temperature, etc.) to digital code.

Linearity errors come in many forms as shown in Figure 7. Sometimes the linearity error of a system can be characterized with a multi-order polynomial, but more typically this error is difficult to predict from system to system, in which case, firmware piecewise linearization methods are usually used.
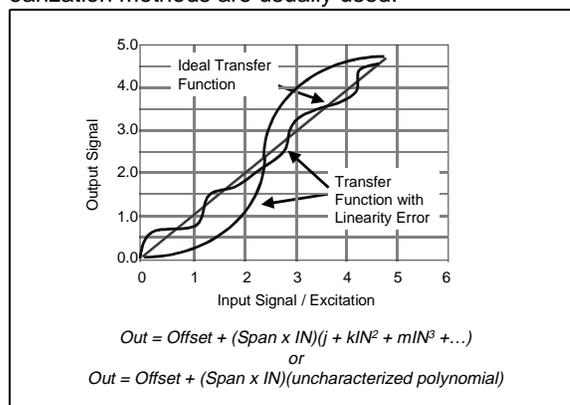

$$Out = Offset + (Span\ x\ IN)(j + kIN^2 + mIN^3 +...)$$
or
$$Out = Offset + (Span\ x\ IN)(uncharacterized\ polynomial)$$

FIGURE 7: *The linearity error of a sensor or system can sometimes be modeled and understood, which allows the designer to use predetermined algorithms in the MCU to minimize their affect. However, typically, these errors are not easily predicted and difficult to calibrate out of the signal path.*

Linearity errors in this system originate primarily in the sensor and secondarily in the remainder of the signal conditioning circuit.

Firmware Linearization

Linearity errors can be calibrated out of the system in firmware using polynomial calculations if the transfer function is understood or piecewise linearization methods if the transfer function from part to part varies. If piecewise linearization is used, calibration data should be taken from the system and stored in EEPROM. Utilizing the calibration data, piecewise linearization is easily implemented using two 16 bit unsigned subtractions, one 16 bit unsigned multiplication and one 16 bit unsigned divide.

$$X_{CAL} = X_{FULL} / (Y_{FULL} - Y_{OFF})\ x\ (Y_{SAMP} - Y_{ZERO})$$

where:

X_{CAL} is equal to the calibrated results

X_{FULL} is the ideal full scale response saved in EEPROM

Y_{FULL} is the measured full scale response saved in EEPROM

Y_{OFF} is the measured offset error saved in EEPROM

Y_{SAMP} is the measured sample that requires linearization and calibration

This style of linearization correction also removes offset and span errors from the digital results.

Hardware Linearization

There are two components that generate linearity errors. The sensor can contribute up to $\pm 0.25\%FS$ error. The capacitor in this circuit can also contribute an appreciable error if care is not taken in limiting the charge and discharge range of the device. If the R/C time constant of the circuit is greater than the inverse of the sample frequency, the non-linearity of this time response will cause a linearity error in the system.

In this case the R/C time constant is equal to:

$t_{RC} = R_1 || R_2 \times C_{INT}$

$t_{RC} = 2.67k\Omega || 165k\Omega \times 1\mu F$

$t_{RC} = 2.627msec$

also, $t_{RC} <= t_{SAMPLE} / 6.5$

The maximum voltage deviation due to the non-linearity of the R/C network is ~10mV. This is below a 0.2% error. If a lower sampling frequency is used, the integrating capacitor must be increased in value.

SYSTEM NOISE ERRORS

Noise can plague the best of circuits, particularly circuits that have large analog segments. An effective way to approach noise problems is to use a basic list of guidelines in conjunction with a working knowledge of noise fundamentals. The checklist that every designer should have on hand includes:

1. Are bypass capacitors included in the design?
2. Is a low impedance ground plane implemented to minimize any ground noise across sensitive analog parts?
3. Are appropriate anti-aliasing filters used in front of the A/D converter?
4. Are the devices in the circuit too noisy?

Firmware Noise Reduction

The A/D converter described in this application note was modeled after a classic first order delta-sigma topology. In the digital domain, the data collection algorithm implements a simple average engine by default. This style of averaging, otherwise known as digital filtering, is also called a single order sinc filter or Finite Impulse Response (FIR) filter.

Further noise reduction algorithms can be implemented with the PIC MCU which will produce a system with higher accuracy. As an example, a third order FIR filter can be implemented with the following calculations in code:

$y(n) = (2x(n) + x(n-1) + x(n-2) + x(n-3) + x(n-4) + x(n-5) + x(n-6)) / 8$

where:

n identifies the measurement sample

$y(n)$ is the output digital results

$x(n)$ is the measurement sample results

This filter is also known as a $sinc^3$ filter.

Other filter types, such as the Infinite Impulse Response (IIR) filter or a decimation filter can also be used to improve accuracy. A detailed discussion of these filters are beyond the scope of this application note, however, references have been provided for further reading.

Hardware Noise Reduction

In Figure 2, the R/C network that is used to implement the integrator function also serves as a low pass filter. This low pass filter is equal to:

$f_{3dB} = 1 / (2\pi R_1 || R_2 \times C_{INT})$

Further noise reduction can be implement by adding a second modulator stage at the input so this system. This implementation is shown in Figure 8.
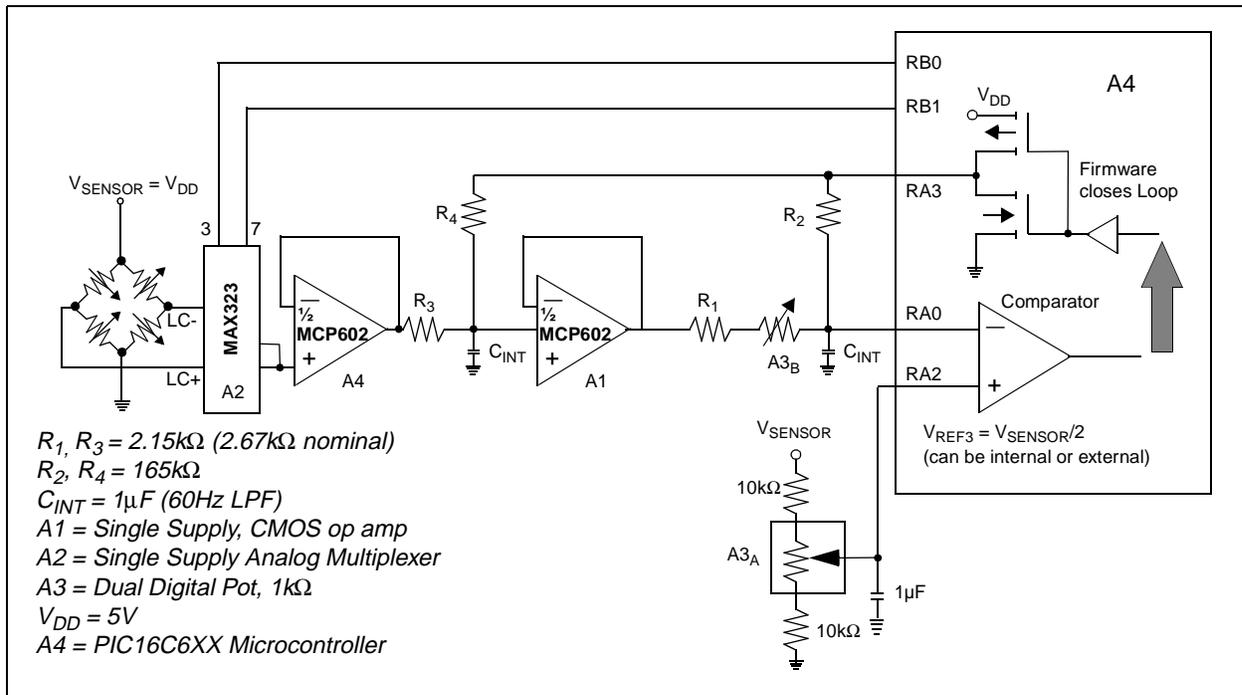
FIGURE 8: *An additional modulator stages can reduce noise in the system even further. In this circuit, one modulator stage is added which improves the system from a 9.9-bit accurate (rms) system to an 11.1-bit accurate system.*

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