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## USB7002/USB7006/USB7016/USB7052N FlexConnect Operation

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### 1.0 INTRODUCTION

The Microchip USB7002, USB7006, USB7016 and USB7052N smart hubs allow one of the downstream ports to be swapped with the upstream port to assume the role of the USB host during hub operation. This port exchange feature is called FlexConnect.

This feature can be used in two primary ways:

- **Host Swapping:** This functionality can be achieved through a hub, where a host and a device can agree to swap the host-device relationship. The host becomes a device, and the device becomes a host.
- **Host Sharing:** A USB ecosystem can be shared between multiple hosts. Note that only one host may access the USB tree at a time.

FlexConnect can be enabled through any of the following methods:

- **Register Control:** An embedded SMBus controller can configure and initiate the FlexConnect through SMBus commands during runtime.
- **USB Command:** A USB host can initiate FlexConnect via a special command to the hub's internal Hub Feature Controller (HFC).
- **Direct Pin Control:** A select number of available GPIO pins on the device can be assigned the role of a FlexConnect control pin.

### 1.1 Sections

This application note covers the following sections:

- [Section 2.0, Functional Overview](#)
- [Section 3.0, FlexConnect Register Control](#)
- [Section 4.0, FlexConnect USB Command Details](#)
- [Section 5.0, FlexConnect Pin Control](#)
- [Section 6.0, FlexConnect Configuration Space](#)
- [Section 7.0, Additional Hardware Considerations](#)

### 1.2 References

The following documents should be referenced when using this application note:

- *USB7002 Data Sheet* ([www.microchip.com/DS00002670](http://www.microchip.com/DS00002670))
- *USB7006 Data Sheet* ([www.microchip.com/DS00003715](http://www.microchip.com/DS00003715))
- *USB7016 Data Sheet* ([www.microchip.com/DS00003740](http://www.microchip.com/DS00003740))
- *USB7052N Data Sheet* ([www.microchip.com/DS00004505](http://www.microchip.com/DS00004505))
- *AN2810 - Configuration of USB7002/USB7006/USB7016/USB705x* ([www.microchip.com/DS00002810](http://www.microchip.com/DS00002810))

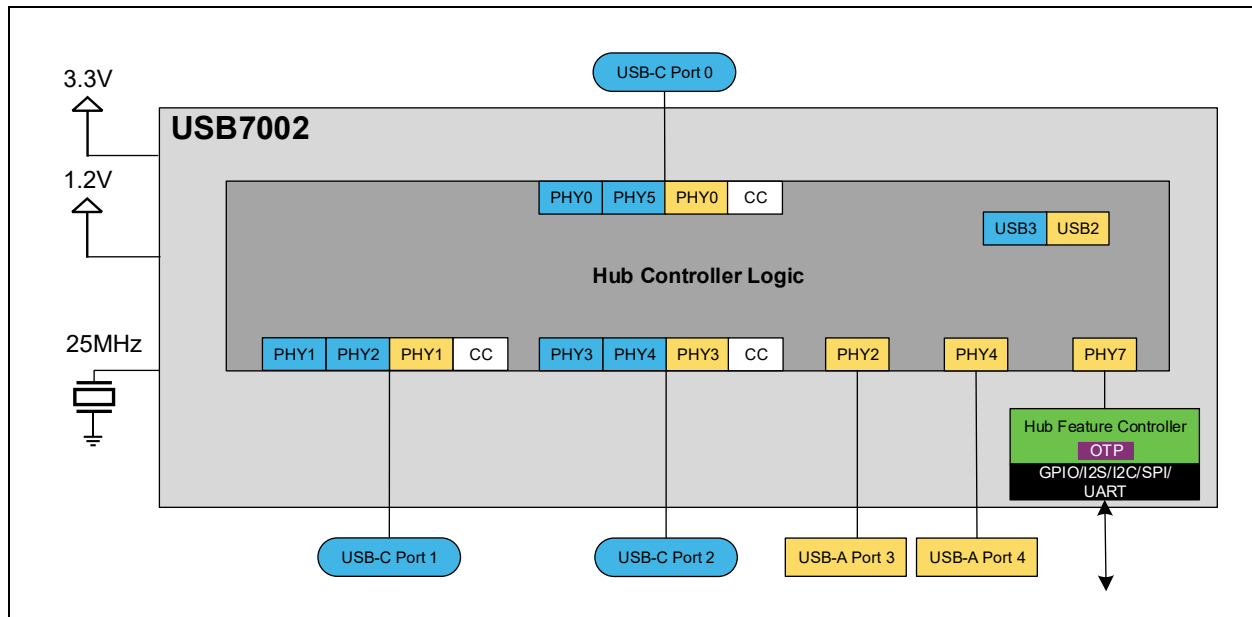
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## 2.0 FUNCTIONAL OVERVIEW

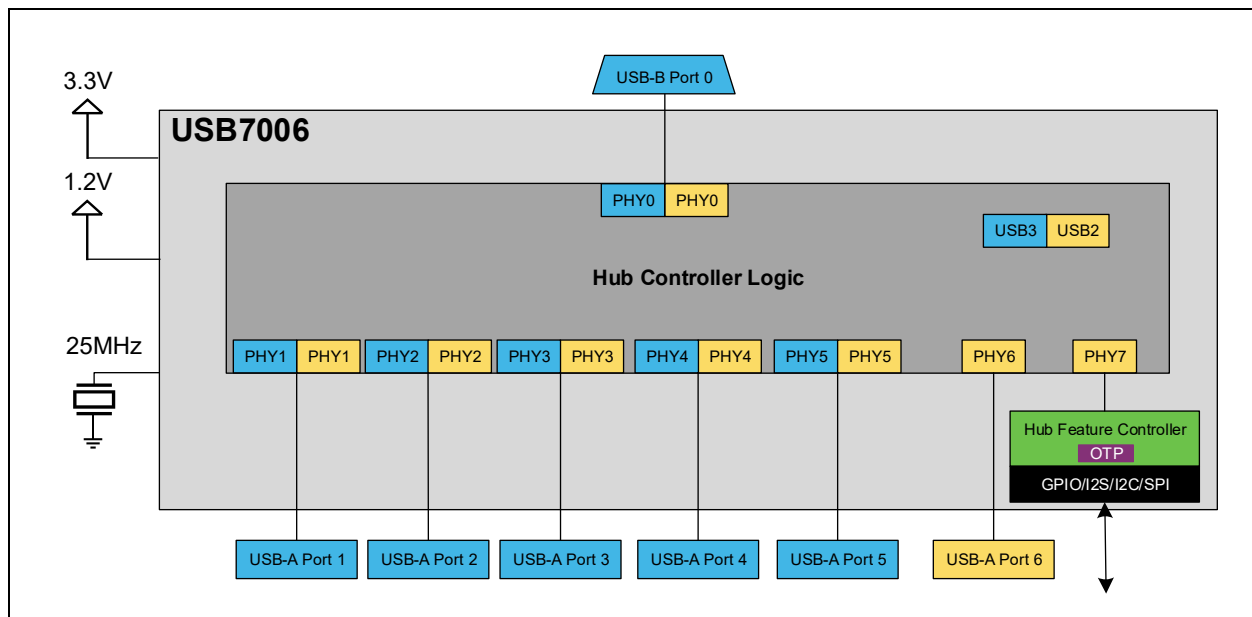
The USB7002/USB7006/USB7016/USB7052N has an internal USB device called a Hub Feature Controller (HFC), which can be used to initiate the FlexConnect feature. The HFC is a generic-class USB device. It is permanently connected to the last USB2 port of the hub as a non-removable device. Figure 1, Figure 2, Figure 3 and Figure 4 illustrate the internal block diagrams of the Microchip USB70xx family.

**Note:** When initiating FlexConnect using SMBus, the specified Flex port refers to the physical port number of USB2. This is different from the default logical port number shown in the following figures. FlexConnect via USB command or OTP-Configured Direct Pin Control continue to use the logical port number.

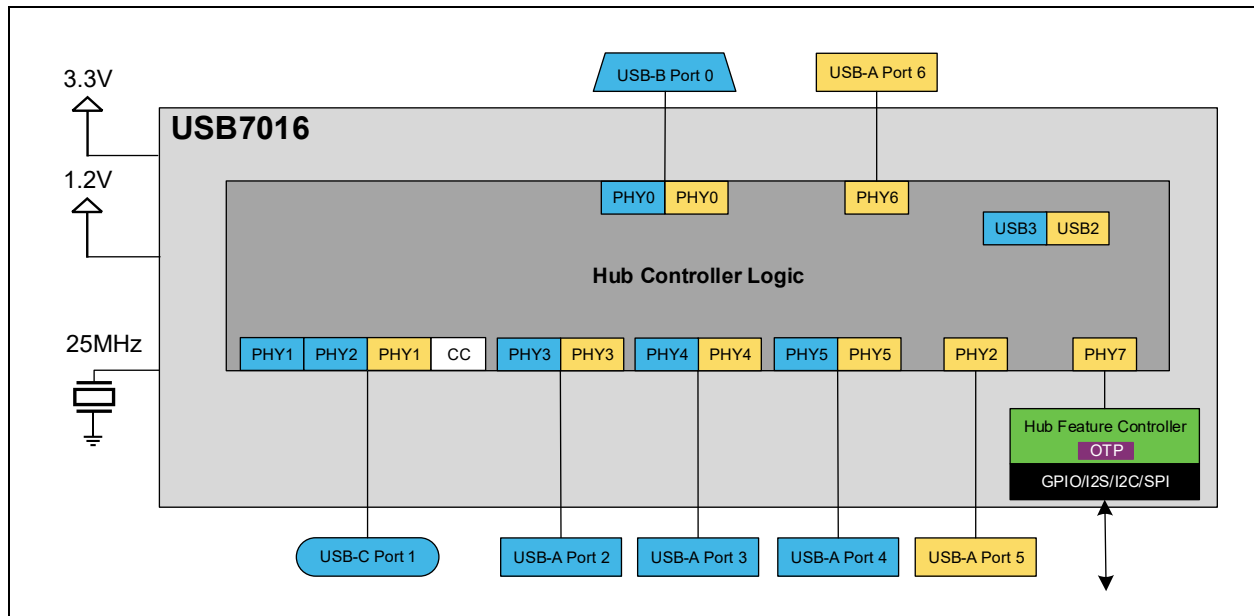
**FIGURE 1: USB7002 INTERNAL BLOCK DIAGRAM**



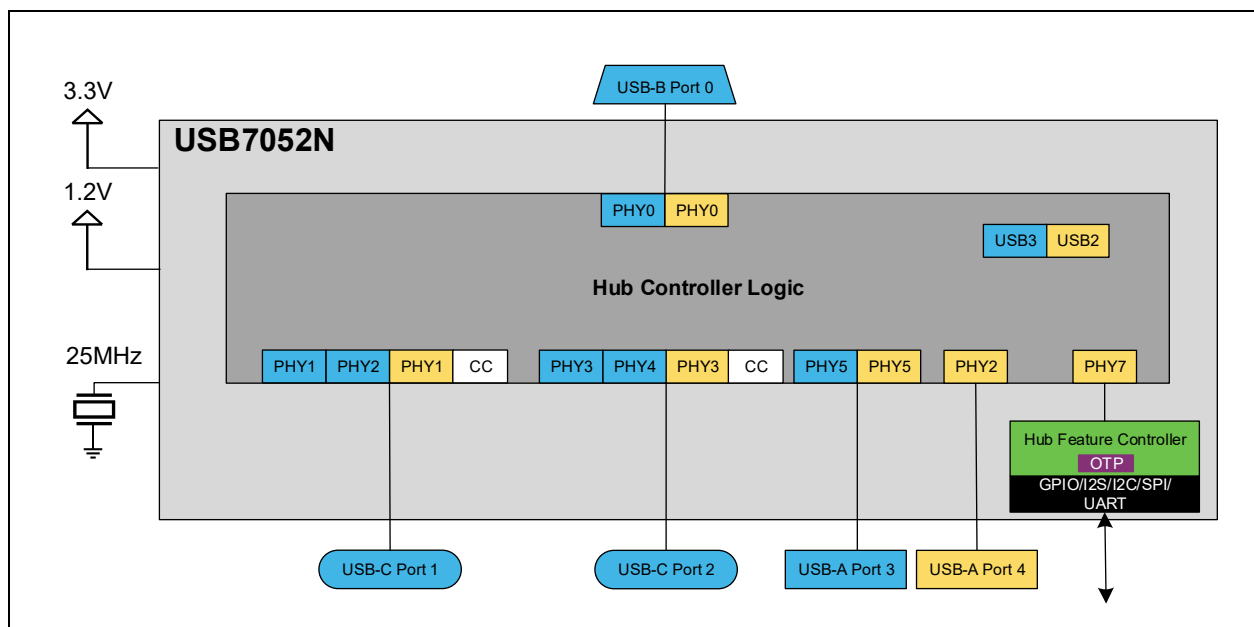
**FIGURE 2: USB7006 INTERNAL BLOCK DIAGRAM**



**FIGURE 3: USB7016 INTERNAL BLOCK DIAGRAM**



**FIGURE 4: USB7052N INTERNAL BLOCK DIAGRAM**



## 2.1 FlexConnect Initiation

The HFC provides the following methods to configure the hub controller to initiate FlexConnect:

- **Register Control** (via SMBus or OTP)
  - Refer to [Section 3.0, FlexConnect Register Control](#).
- **Vendor-Specific Command** SET\_ROLE\_SWITCH to the embedded HFC
  - Refer to [Section 4.0, FlexConnect USB Command Details](#).

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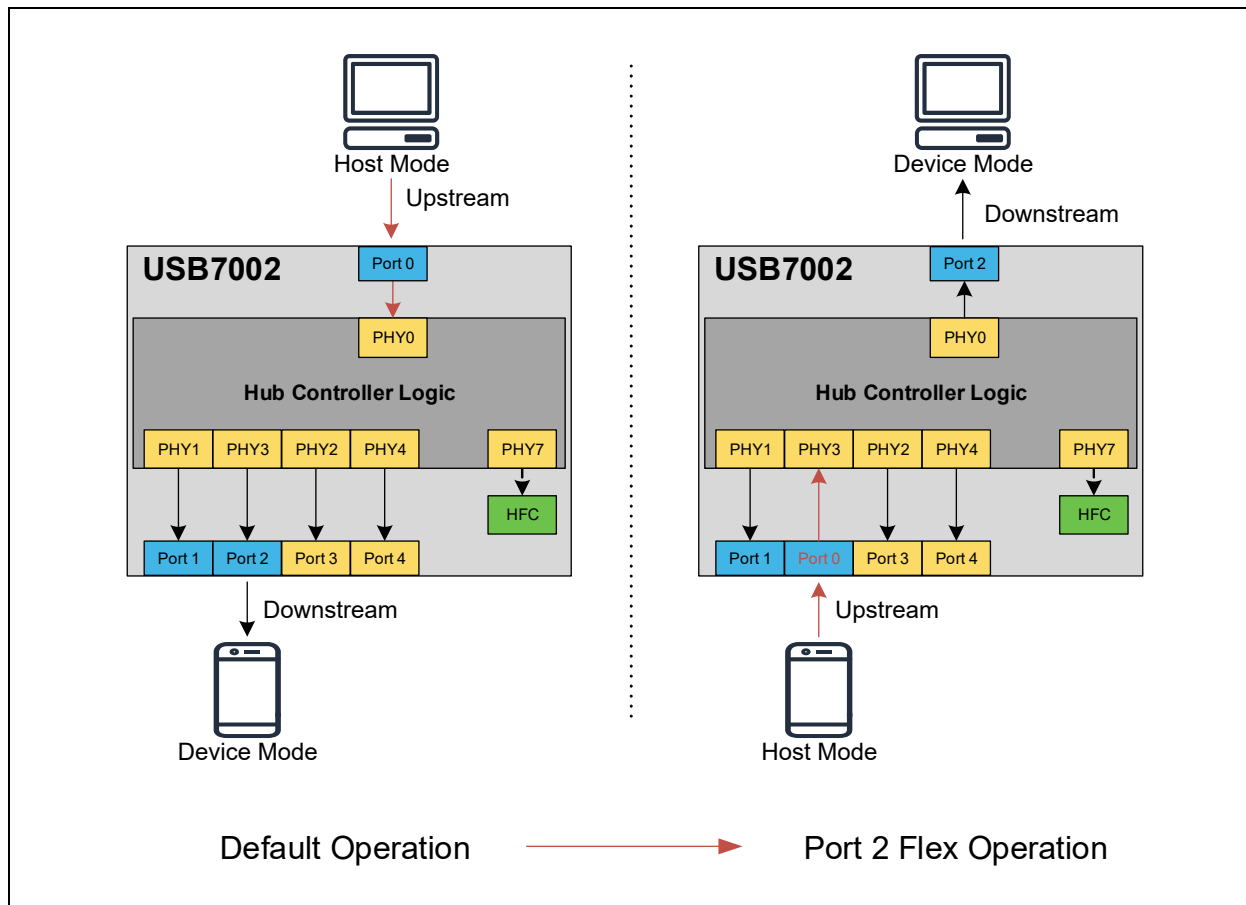
- **GPIO-Based Pin Control** after GPIO settings are programmed to hub OTP configuration memory
  - Refer to [Section 5.0, FlexConnect Pin Control](#).

When FlexConnect is initiated, the current upstream port changes to a downstream port, and the designated port changes into an upstream port. This can be used for Host-Swapping-type applications or Host-Sharing-type applications.

## 2.2 Host Swapping

In a host-swapping application, the role of the host is exchanged between two dual-role-capable devices through ID pin control, protocol handshake or some other proprietary method. An example is shown in [Figure 5](#).

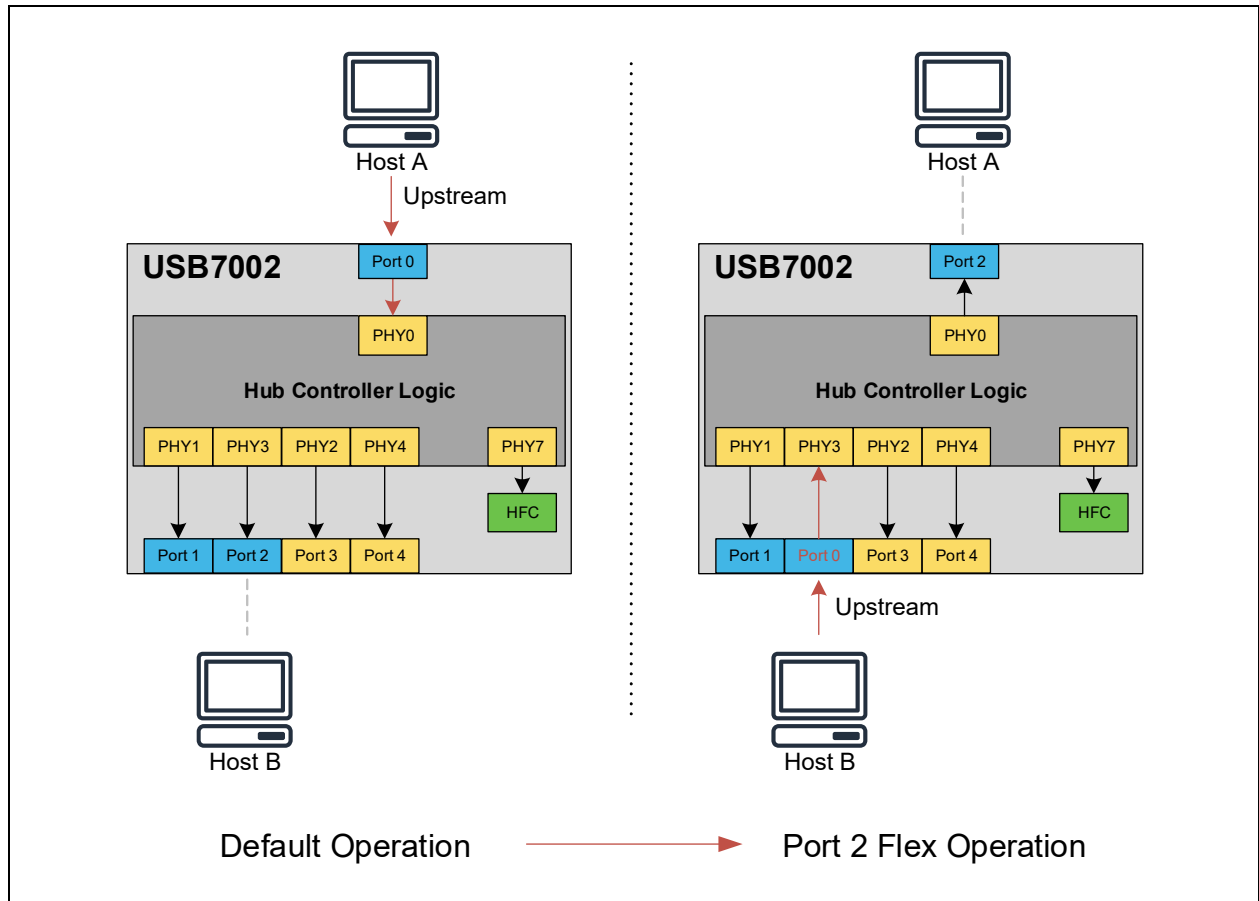
**FIGURE 5: FLEXCONNECT HOST SWAPPING EXAMPLE**



## 2.3 Host Sharing

In a host-sharing application, multiple hosts are connected to the hub. Only one of these hosts has access to the USB device tree at a time. All other hosts are effectively disconnected from the USB tree when they do not control the host port. An example of host sharing is shown in [Figure 6](#).

**FIGURE 6: FLEXCONNECT HOST SHARING EXAMPLE**



## 3.0 FLEXCONNECT REGISTER CONTROL

The FlexConnect registers can be configured via SMBus/I<sup>2</sup>C to initiate FlexConnect during runtime. For SMBus command format, refer to AN2810 - Configuration of USB7002/USB7006/USB7016/USB705x ([www.microchip.com/DS00002810](http://www.microchip.com/DS00002810)).

### 3.1 SMBus/I<sup>2</sup>C Target Pin Assignment

Based on the CFG\_STRAP configuration selected, the SMBus/I<sup>2</sup>C target pins are shown in Table 1. The firmware checks the presence of external 1 kΩ to 10 kΩ pull-up resistors on both pins during the SMBUS\_CHECK stage (see Note) and stays in the CFG\_SMBUS stage indefinitely for SMBus/I<sup>2</sup>C configuration. The external SMBus/I<sup>2</sup>C controller must write the SMBus command USB\_ATTACH (0xAA5500) or USB\_ATTACH\_WITH\_SMBUS (0xAA5600) to finish the configuration and exit the stage.

**Note:** For details on boot sequence, refer to the corresponding data sheet.

**TABLE 1: SMBUS/I<sup>2</sup>C TARGET PIN ASSIGNMENT**

CFG_STRAP	USB7002	USB7006	USB7016	USB7052N
	Configuration 1 (SMBus/I <sup>2</sup> C)	Configuration 3	Configuration 1 (SMBus/I <sup>2</sup> C)	Configuration 1 (SMBus/I <sup>2</sup> C)
I <sup>2</sup> C Clock	PF26			PF26
I <sup>2</sup> C Data	PF27			PF19

### 3.2 Initiating FlexConnect via SMBus/I<sup>2</sup>C Command

To initiate FlexConnect via SMBus, modify the registers defined in the following to flex USB2 and USB3 PHYSICAL ports. While flexing a USB-Type C<sup>®</sup> downstream port, the corresponding CC control logic to the port must be configured as upstream device role accordingly. The device role can be assigned through DEVICE\_ROLE bit in the CC\_HW\_CTL\_x register (see Table 5 and Table 6).

**TABLE 2: USB2 SYSTEM CONFIGURATION REGISTER**

USB2_SYS_CONFIG (BF80_0808h) RESET = 00h			USB2 System Configuration Register
Bit	Name	R/W	Description
7:3	Masked	R	For internal use only. Do not modify the value.
2:0	USB2_HUB_FLEX	R/W	PHYSICAL downstream port to initiate FlexConnect. For the numbering of physical ports, refer to Figure 1 to Figure 4, respectively.  001b = Port 1 010b = Port 2 011b = Port 3 100b = Port 4 101b = Port 5 110b = Port 6 All others = <i>Invalid</i>

TABLE 3: USB3 SYSTEM CONFIGURATION REGISTER

USB3_SYS_CONFIG (BF80_0828h) RESET = 00h			USB3 System Configuration Register
Bit	Name	R/W	Description
7:3	Masked	R	For internal use only. Do not modify the value.
2:0	USB3_HUB_FLEX	R/W	PHYSICAL downstream port to initiate FlexConnect. For the numbering of physical ports, refer to <a href="#">Figure 1</a> to <a href="#">Figure 4</a> , respectively.  001b = Port 1 010b = Port 2 011b = Port 3 100b = Port 4 101b = Port 5 All others = <i>Invalid</i>

TABLE 4: PORT 0 CC HARDWARE CONTROL REGISTER

CC_HW_CTL_0 (BF80_5000h) RESET = 01h			Port 0 CC Hardware Control Register (USB7002 Only)
Bit	Name	R/W	Description
7:3	Reserved	R	Always read as '0.'
2	DEVICE_ROLE	R/W	Device role 0b = Device is configured as Upstream Facing Port (UFP). 1b = Device is configured as Downstream Facing Port (DFP).
1	Reserved	R	Always read as '0.'
0	Masked	R	Always read as '1.' Do not modify the value.

TABLE 5: PORT 1 CC HARDWARE CONTROL REGISTER

CC_HW_CTL_1 (BF80_5400h) RESET = 05h			Port 1 CC Hardware Control Register (USB7002/USB7016/USB7052N)
Bit	Name	R/W	Description
7:3	Reserved	R	Always read as '0.'
2	DEVICE_ROLE	R/W	Device role 0b = Device is configured as UFP. 1b = Device is configured as DFP.
1	Reserved	R	Always read as '0.'
0	Masked	R	Always read as '1.' Do not modify the value.

**TABLE 6: PORT 2 CC HARDWARE CONTROL REGISTER**

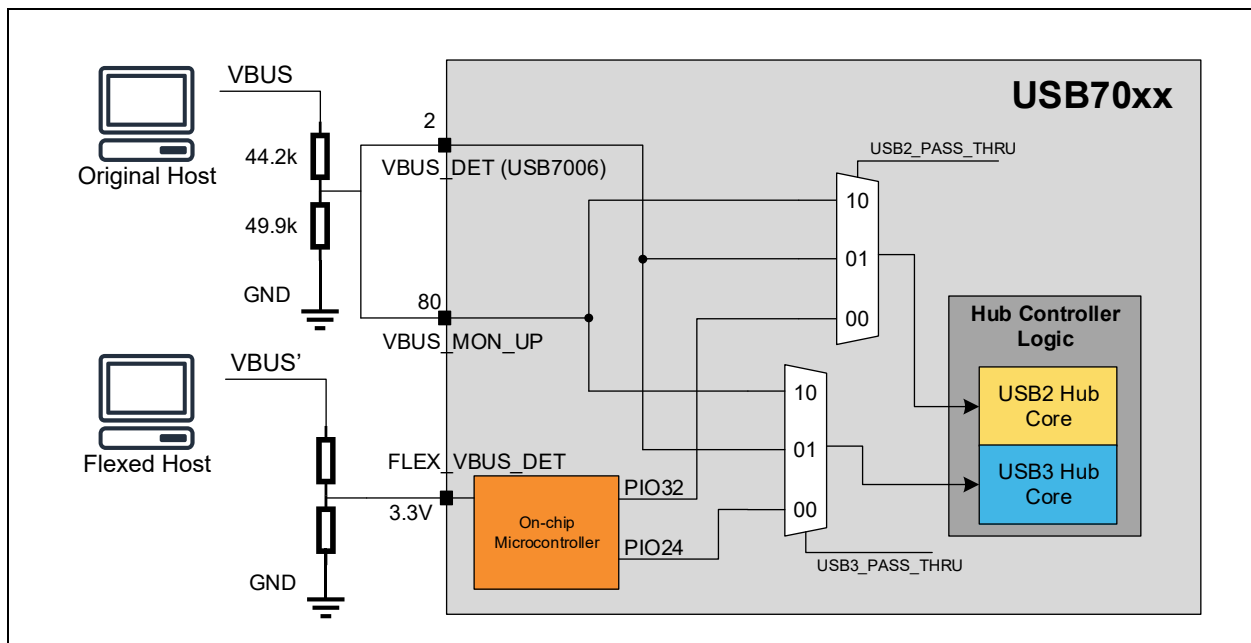
CC_HW_CTL_2 (BF80_5800h) RESET = 05h			Port 2 CC Hardware Control Register (USB7002/USB7052N)
Bit	Name	R/W	Description
7:3	Reserved	R	Always read as '0.'
2	DEVICE_ROLE	R/W	Device role 0b = Device is configured as UFP. 1b = Device is configured as DFP.
1	Reserved	R	Always read as '0.'
0	Masked	R	Always read as '1.' Do not modify the value.

### 3.3 VBUS Status Detection

The implementation of FlexConnect requires that the system designer be responsible for routing the correct host VBUS signal to the USB70xx VBUS\_DET or VBUS\_MON\_UP pins. (See [Figure 7](#).) The selection of the VBUS input signal for the USB2 and USB3 hub cores can be done using the VBUS\_PASS\_THRU register. By default, the USB7006 uses the VBUS\_DET device pin as the input signal, while the USB7002, USB7016 and USB7052N use VBUS\_MON\_UP. Alternatively, the internal controller can provide the signal to the USB3 and USB2 hub cores through PIO24 and PIO32.

In addition to the original VBUS\_DET or VBUS\_MON\_UP pins, the system designer can also select a PFX pin in the list through the FLEX\_VBUSDET register as a new VBUS detection pin. For more details, please refer to [Section 7.1.4, Assigning a Specific FLEX\\_VBUS\\_DET Pin](#).

**FIGURE 7: VBUS STATE DETECTION ON UPSTREAM PORT**



**TABLE 7: VBUS PASS THROUGH REGISTER**

VBUS_PASS_THRU (BF80_3C40h) RESET = 05h (USB7006) RESET = 0Ah (USB7002/USB7016/ USB7052N)			VBUS Pass Through Register
Bit	Name	R/W	Description
7:4	Masked	R	For internal use only. Do not modify the value.
3:2	USB3_PASS_THRU	R/W	00 = The VBUS to USB3 hub comes from Internal PIO24. 01 = The VBUS to USB3 hub comes from device pin (PF30). 10 = The VBUS to USB3 hub comes from VBUS_MON_UP (not available on USB7006). 11 = Reserved
1:0	USB2_PASS_THRU	R/W	00 = The VBUS to USB2 hub comes from Internal PIO32. 01 = The VBUS to USB2 hub comes from device pin (PF30). 10 = The VBUS to USB2 hub comes from VBUS_MON_UP (not available on USB7006). 11 = Reserved

**TABLE 8: PIO[31:0] OUTPUT ENABLE REGISTER**

PIO32_OUT_EN (BF80_0900h) RESET = 00000000h			PIO Output Enable Register
Bit	Name	R/W	Description
31:0	PIO[31:0]	R/W	Output: 0 = Disabled, 1 = Enabled

**TABLE 9: PIO[63:32] OUTPUT ENABLE REGISTER**

PIO64_OUT_EN (BF80_0904h) RESET = 00000000h			PIO Output Enable Register
Bit	Name	R/W	Description
31:0	PIO[63:32]	R/W	Output: 0 = Disabled, 1 = Enabled

**TABLE 10: PIO[31:0] OUTPUT DATA REGISTER**

PIO32_OUT (BF80_0920h) RESET = 00000000h			PIO Data Output Register
Bit	Name	R/W	Description
31:0	PIO[31:0]	R/W	Output Buffer Data

**TABLE 11: PIO[63:32] OUTPUT DATA REGISTER**

PIO64_OUT (BF80_0924h) RESET = 00000000h			PIO Data Output Register
Bit	Name	R/W	Description
31:0	PIO[63:32]	R/W	Output Buffer Data

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## EXAMPLE 1: FLEXCONNECT VIA SMBUS/I<sup>2</sup>C COMMAND

An example of FlexConnect port 3 on USB7002 through SMBus/I<sup>2</sup>C controller is shown below:

1. Write 0x02 to **0xBF80\_0808** to flex USB2 port 3. (See [Note 1](#).)  
0x00 0x00 0x07 0x00 0x01 **0xBF 0x80 0x08 0x08** 0x02  
0x99 0x37 0x00
2. Write 0x05 to **0xBF80\_5000** to configure port 0 as DFP.  
0x00 0x00 0x07 0x00 0x01 **0xBF 0x80 0x50 0x00** 0x05  
0x99 0x37 0x00
3. Send Attach command. (See [Note 2](#).)  
0xAA 0x56 0x00
4. Write 0x00 to **0xBF80\_3C40** to specify VBUS signal is from internal PIO24 and PIO32.  
0x00 0x00 0x07 0x00 0x01 **0xBF 0x80 0x3C 0x40** 0x00  
0x99 0x37 0x00
5. Configure **0xBF80\_0903** and **0xBF80\_0904** to set the direction of PIO24 and PIO32 as output.  
0x00 0x00 0x08 0x00 0x02 **0xBF 0x80 0x09 0x03** 0x01 0x01  
0x99 0x37 0x00
6. Configure **0xBF80\_0923** and **0xBF80\_0924** to set the PIO24 and PIO32 as output high.  
0x00 0x00 0x08 0x00 0x02 **0xBF 0x80 0x09 0x23** 0x01 0x01  
0x99 0x37 0x00

**Note 1:** On USB7002, physical port 2 is configured as logical port 3.

**2:** The configuration for VBUS\_PASS\_THRU and PIO registers need to be done after the Attach command.

**3:** On USB7002, physical port 3 is configured as logical port 2.

## 3.4 FlexConnect on Type C Downstream Port

While flexing a USB-Type C<sup>®</sup> downstream port, the corresponding CC control logic to the port must be configured as upstream device role. The device role can be assigned through CC\_HW\_CTL\_x register.

## EXAMPLE 2: SMBUS/I<sup>2</sup>C COMMAND FOR FLEXING TYPE C PORT 1 ON USB7002

The following example shows a sequence of the SMBus command for flexing Type C port 1 on USB7002:

1. Write 0x01 to **0xBF80\_0808** to flex USB2 port 1.  
0x00 0x00 0x07 0x00 0x01 **0xBF 0x80 0x08 0x08** 0x01  
0x99 0x37 0x00
2. Write 0x01 to **0xBF80\_0828** to flex USB3 port 1.  
0x00 0x00 0x07 0x00 0x01 **0xBF 0x80 0x08 0x28** 0x01  
0x99 0x37 0x00
3. Write 0x05 to **0xBF80\_5000** to configure port 0 as DFP.  
0x00 0x00 0x07 0x00 0x01 **0xBF 0x80 0x50 0x00** 0x05  
0x99 0x37 0x00
4. Write 0x01 to **0xBF80\_5400** to change the device role for port 1 CC Logic.  
0x00 0x00 0x07 0x00 0x01 **0xBF 0x80 0x54 0x00** 0x01  
0x99 0x37 0x00
5. Send Attach command. (See [Note 2](#).)  
0xAA 0x56 0x00

6. Write 0x00 to **0xBF80\_3C40** to specify VBUS signal is from internal PIO24 and PIO32.  
0x00 0x00 0x07 0x00 0x01 **0xBF 0x80 0x3C 0x40** 0x00  
0x99 0x37 0x00
7. Configure **0xBF80\_0903** and **0xBF80\_0904** to set the direction of PIO24 and PIO32 as output.  
0x00 0x00 0x08 0x00 0x02 **0xBF 0x80 0x09 0x03** 0x01 0x01  
0x99 0x37 0x00
8. Configure **0xBF80\_0923** and **0xBF80\_0924** to set the PIO24 and PIO32 as output high.  
0x00 0x00 0x08 0x00 0x02 **0xBF 0x80 0x09 0x23** 0x01 0x01  
0x99 0x37 0x00

### EXAMPLE 3: SMBUS/I<sup>2</sup>C COMMAND FOR FLEXING TYPE C PORT 2 ON USB7002

The following example shows a sequence of the SMBus command for flexing Type C port 2 on USB7002:

1. Write 0x03 to **0xBF80\_0808** to flex USB2 port 2. (See [Note 3](#).)  
0x00 0x00 0x07 0x00 0x01 **0xBF 0x80 0x08 0x08** 0x03  
0x99 0x37 0x00
2. Write 0x03 to **0xBF80\_0828** to flex USB3 port 2. (See [Note 3](#).)  
0x00 0x00 0x07 0x00 0x01 **0xBF 0x80 0x08 0x28** 0x03  
0x99 0x37 0x00
3. Write 0x05 to **0xBF80\_5000** to configure port 0 as DFP.  
0x00 0x00 0x07 0x00 0x01 **0xBF 0x80 0x50 0x00** 0x05  
0x99 0x37 0x00
4. Write 0x01 to **0xBF80\_5800** to change the device role for port 2 CC Logic.  
0x00 0x00 0x07 0x00 0x01 **0xBF 0x80 0x58 0x00** 0x01  
0x99 0x37 0x00
5. Send Attach command. (See [Note 2](#).)  
0xAA 0x56 0x00
6. Write 0x00 to **0xBF80\_3C40** to specify VBUS signal is from internal PIO24 and PIO32.  
0x00 0x00 0x07 0x00 0x01 **0xBF 0x80 0x3C 0x40** 0x00  
0x99 0x37 0x00
7. Configure **0xBF80\_0903** and **0xBF80\_0904** to set the direction of PIO24 and PIO32 as output.  
0x00 0x00 0x08 0x00 0x02 **0xBF 0x80 0x09 0x03** 0x01 0x01  
0x99 0x37 0x00
8. Configure **0xBF80\_0923** and **0xBF80\_0924** to set the PIO24 and PIO32 as output high.  
0x00 0x00 0x08 0x00 0x02 **0xBF 0x80 0x09 0x23** 0x01 0x01  
0x99 0x37 0x00

## 4.0 FLEXCONNECT USB COMMAND DETAILS

A special USB command SET\_ROLE\_SWITCH can be issued by the USB host to the internal HFC to initiate FlexConnect. After FlexConnect is initiated, the hub automatically reverts to the default port 0 host state if one of the following conditions is met:

- If the new flex host sends a USB command, which commands the hub to return to the default state
- If the new flex host is disconnected any time after the flex host has enumerated the hub
- If the hub has not yet been enumerated by the flex host after the ENUM\_TIMEOUT expires
- If the VBUS\_DET signal on either the default host port or the new flex host port goes low

The USB command is a control transfer with NO DATA, sent to Endpoint 0 of the internal HFC. This controller is located on USB2 port 7. The SETUP command format is shown in [Table 12](#).

**TABLE 12: FLEXCONNECT SETUP PACKET**

Setup Parameter	Value	Description
bmRequestType	0x41	Host-to-device, vendor-class, targeted to interface
bRequest	0x90	SET_ROLE_SWITCH
wValue	0xYYYY	Refer to <a href="#">Table 13</a>
wIndex	0x0000	Reserved
wLength	00	No data

**TABLE 13: WVALUE DETAIL OF FLEXCONNECT COMMAND SETUP PACKET**

Bit	Name	Description
15:12	FLEX_USB3_PORT	LOGICAL downstream port to initiate or terminate FlexConnect  0001b = Port 1 0010b = Port 2 0011b = Port 3 0100b = Port 4 0101b = Port 5 All others = <b>Invalid</b>
11	FLEX_USB3_ON	1b = Flex the USB3 portion of hub. 0b = Unflex the USB3 portion of hub or no change if the hub is already unflexed.
10:8	ENUM_TIMEOUT	These bits control a timer, which is started after FlexConnect is initiated. The hub will revert to the unflexed state after timeout if the flex host does not enumerate the hub.  000b = No timeout defined (hub waits for enumeration indefinitely) 001b = 10 ms 010b = 100 ms 011b = 500 ms 100b = 1s 101b = 5s 110b = 10s 111b = 20s
7:6	Reserved	Always '0'
5	FLEX_CONNECT	Always 1 for selection of FlexConnect mode
4	FLEX_USB2_ON	1b = Flex the USB2 portion of hub. 0b = Unflex the USB2 portion of hub or no change if the hub is already unflexed.

**TABLE 13: WVALUE DETAIL OF FLEXCONNECT COMMAND SETUP PACKET (CONTINUED)**

Bit	Name	Description
3:0	FLEX_USB2_PORT	LOGICAL downstream port to initiate or terminate FlexConnect  0001b = Port 1 0010b = Port 2 0011b = Port 3 0100b = Port 4 0101b = Port 5 0110b = Port 6 All others = <i>Invalid</i>

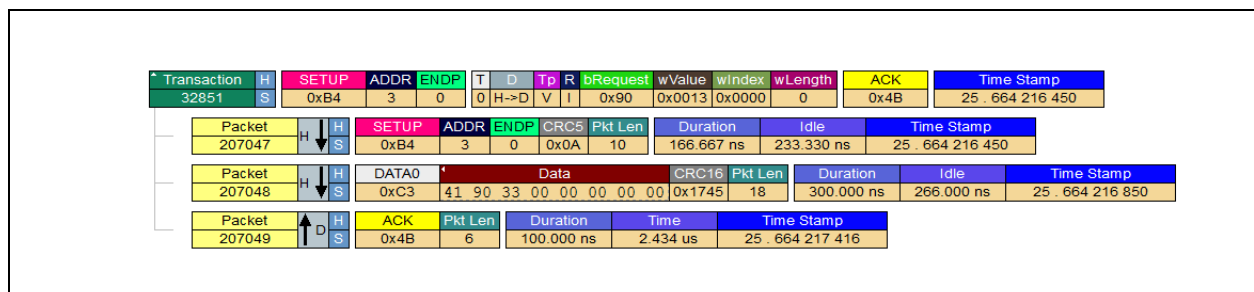
## 4.1 FlexConnect USB Command Example

An example of a FlexConnect initialization command for USB2 hub to Port 3 is shown in [Table 14](#). This command is sent to Endpoint 0 of the HFC.

**TABLE 14: FLEXCONNECT SETUP COMMAND EXAMPLE**

Setup Parameter	Value	Note
bmRequestType	0x41	Host-to-device, vendor-class, targeted to interface
bRequest	0x90	SET_ROLE_SWITCH
wValue	0x0033	Bits 15:12 = 0000b (No flexing of the USB3 portion of hub) Bit 11 = 0b (No flexing of the USB3 portion of hub) Bits 10:8 = 000b (No enumeration timeout) Bits 7:6 = 00b (Reserved and always 0) Bit 5 = 1b (Enter FlexConnect mode) Bit 4 = 1b (Flex of the USB2 portion of hub) Bits 3:0 = 0011b (LOGICAL Port 3)
wIndex	0x0000	Reserved
wLength	00	No data

**FIGURE 8: REGISTER READ SETUP TRANSACTION EXAMPLE**



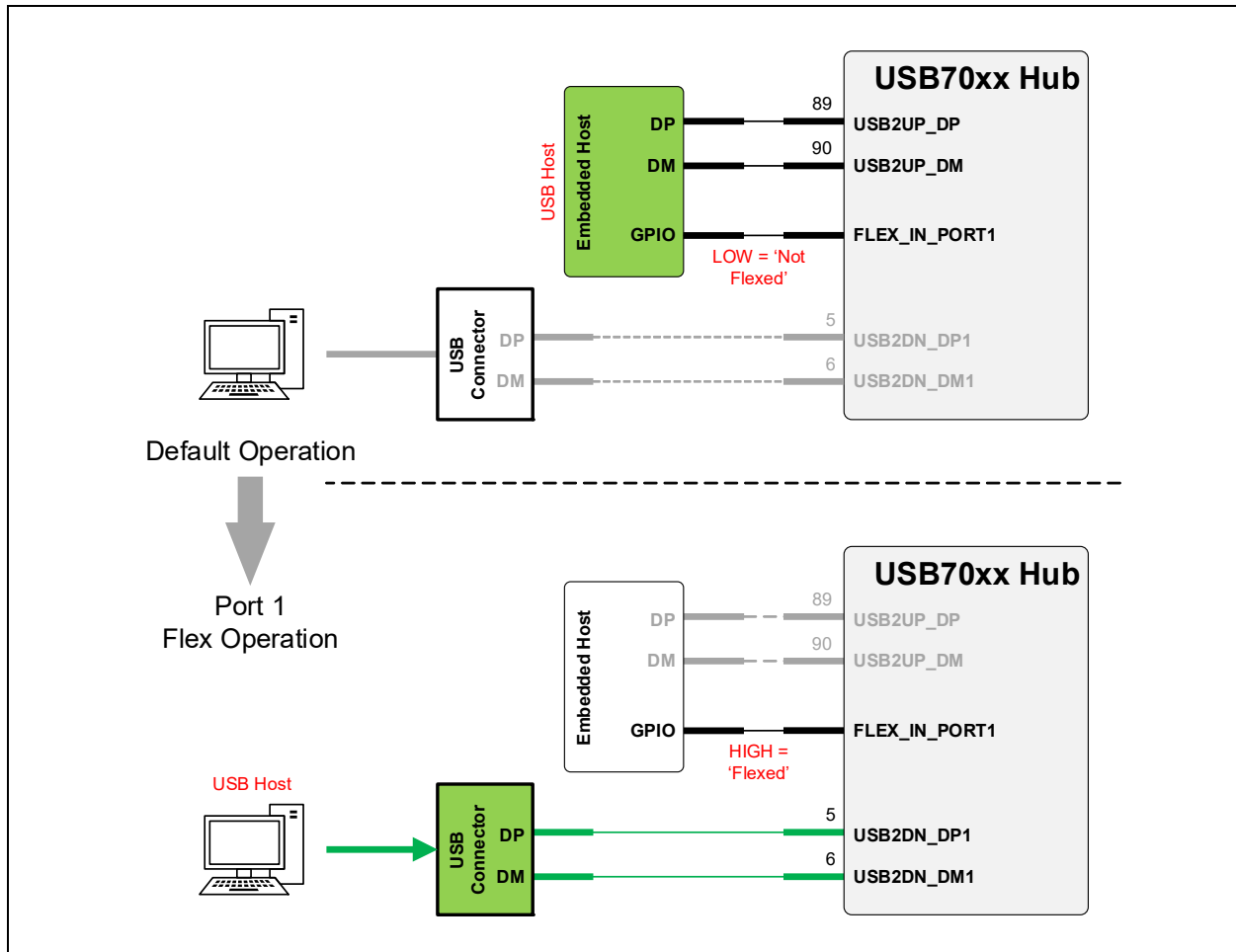
## 5.0 FLEXCONNECT PIN CONTROL

The FlexConnect can also be initiated through pin control by an embedded host. A selected number of available programmable function pins PFx may be assigned the role of FLEX\_IN\_PORTx.

If using the direct pin control method, each port that utilizes the FlexConnect feature must also be assigned its own FLEX\_IN\_PORTx signal. If multiple FLEX\_IN\_PORTx signals are triggered, the first triggered pin associated with its port will be flexed to an upstream port.

An example of how an embedded USB host may use the direct pin control method is shown in [Figure 9](#).

**FIGURE 9: FLEXCONNECT PIN CONTROL EXAMPLE**



By default, FLEX\_IN\_PORT[1:6] pins are not assigned, and hence, not active. Only ports that are to be controlled via direct pin control must have a PF/GPIO pin assigned. Note that the assigned pins must be multiplexed to GPIO function.

Once one or more FLEX\_IN\_PORT[1:6] pins have been assigned, the pins will behave as shown in [Table 15](#). Note that only one FLEX\_IN\_PORT[1:6] should be asserted at once.

**TABLE 15: FLEXCONNECT STATE TRUTH TABLE EXAMPLE**

FLEX_IN_PORT6	FLEX_IN_PORT5	FLEX_IN_PORT4	FLEX_IN_PORT3	FLEX_IN_PORT2	FLEX_IN_PORT1	FlexConnect State
0	0	0	0	0	0	Port 0 = Host Port
0	0	0	0	0	1	Port 1 = Host Port
0	0	0	0	1	0	Port 2 = Host Port
0	0	0	1	0	0	Port 3 = Host Port

**TABLE 15: FLEXCONNECT STATE TRUTH TABLE EXAMPLE (CONTINUED)**

FLEX_IN_PORT6	FLEX_IN_PORT5	FLEX_IN_PORT4	FLEX_IN_PORT3	FLEX_IN_PORT2	FLEX_IN_PORT1	FlexConnect State
0	0	1	0	0	0	Port 4 = Host Port
0	1	0	0	0	0	Port 5 = Host Port
1	0	0	0	0	0	Port 6 = Host Port
All Others						<b>INVALID STATE</b>

**Note:** The USB command method has specific conditions where the hub automatically unflexes and returns to the default Port 0 Host state. When using the direct pin control method, the hub always follows the state of the pins and never attempts to automatically unflex.

It is particularly important to understand that these control signals operated based on the hub's Logical Port assignments or how the ports are numbered as the USB host identifies the ports numbered. These control I/Os are not linked to the physical port numbering, which changes from one hub part number to another (since PHYs are grouped and remapped in various ways to form different combinations of Type-C and Type-A ports on the UFP and DFPs).

The pin assignment registers are detailed in [Table 16](#) to [Table 29](#). These can be modified through the hub's internal OTP memory or through the SMBus interface during hub startup configuration. These pins cannot be modified through run-time register writes.

**TABLE 16: LOGICAL PORT 1 FLEXCONNECT TRIGGER PIO CONFIGURATION REGISTER**

FLEX_IN_PORT1 (BFD2_3442h)			FlexConnect Trigger PIO Configuration Register
Bit	Name	R/W	Description
7	USB2_FLEX_IN_EN	R/W	This bit is used for USB2.0 hub.  1b = Enables FlexConnect trigger for the USB2.0 portion of Port 1 through GPIO control. The specific GPIO pin is selected in bits [2:0] of this register. The FlexConnect state is entered upon the rising edge of the selected GPIO. The FlexConnect state is exited upon the falling edge of the selected GPIO. 0b = Disables FlexConnect pin trigger for the USB2.0 portion of Port 1. All other bits in this register are ignored.
6:4	Reserved	R	Reserved
3	USB3_FLEX_IN_EN	R/W	This bit is used for USB3.2 hub.  1b = Enables FlexConnect trigger for the USB3.2 portion of Port 1 through GPIO control. The specific GPIO pin is selected in bits [2:0] of this register. The FlexConnect state is entered upon the rising edge of the selected GPIO. The FlexConnect state is exited upon the falling edge of the selected GPIO. 0b = Disables FlexConnect pin trigger for the USB3.2 portion of Port 2. All other bits in this register are ignored.
2:0	FLEX_IN_IO	R/W	This bit selects the GPIO to be used for the Logical Port 2 FlexConnect trigger.  000b = PF6/GPIO70 001b = PF7/GPIO71 010b = PF14/GPIO78 011b = PF19/GPIO83 100b = PF26/GPIO90 101b = PF27/GPIO91 110b = PF28/GPIO92 111b = PF29/GPIO93

**TABLE 17: LOGICAL PORT 2 FLEXCONNECT TRIGGER PIO CONFIGURATION REGISTER**

FLEX_IN_PORT2 (BFD2_3443h)			FlexConnect Trigger PIO Configuration Register
Bit	Name	R/W	Description
7	USB2_FLEX_IN_EN	R/W	This bit is used for USB2.0 hub.  1b = Enables FlexConnect trigger for the USB2.0 portion of Port 2 through GPIO control. The specific GPIO pin is selected in bits [2:0] of this register. The FlexConnect state is entered upon the rising edge of the selected GPIO. The FlexConnect state is exited upon the falling edge of the selected GPIO. 0b = Disables FlexConnect pin trigger for the USB2.0 portion of Port 2. All other bits in this register are ignored.
6:4	Reserved	R	Reserved
3	USB3_FLEX_IN_EN	R/W	This bit is used for USB3.2 hub.  1b = Enables FlexConnect trigger for the USB3.2 portion of Port 2 through GPIO control. The specific GPIO pin is selected in bits [2:0] of this register. The FlexConnect state is entered upon the rising edge of the selected GPIO. The FlexConnect state is exited upon the falling edge of the selected GPIO. 0b = Disables FlexConnect pin trigger for the USB3.2 portion of Port 2. All other bits in this register are ignored.
2:0	FLEX_IN_IO	R/W	This bit selects the GPIO to be used for the Logical Port 2 FlexConnect trigger.  000b = PF6/GPIO70 001b = PF7/GPIO71 010b = PF14/GPIO78 011b = PF19/GPIO83 100b = PF26/GPIO90 101b = PF27/GPIO91 110b = PF28/GPIO92 111b = PF29/GPIO93

**TABLE 18: PORT 3 FLEXCONNECT TRIGGER PIO CONFIGURATION REGISTER**

FLEX_IN_PORT3 (BFD2_3444h)			FlexConnect Trigger PIO Configuration Register
Bit	Name	R/W	Description
7	USB2_FLEX_IN_EN	R/W	This bit is used for USB2.0 hub.  1b = Enables FlexConnect trigger for the USB2.0 portion of Port 3 through GPIO control. The specific GPIO pin is selected in bits [2:0] of this register. The FlexConnect state is entered upon the rising edge of the selected GPIO. The FlexConnect state is exited upon the falling edge of the selected GPIO. 0b = Disables FlexConnect pin trigger for the USB2.0 portion of Port 3. All other bits in this register are ignored.
6:4	Reserved	R	Reserved

TABLE 18: PORT 3 FLEXCONNECT TRIGGER PIO CONFIGURATION REGISTER (CONTINUED)

FLEX_IN_PORT3 (BFD2_3444h)			FlexConnect Trigger PIO Configuration Register
Bit	Name	R/W	Description
3	USB3_FLEX_IN_EN	R/W	This bit is used for USB3.2 hub.  1b = Enables FlexConnect trigger for the USB3.2 portion of Port 3 through GPIO control. The specific GPIO pin is selected in bits [2:0] of this register. The FlexConnect state is entered upon the rising edge of the selected GPIO. The FlexConnect state is exited upon the falling edge of the selected GPIO. 0b = Disables FlexConnect pin trigger for the USB3.2 portion of Port 3. All other bits in this register are ignored.
2:0	FLEX_IN_IO	R/W	This bit selects the GPIO to be used for the Logical Port 3 FlexConnect trigger.  000b = PF6/GPIO70 001b = PF7/GPIO71 010b = PF14/GPIO78 011b = PF19/GPIO83 100b = PF26/GPIO90 101b = PF27/GPIO91 110b = PF28/GPIO92 111b = PF29/GPIO93

TABLE 19: PORT 4 FLEXCONNECT TRIGGER PIO CONFIGURATION REGISTER

FLEX_IN_PORT4 (BFD2_3445h)			FlexConnect Trigger PIO Configuration Register
Bit	Name	R/W	Description
7	USB2_FLEX_IN_EN	R/W	This bit is used for USB2.0 hub.  1b = Enables FlexConnect trigger for the USB2.0 portion of Port 4 through GPIO control. The specific GPIO pin is selected in bits [2:0] of this register. The FlexConnect state is entered upon the rising edge of the selected GPIO. The FlexConnect state is exited upon the falling edge of the selected GPIO. 0b = Disables FlexConnect pin trigger for the USB2.0 portion of Port 4. All other bits in this register are ignored.
6:4	Reserved	R	Reserved
3	USB3_FLEX_IN_EN	R/W	This bit is used for USB3.2 hub.  1b = Enables FlexConnect trigger for the USB3.2 portion of Port 4 through GPIO control. The specific GPIO pin is selected in bits [2:0] of this register. The FlexConnect state is entered upon the rising edge of the selected GPIO. The FlexConnect state is exited upon the falling edge of the selected GPIO. 0b = Disables FlexConnect pin trigger for the USB3.2 portion of Port 4. All other bits in this register are ignored.

**TABLE 19: PORT 4 FLEXCONNECT TRIGGER PIO CONFIGURATION REGISTER**

FLEX_IN_PORT4 (BFD2_3445h)			FlexConnect Trigger PIO Configuration Register
Bit	Name	R/W	Description
2:0	FLEX_IN_IO	R/W	<p>This bit selects the GPIO to be used for the Logical Port 4 FlexConnect trigger.</p> <p>000b = PF6/GPIO70            001b = PF7/GPIO71            010b = PF14/GPIO78            011b = PF19/GPIO83            100b = PF26/GPIO90            101b = PF27/GPIO91            110b = PF28/GPIO92            111b = PF29/GPIO93</p>

**TABLE 20: PORT 5 FLEXCONNECT TRIGGER PIO CONFIGURATION REGISTER**

FLEX_IN_PORT5 (BFD2_3446h)			FlexConnect Trigger PIO Configuration Register
Bit	Name	R/W	Description
7	USB2_FLEX_IN_EN	R/W	<p>This bit is used for USB2.0 hub.</p> <p>1b = Enables FlexConnect trigger for the USB2.0 portion of Port 5 through GPIO control. The specific GPIO pin is selected in bits [2:0] of this register. The FlexConnect state is entered upon the rising edge of the selected GPIO. The FlexConnect state is exited upon the falling edge of the selected GPIO.</p> <p>0b = Disables FlexConnect pin trigger for the USB2.0 portion of Port 5. All other bits in this register are ignored.</p>
6:4	Reserved	R	Reserved
3	USB3_FLEX_IN_EN	R/W	<p>This bit is used for USB3.2 hub.</p> <p>1b = Enables FlexConnect trigger for the USB3.2 portion of Port 5 through GPIO control. The specific GPIO pin is selected in bits [2:0] of this register. The FlexConnect state is entered upon the rising edge of the selected GPIO. The FlexConnect state is exited upon the falling edge of the selected GPIO.</p> <p>0b = Disables FlexConnect pin trigger for the USB3.2 portion of Port 5. All other bits in this register are ignored.</p>
2:0	FLEX_IN_IO	R/W	<p>This bit selects the GPIO to be used for the Logical Port 5 FlexConnect trigger.</p> <p>000b = PF6/GPIO70            001b = PF7/GPIO71            010b = PF14/GPIO78            011b = PF19/GPIO83            100b = PF26/GPIO90            101b = PF27/GPIO91            110b = PF28/GPIO92            111b = PF29/GPIO93</p>

TABLE 21: PORT 6 FLEXCONNECT TRIGGER PIO CONFIGURATION REGISTER

FLEX_IN_PORT6 (BFD2_3447h)			FlexConnect Trigger PIO Configuration Register
Bit	Name	R/W	Description
7	USB2_FLEX_IN_EN	R/W	This bit is used for USB2.0 hub.  1b = Enables FlexConnect trigger for the USB2.0 portion of Port 6 through GPIO control. The specific GPIO pin is selected in bits [2:0] of this register. The FlexConnect state is entered upon the rising edge of the selected GPIO. The FlexConnect state is exited upon the falling edge of the selected GPIO. 0b = Disables FlexConnect pin trigger for the USB2.0 portion of Port 6. All other bits in this register are ignored.
6:4	Reserved	R	Reserved
3	USB3_FLEX_IN_EN	R/W	This bit is used for USB3.2 hub. <i>This bit has no effect to USB70xx.</i>  1b = Enables FlexConnect trigger for the USB3.2 portion of Port 6 through GPIO control. The specific GPIO pin is selected in bits [2:0] of this register. The FlexConnect state is entered upon the rising edge of the selected GPIO. The FlexConnect state is exited upon the falling edge of the selected GPIO. 0b = Disables FlexConnect pin trigger for the USB3.2 portion of Port 6. All other bits in this register are ignored.
2:0	FLEX_IN_IO	R/W	This bit selects the GPIO to be used for the Logical Port 6 FlexConnect trigger.  000b = PF6/GPIO70 001b = PF7/GPIO71 010b = PF14/GPIO78 011b = PF19/GPIO83 100b = PF26/GPIO90 101b = PF27/GPIO91 110b = PF28/GPIO92 111b = PF29/GPIO93

TABLE 22: PF6 CONTROL REGISTER

PF6_CTL (BF80_0C09h)			Programmable Function 6 Control Register
Bit	Name	R/W	Description
7:3	Reserved	R	These bits are always read as 0.
2:0	Select	R/W	000b = GPIO70 001b = I2S_LRCK 010b = UART_RX 011b = DP1_DISCHARGE 100b = PD_SPI_CE_NO 101b = PRT_CTL1_U3

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**TABLE 23: PF7 CONTROL REGISTER**

PF7_CTL (BF80_0C0Ah)			Programmable Function 7 Control Register
Bit	Name	R/W	Description
7:3	Reserved	R	These bits are always read as 0.
2:0	Select	R/W	000b = GPIO71 001b = I2S_MCLK 010b = UART_TX 011b = DP1_DISCHARGE 100b = PD_SPI_CLK 101b = PRT_CTL2_U3

**TABLE 24: PF14 CONTROL REGISTER**

PF14_CTL (BF80_0C11h)			Programmable Function 14 Control Register
Bit	Name	R/W	Description
7:3	Reserved	R	These bits are always read as 0.
2:0	Select	R/W	000b = GPIO78 001b = I2S_SDI 010b = UART_nCTS 011b = PRT_CTL4/OCS 100b = MSTR_I2C_CLK 101b = UART_nRTS 110b = UART_nDTR

**TABLE 25: PF19 CONTROL REGISTER**

PF19_CTL (BF80_0C16h)			Programmable Function 19 Control Register
Bit	Name	R/W	Description
7:3	Reserved	R	These bits are always read as 0.
2:0	Select	R/W	000b = GPIO83 001b = I2S_SD0 010b = UART_nRTS 011b = SLV_I2C_DATA 100b = MSTR_I2C_DATA

**TABLE 26: PF26 CONTROL REGISTER**

PF26_CTL (BF80_0C1Dh)			Programmable Function 26 Control Register
Bit	Name	R/W	Description
7:3	Reserved	R	These bits are always read as 0.
2:0	Select	R/W	000b = GPIO90 001b = I2S_SCK 010b = UART_nDSR 011b = Reserved 100b = SLV_I2C_CLK

**TABLE 27: PF27 CONTROL REGISTER**

PF27_CTL (BF80_0C1Eh)			Programmable Function 27 Control Register
Bit	Name	R/W	Description
7:3	Reserved	R	These bits are always read as 0.
2:0	Select	R/W	000b = GPIO91 001b = I2S_MCLK 010b = UART_nDTR 011b = Reserved 100b = SLV_I2C_DATA 101b = PRT_CTL6/OCS 110b = UART_RX

**TABLE 28: PF28 CONTROL REGISTER**

PF28_CTL (BF80_0C1F)			Programmable Function 28 Control Register
Bit	Name	R/W	Description
7:3	Reserved	R	These bits are always read as 0.
2:0	Select	R/W	000b = GPIO92 001b = I2S_LRCK 010b = UART_nDSD 011b = PRT_CTL6/OCS 100b = UART_TX

**TABLE 29: PF29 CONTROL REGISTER**

PF29_CTL (BF80_0C20h)			Programmable Function 29 Control Register
Bit	Name	R/W	Description
7:3	Reserved	R	These bits are always read as 0.
2:0	Select	R/W	000b = GPIO93 Others = Reserved

**EXAMPLE 4: FLEXCONNECT VIA PIN CONTROL BY OTP PATCH**

A .cfg example of FlexConnect port 1 on USB7002 through Pin Control PF6 is shown in the following:

- Write 0x00 to 0xBF80\_0C09 to configure PF6 as GPIO70 function.  
`XWRE_BF800C09 = 00`
- Write 0x88 to 0xBF80\_3442 to flex USB2 and USB3 port 1 through PF6.  
`XWRE_BF803442 = 88`
- Write 0x01 to 0xBF80\_5400 to change the device role of port 1 as UFP.  
`XWRE_BF805400 = 01`
- Write 0x00 to 0xBF80\_3C40 to specify VBUS signal is from internal PIO24 and PIO32.  
`XWRE_BF803C40 = 00`
- Configure 0xBF80\_0903 and 0xBF80\_0904 to set the direction of PIO24 and PIO32 as output.  
`XWRE_BF800903 = 01 01`
- Configure 0xBF80\_0923 and 0xBF80\_0924 to set the PIO24 and PIO32 as output high.  
`XWRE_BF800923 = 01 01`

## 6.0 FLEXCONNECT CONFIGURATION SPACE

The FlexConnect Configuration Space is a versatile option that allows for specific settings to be applied only when the hub is in a Flexed state. It encompasses any feature typically configured through hub configuration registers. Examples of such features include port enable/disable, battery charging configuration, and more. The FlexConnect Configuration Space, referred to as FLEXCFG area, utilizes the same command format as general hub configuration files (.cfg) generated with the MPLAB<sup>®</sup> Connect Configurator tool. Therefore, the same methods used for generating general configuration files can also be applied to the FlexConnect Configuration Space. Refer to the following registers and example for additional details on how to use the FlexConnect Configuration Space.

**TABLE 30: FLEX CONFIGURATION CONTROL REGISTER**

FLEX_CTL_REG (BFD2_345Bh)			Flex Configuration Control Register
Bit	Name	R/W	Description
7	OTP_FLEXCFG	R/W	<p>This bit indicates if the data in the FLEXCFG area is dynamically provided by the USB host or if it is statically configured on a per-port basis through hub OTP memory.</p> <p>1b = Each flex port shall have its own configuration chunk within the FLEXCFG_DATA. The data for each port shall begin right at the start of the offset in the FLEXCFG area. APPLY_FLEXCFG and FLEX_CFG_LEN are all invalid in this mode of operation.</p> <p>0b = FLEXCFG area shall be dynamically populated by the host. This method allows for the highest level of flexibility, but requires software on the USB host to control FlexConnect and load new FLEXCFG data prior to each FlexConnect transition.</p>
6:1	Reserved	R	Reserved
0	APPLY_FLEXCFG	R/W	<p>1b = FLEXCFG configuration of length specified in the FLEXCFG_LEN register will be applied during the Flex state transition.</p> <p>0b = FLEXCFG configuration will not be applied on the next Flex state transition.</p>

TABLE 31: FLEX CONFIGURATION DATA REGISTERS

FLEXCFG_DATA (BFD2_3800h-BFD2_3BFFh)			Flex Configuration Data Registers
Byte	Name	R/W	Description
1,023:0	FLEXCFG_DATA	R/W	<p>Bytes from the configurations for FLEXCFG are programmed here. Up to 1,024 bytes of configuration data may be loaded. The standard OTP configuration file format shall be used. See AN2810 - Configuration of USB7002/USB7006/USB7016/USB705x (<a href="http://www.microchip.com/DS00002810">www.microchip.com/DS00002810</a>) for details on configuration file formatting, or use the MPLAB Connect Configurator tool to generate a .cfg file. The binary data within the .cfg file can be placed directly into these registers.</p> <p>When OTP_FLEXCFG = 0b, then the entire FLEXCFG_DATA space may be used, and the length of the configuration data must be properly defined in FLEXCFG_LEN.</p> <p>When OTP_FLEXCFG = 1b, this space is chunked into portions that are allocated to logical port numbers. When FlexConnect is initiated to a logical port, the FLEXCFG data that pertains only to that logical port is loaded.</p> <p>Logical Port 1: Bytes 00 - 170            Logical Port 2: Bytes 171 - 340            Logical Port 3: Bytes 341 - 510            Logical Port 4: Bytes 511 - 680            Logical Port 5: Bytes 681 - 850            Logical Port 6: Bytes 851 - 1,020            Unused: Bytes 1,021 - 1,023</p>

TABLE 32: FLEX CONFIGURATION LENGTH REGISTERS

FLEXCFG_LEN (BFD2_345Ch)			Flex Configuration Length Registers
Bit	Name	R/W	Description
15:10	Reserved	R	Reserved
9:0	FLEXCFG_LEN	R/W	This field indicates the length of the FLEXCFG data. This is only used if OTP_FLEXCFG = 0b.

### 6.1 Recommended Procedure for a Dynamic USB Host-Controlled FLEXCFG Data (OTP\_FLEXCFG = 0b)

The recommended procedure for implementing dynamic USB Host-controlled FLEXCFG is as follows:

1. Create a configuration file with all the options that will be applied after flexing.
2. Program the bytes from the configuration file starting at the first register of FLEXCFG\_DATA (BFD2\_3800h).
3. Program the length of the data in the configuration file/FLEXCFG\_DATA area into the FLEXCFG\_LEN register.
4. Set the APPLY\_FLEXCFG bit in the FLEX\_CTL\_REG register.
5. Send the FlexConnect USB command SET\_ROLE\_SWITCH.

At this point, the data from the FLEXCFG\_DATA registers of length FLEXCFG\_LEN will be applied to the hub and can be seen by the new flexed host.

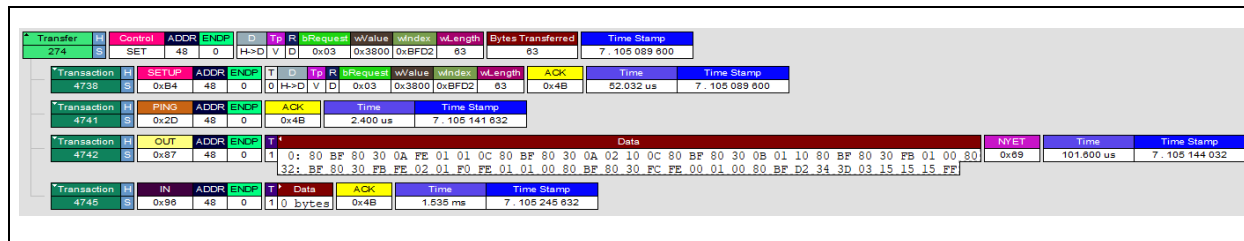
If the same configuration will be programmed when the next FlexConnect occurs, rewrite the length of the FLEXCFG patch in FLEXCFG\_LEN and send the FlexConnect USB command. If FLEXCFG\_DATA will be updated, clear out the data in the FLEXCFG\_DATA area and repeat the recommended procedure.

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The following is an example configuration that might be programmed into the FLEXCFG area as well as a USB trace of the process:

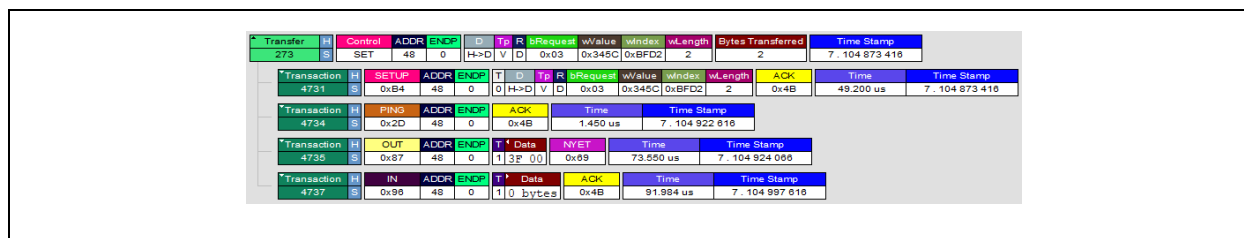
1. Create a configuration file with all the options that will be applied after flexing.  
In this example, FlexConnect will be sent to port 1. This configuration file will disable ports 2 to 4 and set them to be dedicated charging ports (DCPs). After flexing, the new host will see a two-port hub with the other three ports set to DCP.
2. Program the bytes from the configuration file starting at the first register of FLEXCFG\_DATA (BFD2\_3800h).  
See Figure 10.

**FIGURE 10: WRITING FLEXCFG\_DATA TRANSACTION EXAMPLE**



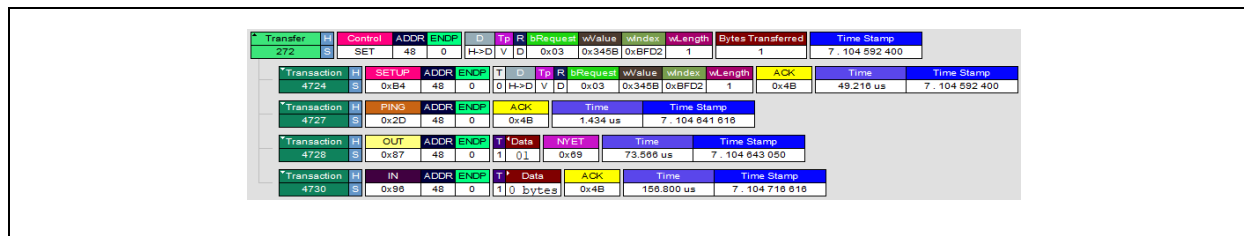
3. Program the length of the data in the configuration file/FLEXCFG\_DATA area into the FLEXCFG\_LEN register.  
See Figure 11.

**FIGURE 11: WRITING FLEXCFG\_LEN TRANSACTION EXAMPLE**



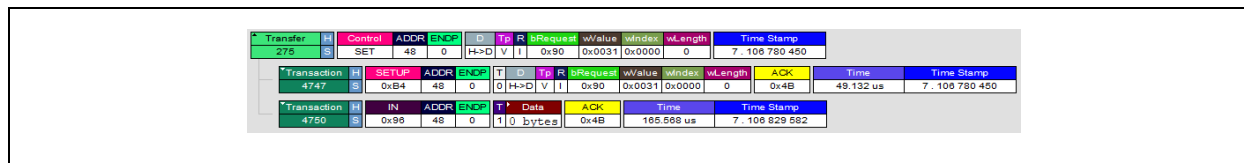
4. Set the APPLY\_FLEXCFG bit in the FLEX\_CTL\_REG register.  
See Figure 12.

**FIGURE 12: WRITING FLEX\_CTL\_REG TRANSACTION EXAMPLE**



5. Send the FlexConnect USB command SET\_ROLE\_SWITCH.  
See Figure 13.

**FIGURE 13: SENDING FLEXCONNECT COMMAND TO PORT 1 TRANSACTION EXAMPLE**



**Note:** Battery charging enabling/disabling through the FLEXCFG area is not supported. If battery charging is to be enabled on a port via the FLEXCFG area like in the example above, battery charging *must* also be enabled via OTP or strapping in the original unflexed configuration. For example, if port 2 is to be configured as a battery charging port in the FLEXCFG area, then battery charging must be enabled via the CFG\_BC\_EN strap or OTP write in the default Unflexed state.

## 7.0 ADDITIONAL HARDWARE CONSIDERATIONS

Schematics for FlexConnect applications are implementation-specific and, hence, do not necessarily follow any common framework. The succeeding sections show few, common considerations that must be made for each design.

### 7.1 Host VBUS Detection

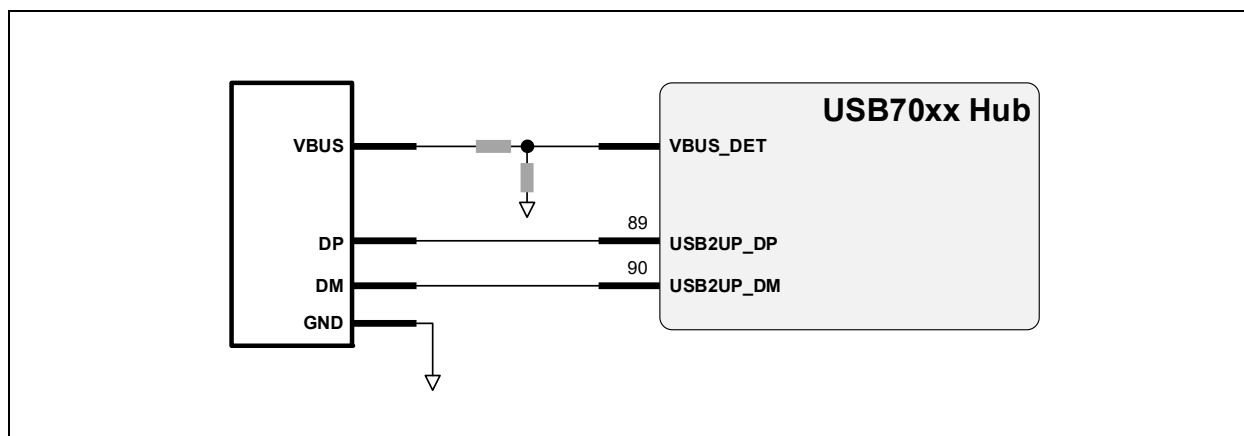
The upstream VBUS detection is a signal used by the hub to determine when a USB host is connected. When VBUS\_MON\_UP/VBUS\_DET is not present, the hub enters a Low-Power state to conserve energy. This causes the hub to disconnect from either the upstream port or the new flexed upstream port.

#### 7.1.1 NO POWER ROLE SWAP VBUS\_DET IMPLEMENTATION

When initiating FlexConnect without changing power roles, it is possible to directly connect VBUS\_DET to the VBUS pin of the default USB host through a resistor divider. As shown in Figure 14, this is a popular implementation in the automotive application space as the head unit will always be connected to the hub.

**Note:** Ensure that the default USB host will not toggle its VBUS supply at any time when FlexConnect is initiated. Otherwise, the hub will be reset and revert to its default state.

**FIGURE 14: NO POWER ROLE SWAP VBUS\_DET CONFIGURATION**



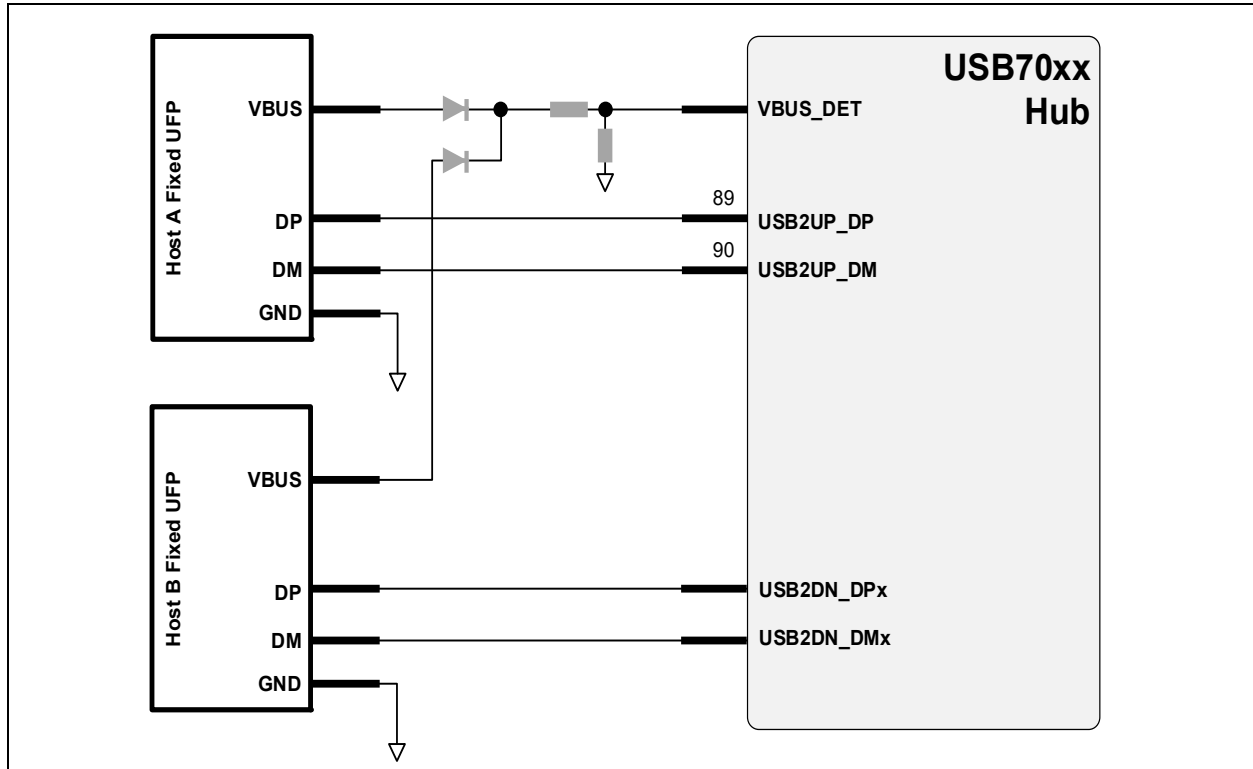
#### 7.1.2 CONNECTING VBUS\_DET DIRECTLY TO A FIXED 3.3V

If Low-Power states are unnecessary when there is no USB host, it is permissible to connect VBUS\_DET to a stable 3.3V supply on the PCB. However, this approach is recommended only for designs where the hub is connected to an embedded host. In certain cases, a USB host might attempt a hard Reset on a device by toggling VBUS, but the hub will not be reset in such instances.

## 7.1.3 'OR'-ING ALL HOST VBUS CONNECTIONS TO VBUS\_DET

In Host-Sharing-type systems, 'OR'-ing all host VBUS connections is an appropriate solution as shown in [Figure 15](#). This can be used when the "one-host-at-a-time" implementation is used. The disadvantage with this type of solution is that there is no way to distinguish which host port is actually supplying VBUS.

**FIGURE 15: DIODE-OR VBUS\_DET SIGNALS**



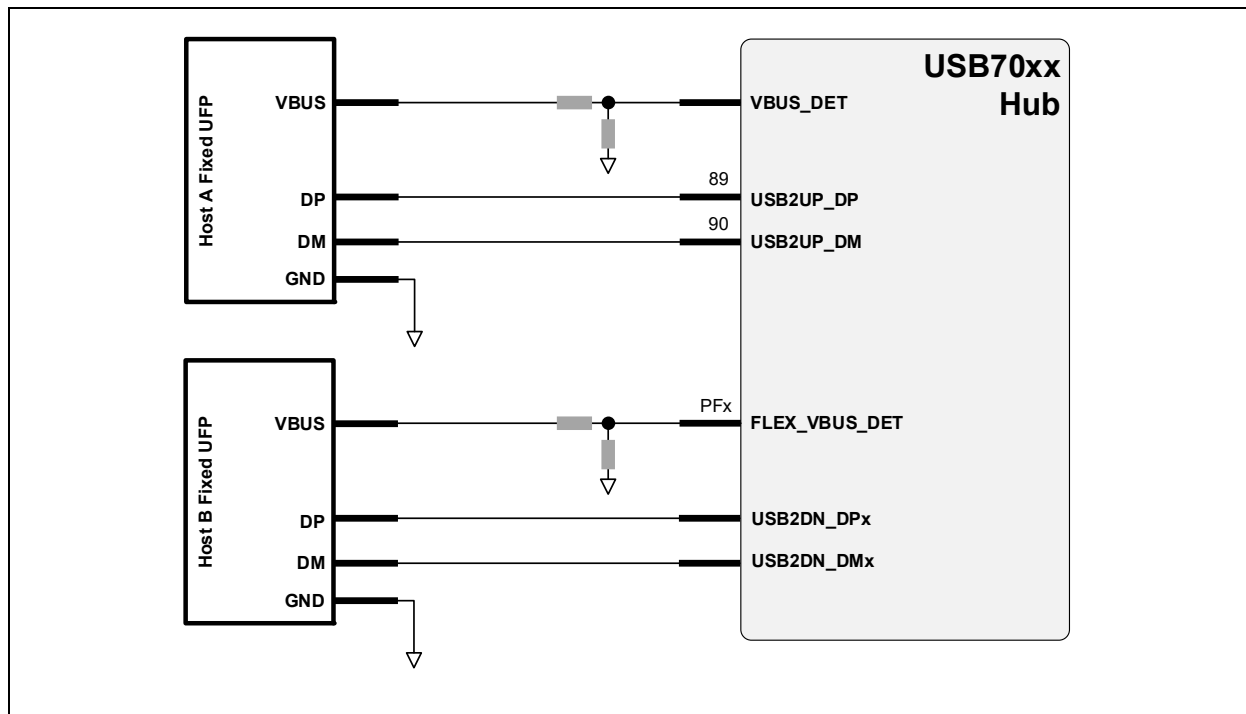
**Note:** The resistor divider values change depending on the characteristics of the diodes used.

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## 7.1.4 ASSIGNING A SPECIFIC FLEX\_VBUS\_DET PIN

An available PFx/GPIOx pin may be reassigned the role of FLEX\_VBUS\_DET permanently via the hub OTP configuration. If using the FLEX\_VBUS\_DET option, the default VBUS\_DET pin is ignored while in the Flexed state. Likewise, the FLEX\_VBUS\_DET pin state is ignored while the hub is in default state. Note that when FLEX\_VBUS\_DET is enabled, the PIO24 and PIO32 options in [VBUS Pass Through Register](#) are selected automatically, and the states of PIO24 and PIO32 follow the FLEX\_VBUS\_DET pin. See [Figure 7](#).

**FIGURE 16: FLEX\_VBUS\_DET SIGNALS**



The register for controlling this feature is detailed in [Table 33](#).

**TABLE 33: FLEX\_VBUS\_DET CONFIGURATION REGISTER**

FLEX_VBUSDET (BFD2_3454h)			FlexConnect VBUS Detect Configuration Register
Bit	Name	R/W	Description
7	FLEX_VBUSDET_EN	R/W	1b = The specific GPIO is selected in bits [2:0] of this register as the VBUS detection pin while the hub is in the Flexed state. 0b = The default VBUS_DET/VBUS_MON_UP pin is also the VBUS detection pin while in the Flexed state.
6	FLEX_VBUSDET_HIGH	R/W	1b = VBUS to hub controller logic is from PIO24/PIO32, and are forced high internally. All other bits in this register is ignored. 0b = VBUS to the hub controller logic is driven based on FLEX_VBUSDET_EN.
5:3	Reserved	R	Reserved

**TABLE 33: FLEX\_VBUS\_DET CONFIGURATION REGISTER (CONTINUED)**

FLEX_VBUSDET (BFD2_3454h)			FlexConnect VBUS Detect Configuration Register
Bit	Name	R/W	Description
2:0	FLEX_VBUSDET_IN	R/W	Selects the GPIO to be used as FLEX_VBUS_DET  000b = PF6/GPIO70 001b = PF7/GPIO71 010b = PF14/GPIO78 011b = PF19/GPIO83 100b = PF26/GPIO90 101b = PF27/GPIO91 110b = PF28/GPIO92 111b = PF29/GPIO93

## 7.2 Ports 1-6 Port Power Control

The required behavior of the PRT\_CTLx pins should be considered before and after the FlexConnect mode is initiated during the system architecture design phase of the application.

Additional configuration options exist that allow the end system integrator to change how PRT\_CTLx works while in the Flexed state or assign an entirely new output signal to be activated while in the Flexed state. [Table 34](#) describes the possible configuration options.

**TABLE 34: PRT\_CTLX BEHAVIORAL OPTIONS**

FLEX_PRTCTL_EN	FLEX_PRTCTL_PIO_EN	Unflexed Port Control Output Behavior	Flexed Port Control Output Behavior
0 (default)	0 (default)	PRT_CTLx: Controlled from USB host commands. The pin will enable an internal 50 kΩ pull-up resistor when the USB host issues to command to enable power to the port, and will drive low during hub initialization or when the USB host issues to command to disable power to the port.	PRT_CTLx: Set to Output and Drive High FLEX_PRTCTL: No action
0	1		PRT_CTLx: Set to Output and Drive High FLEX_PRTCTL: No action
1	0	FLEX_PRTCTL: No action	PRT_CTLx: Set per PRTCTL_OUT[1:0] bit field FLEX_PRTCTL: No action
1	1		PRT_CTLx: Set to Output and Drive High FLEX_PRTCTL: Selected GPIO is set per PRTCTL_OUT[1:0] bit field.

Each physical port that utilizes the FlexConnect feature must be configured if settings that deviate from the default options are desired by the end system integrator.

**TABLE 35: PHYSICAL PORT 1 FLEXCONNECT PORT POWER CONTROL REGISTER**

FLEX_PRTCTL_PORT1 (BFD2_344Eh)			FlexConnect Port Power Control Register
Bit	Name	R/W	Description
7	FLEX_PRTCTL_EN	R/W	1b = Enables alternate port power control operation that functions per the control bits within this register. 0b = Default operation. The standard PRT_CTL1 is set as an output and driven high while in the flexed state.
6:5	PRTCTL_OUT[1:0]	R/W	00b = Tri-stated 01b = Drive high 10b = Drive low 11b = Internal pull-up resistor

**TABLE 35: PHYSICAL PORT 1 FLEXCONNECT PORT POWER CONTROL REGISTER**

FLEX_PRTCTL_PORT1 (BFD2_344Eh)			FlexConnect Port Power Control Register
Bit	Name	R/W	Description
4	Reserved	R	Reserved
3	FLEX_PRTCTL_PIO_EN	R/W	1b = GPIO selected in FLEX_PRTCTL_PIO is set to the state selected in PRTCTL_OUT[1:0]. 0b = The standard PRT_CTL1 pin is set to the state selected in PRTCTL_OUT[1:0].
2:0	FLEX_PRTCTL_PIO	R/W	This bit selects the GPIO to be used for the Physical Port 1 FlexConnect port power control.  000b = PF6/GPIO70 001b = PF7/GPIO71 010b = PF14/GPIO78 011b = PF19/GPIO83 100b = PF26/GPIO90 101b = PF27/GPIO91 110b = PF28/GPIO92 111b = PF29/GPIO93

**TABLE 36: PHYSICAL PORT 2 FLEXCONNECT PORT POWER CONTROL REGISTER**

FLEX_PRTCTL_PORT2 (BFD2_344Fh)			FlexConnect Port Power Control Register
Bit	Name	R/W	Description
7	FLEX_PRTCTL_EN	R/W	1b = Enables alternate port power control operation that functions per the control bits within this register. 0b = Default operation. The standard PRT_CTL2 is set as an output and driven high while in the flexed state.
6:5	PRTCTL_OUT[1:0]	R/W	00b = Tri-stated 01b = Drive high 10b = Drive low 11b = Internal pull-up resistor
4	Reserved	R	Reserved
3	FLEX_PRTCTL_PIO_EN	R/W	1b = GPIO selected in FLEX_PRTCTL_PIO is set to the state selected in PRTCTL_OUT[1:0]. 0b = The standard PRT_CTL2 pin is set to the state selected in PRTCTL_OUT[1:0].
2:0	FLEX_PRTCTL_PIO	R/W	This bit selects the GPIO to be used for the Physical Port 2 FlexConnect port power control.  000b = PF6/GPIO70 001b = PF7/GPIO71 010b = PF14/GPIO78 011b = PF19/GPIO83 100b = PF26/GPIO90 101b = PF27/GPIO91 110b = PF28/GPIO92 111b = PF29/GPIO93

TABLE 37: PHYSICAL PORT 3 FLEXCONNECT PORT POWER CONTROL REGISTER

FLEX_PRTCTL_PORT3 (BFD2_3450h)			FlexConnect Port Power Control Register
Bit	Name	R/W	Description
7	FLEX_PRTCTL_EN	R/W	1b = Enables alternate port power control operation that functions per the control bits within this register. 0b = Default operation. The standard PRT_CTL3 is set as an output and driven high while in the flexed state.
6:5	PRTCTL_OUT[1:0]	R/W	00b = Tri-stated 01b = Drive high 10b = Drive low 11b = Internal pull-up resistor
4	Reserved	R	Reserved
3	FLEX_PRTCTL_PIO_EN	R/W	1b = GPIO selected in FLEX_PRTCTL_PIO is set to the state selected in PRTCTL_OUT[1:0]. 0b = The standard PRT_CTL3 pin is set to the state selected in PRTCTL_OUT[1:0].
2:0	FLEX_PRTCTL_PIO	R/W	This bit selects the GPIO to be used for the Physical Port 3 FlexConnect port power control.  000b = PF6/GPIO70 001b = PF7/GPIO71 010b = PF14/GPIO78 011b = PF19/GPIO83 100b = PF26/GPIO90 101b = PF27/GPIO91 110b = PF28/GPIO92 111b = PF29/GPIO93

TABLE 38: PHYSICAL PORT 4 FLEXCONNECT PORT POWER CONTROL REGISTER

FLEX_PRTCTL_PORT4 (BFD2_3451h)			FlexConnect Port Power Control Register
Bit	Name	R/W	Description
7	FLEX_PRTCTL_EN	R/W	1b = Enables alternate port power control operation that functions per the control bits within this register. 0b = Default operation. The standard PRT_CTL4 is set as an output and driven high while in the Flexed state.
6:5	PRTCTL_OUT[1:0]	R/W	00b = Tri-stated 01b = Drive high 10b = Drive low 11b = Internal pull-up resistor
4	Reserved	R	Reserved
3	FLEX_PRTCTL_PIO_EN	R/W	1b = GPIO selected in FLEX_PRTCTL_PIO is set to the state selected in PRTCTL_OUT[1:0]. 0b = The standard PRT_CTL4 pin is set to the state selected in PRTCTL_OUT[1:0].

**TABLE 38: PHYSICAL PORT 4 FLEXCONNECT PORT POWER CONTROL REGISTER**

FLEX_PRTCTL_PORT4 (BFD2_3451h)			FlexConnect Port Power Control Register
Bit	Name	R/W	Description
2:0	FLEX_PRTCTL_PIO	R/W	<p>This bit selects the GPIO to be used for the Physical Port 4 FlexConnect port power control.</p> <p>000b = PF6/GPIO70            001b = PF7/GPIO71            010b = PF14/GPIO78            011b = PF19/GPIO83            100b = PF26/GPIO90            101b = PF27/GPIO91            110b = PF28/GPIO92            111b = PF29/GPIO93</p>

**TABLE 39: PHYSICAL PORT 5 FLEXCONNECT PORT POWER CONTROL REGISTER**

FLEX_PRTCTL_PORTS5 (BFD2_3452h)			FlexConnect Port Power Control Register
Bit	Name	R/W	Description
7	FLEX_PRTCTL_EN	R/W	<p>1b = Enables alternate port power control operation that functions per the control bits within this register.            0b = Default operation. The standard PRT_CTL5 is set as an output and driven high while in the flexed state.</p>
6:5	PRTCTL_OUT[1:0]	R/W	<p>00b = Tri-stated            01b = Drive high            10b = Drive low            11b = Internal pull-up resistor</p>
4	Reserved	R	Reserved
3	FLEX_PRTCTL_PIO_EN	R/W	<p>1b = GPIO selected in FLEX_PRTCTL_PIO is set to the state selected in PRTCTL_OUT[1:0].            0b = The standard PRT_CTL5 pin is set to the state selected in PRTCTL_OUT[1:0].</p>
2:0	FLEX_PRTCTL_PIO	R/W	<p>This bit selects the GPIO to be used for the Physical Port 5 FlexConnect port power control.</p> <p>000b = PF6/GPIO70            001b = PF7/GPIO71            010b = PF14/GPIO78            011b = PF19/GPIO83            100b = PF26/GPIO90            101b = PF27/GPIO91            110b = PF28/GPIO92            111b = PF29/GPIO93</p>

TABLE 40: PHYSICAL PORT 6 FLEXCONNECT PORT POWER CONTROL REGISTER

FLEX_PRTCTL_PORT6 (BFD2_3453h)			FlexConnect Port Power Control Register
Bit	Name	R/W	Description
7	FLEX_PRTCTL_EN	R/W	1b = Enables alternate port power control operation that functions per the control bits within this register. 0b = Default operation. The standard PRT_CTL6 is set as an output and driven high while in the flexed state.
6:5	PRTCTL_OUT[1:0]	R/W	00b = Tri-stated 01b = Drive high 10b = Drive low 11b = Internal pull-up resistor
4	Reserved	R	Reserved
3	FLEX_PRTCTL_PIO_EN	R/W	1b = GPIO selected in FLEX_PRTCTL_PIO is set to the state selected in PRTCTL_OUT[1:0]. 0b = The standard PRT_CTL6 pin is set to the state selected in PRTCTL_OUT[1:0].
2:0	FLEX_PRTCTL_PIO	R/W	This bit selects the GPIO to be used for the Physical Port 6 FlexConnect port power control.  000b = PF6/GPIO70 001b = PF7/GPIO71 010b = PF14/GPIO78 011b = PF19/GPIO83 100b = PF26/GPIO90 101b = PF27/GPIO91 110b = PF28/GPIO92 111b = PF29/GPIO93

## 7.3 FlexConnect State Indicator Output

GPIOs may also be assigned the role of FlexConnect status indicator outputs. The use of these outputs is completely optional. These outputs can be connected to external LEDs or an embedded microcontroller to communicate the current FlexConnect state.

The GPIO can be configured as drive-high/drive-low or open-drain, and the polarity can be configured. This mode should not be used in combination with the FlexConnect GPIO input mode.

**Note:** These outputs operate with respect to the PHYSICAL port numbering (which is different than the FlexConnect input control operation).

**TABLE 41: PHYSICAL PORT 1 FLEXCONNECT STATE INDICATOR GPIO CONFIGURATION REGISTER**

FLEX_OUT_PORT1 (BFD2_3448h)			FlexConnect State Indicator GPIO Configuration
Bit	Name	R/W	Description
7	FLEX_OUT_EN	R/W	1b = Enables FlexConnect state indicator for Port 1 through GPIO. The specific GPIO is selected in bits [2:0] of this register. 0b = Disables FlexConnect state indicator for Port 1 through GPIO. All other bits in this register are ignored.
6	FLEX_OUT_ACTIVE_HIGH	R/W	1b = The selected GPIO is driven active-high while in FlexConnect state. Driven low otherwise. 0b = The selected GPIO is driven active-low while in FlexConnect state. Driven high otherwise.
5	FLEX_OUT_OD	R/W	1b = The selected GPIO is open-drain Output mode. 0b = The selected GPIO is drive-high/drive-low Output mode.
4:3	Reserved	R	Reserved
2:0	FLEX_OUT_IO	R/W	This bit selects the GPIO to be used for the Physical Port 1 FlexConnect state indicator.  000b = PF6/GPIO70 001b = PF7/GPIO71 010b = PF14/GPIO78 011b = PF19/GPIO83 100b = PF26/GPIO90 101b = PF27/GPIO91 110b = PF28/GPIO92 111b = PF29/GPIO93

**TABLE 42: PHYSICAL PORT 2 FLEXCONNECT STATE INDICATOR GPIO CONFIGURATION REGISTER**

FLEX_OUT_PORT2 (BFD2_3449h)			FlexConnect State Indicator GPIO Configuration
Bit	Name	R/W	Description
7	FLEX_OUT_EN	R/W	1b = Enables FlexConnect state indicator for Port 2 through GPIO. The specific GPIO is selected in bits [2:0] of this register. 0b = Disables FlexConnect state indicator for Port 2 through GPIO. All other bits in this register are ignored.
6	FLEX_OUT_ACTIVE_HIGH	R/W	1b = The selected GPIO is driven active-high while in FlexConnect state. Driven low otherwise. 0b = The selected GPIO is driven active-low while in FlexConnect state. Driven high otherwise.

**TABLE 42: PHYSICAL PORT 2 FLEXCONNECT STATE INDICATOR GPIO CONFIGURATION REGISTER (CONTINUED)**

FLEX_OUT_PORT2 (BFD2_3449h)			FlexConnect State Indicator GPIO Configuration
Bit	Name	R/W	Description
5	FLEX_OUT_OD	R/W	1b = The selected GPIO is open-drain Output mode. 0b = The selected GPIO is drive-high/drive-low Output mode.
4:3	Reserved	R	Reserved
2:0	FLEX_OUT_IO	R/W	This bit selects the GPIO to be used for the Physical Port 2 FlexConnect state indicator.  000b = PF6/GPIO70 001b = PF7/GPIO71 010b = PF14/GPIO78 011b = PF19/GPIO83 100b = PF26/GPIO90 101b = PF27/GPIO91 110b = PF28/GPIO92 111b = PF29/GPIO93

**FIGURE 17: PHYSICAL PORT 3 FLEXCONNECT STATE INDICATOR GPIO CONFIGURATION REGISTER**

FLEX_OUT_PORT3 (BFD2_344Ah)			FlexConnect State Indicator GPIO Configuration
Bit	Name	R/W	Description
7	FLEX_OUT_EN	R/W	1b = Enables FlexConnect state indicator for Port 3 through GPIO. The specific GPIO is selected in bits [2:0] of this register. 0b = Disables FlexConnect state indicator for Port 3 through GPIO. All other bits in this register are ignored.
6	FLEX_OUT_ACTIVE_HIGH	R/W	1b = The selected GPIO is driven active-high while in FlexConnect state. Driven low otherwise. 0b = The selected GPIO is driven active-low while in FlexConnect state. Driven high otherwise.
5	FLEX_OUT_OD	R/W	1b = The selected GPIO is open-drain Output mode. 0b = The selected GPIO is drive-high/drive-low Output mode.
4:3	Reserved	R	Reserved
2:0	FLEX_OUT_IO	R/W	This bit selects the GPIO to be used for the Physical Port 3 FlexConnect state indicator.  000b = PF6/GPIO70 001b = PF7/GPIO71 010b = PF14/GPIO78 011b = PF19/GPIO83 100b = PF26/GPIO90 101b = PF27/GPIO91 110b = PF28/GPIO92 111b = PF29/GPIO93

**TABLE 43: PHYSICAL PORT 4 FLEXCONNECT STATE INDICATOR GPIO CONFIGURATION REGISTER**

FLEX_OUT_PORT4 (BFD2_344Bh)			FlexConnect State Indicator GPIO Configuration
Bit	Name	R/W	Description
7	FLEX_OUT_EN	R/W	1b = Enables FlexConnect state indicator for Port 4 through GPIO. The specific GPIO is selected in bits [2:0] of this register. 0b = Disables FlexConnect state indicator for Port 4 through GPIO. All other bits in this register are ignored.
6	FLEX_OUT_ACTIVE_HIGH	R/W	1b = The selected GPIO is driven active-high while in FlexConnect state. Driven low otherwise. 0b = The selected GPIO is driven active-low while in FlexConnect state. Driven high otherwise.
5	FLEX_OUT_OD	R/W	1b = The selected GPIO is open-drain Output mode. 0b = The selected GPIO is drive-high/drive-low Output mode.
4:3	Reserved	R	Reserved
2:0	FLEX_OUT_IO	R/W	This bit selects the GPIO to be used for the Physical Port 4 FlexConnect state indicator.  000b = PF6/GPIO70 001b = PF7/GPIO71 010b = PF14/GPIO78 011b = PF19/GPIO83 100b = PF26/GPIO90 101b = PF27/GPIO91 110b = PF28/GPIO92 111b = PF29/GPIO93

**TABLE 44: PHYSICAL PORT 5 FLEXCONNECT STATE INDICATOR GPIO CONFIGURATION REGISTER**

FLEX_OUT_PORT5 (BFD2_344Ch)			FlexConnect State Indicator GPIO Configuration
Bit	Name	R/W	Description
7	FLEX_OUT_EN	R/W	1b = Enables FlexConnect state indicator for Port 5 through GPIO. The specific GPIO is selected in bits [2:0] of this register. 0b = Disables FlexConnect state indicator for Port 5 through GPIO. All other bits in this register are ignored.
6	FLEX_OUT_ACTIVE_HIGH	R/W	1b = The selected GPIO is driven active-high while in FlexConnect state. Driven low otherwise. 0b = The selected GPIO is driven active-low while in FlexConnect state. Driven high otherwise.
5	FLEX_OUT_OD	R/W	1b = The selected GPIO is open-drain Output mode. 0b = The selected GPIO is drive-high/drive-low Output mode.
4:3	Reserved	R	Reserved

**TABLE 44: PHYSICAL PORT 5 FLEXCONNECT STATE INDICATOR GPIO CONFIGURATION REGISTER (CONTINUED)**

FLEX_OUT_PORT5 (BFD2_344Ch)			FlexConnect State Indicator GPIO Configuration
Bit	Name	R/W	Description
2:0	FLEX_OUT_IO	R/W	This bit selects the GPIO to be used for the Physical Port 5 FlexConnect state indicator.  000b = PF6/GPIO70 001b = PF7/GPIO71 010b = PF14/GPIO78 011b = PF19/GPIO83 100b = PF26/GPIO90 101b = PF27/GPIO91 110b = PF28/GPIO92 111b = PF29/GPIO93

**TABLE 45: PHYSICAL PORT 6 FLEXCONNECT STATE INDICATOR GPIO CONFIGURATION REGISTER**

FLEX_OUT_PORT6 (BFD2_344Dh)			FlexConnect State Indicator GPIO Configuration
Bit	Name	R/W	Description
7	FLEX_OUT_EN	R/W	1b = Enables FlexConnect state indicator for Port 6 through GPIO. The specific GPIO is selected in bits [2:0] of this register. 0b = Disables FlexConnect state indicator for Port 6 through GPIO. All other bits in this register are ignored.
6	FLEX_OUT_ACTIVE_HIGH	R/W	1b = The selected GPIO is driven active-high while in FlexConnect state. Driven low otherwise. 0b = The selected GPIO is driven active-low while in FlexConnect state. Driven high otherwise.
5	FLEX_OUT_OD	R/W	1 = The selected GPIO is open-drain Output mode. 0b = The selected GPIO is drive-high/drive-low Output mode.
4:3	Reserved	R	Reserved
2:0	FLEX_OUT_IO	R/W	This bit selects the GPIO to be used for the Physical Port 6 FlexConnect state indicator.  000b = PF6/GPIO70 001b = PF7/GPIO71 010b = PF14/GPIO78 011b = PF19/GPIO83 100b = PF26/GPIO90 101b = PF27/GPIO91 110b = PF28/GPIO92 111b = PF29/GPIO93

#### 7.4 FlexConnect Hub Attach Delay

Certain systems may require a specific amount of debounce or delay between when the hub is issued the FlexConnect command and when it attempts to reattach in the Flexed state. This feature may also be useful during debugging or troubleshooting systems. See [Table 46](#) and [Table 47](#).

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**TABLE 46: FLEXCONNECT HUB ATTACH DELAY REGISTER**

FLEX_ATTACH_DELAY (BFD2_3455h)			FlexConnect Hub Attach Delay Register
Bit	Name	R/W	Description
7:0	FLEX_ATTACH_DELAY	R/W	<p>This field may be used to add a delay between the moment when the FlexConnect command is issued and the hub detaches, and when the hub flexes and reattaches (enables the D+ pull-up of the upstream port) in the Flexed state.</p> <p>This delay is in increments of 10 ms. For example, a value of two provides 20 ms of delay before the USB hub reattaches in the Flexed state after the FlexConnect command is received.</p> <p>The default setting is 0x00.</p>

**TABLE 47: FLEXCONNECT ROLE SWITCH DELAY REGISTER**

ROLE_SWITCH_DELAY (BFD2_3456h)			FlexConnect Role Switch Delay Register
Bit	Name	R/W	Description
7:0	ROLE_SWITCH_DELAY	R/W	<p>This field refers to the amount of time by which role switch will be delayed once SET_ROLE_SWITCH command is initiated. This might be required with specific USB hosts where a debounce time is required between USB device detach and subsequent attach.</p> <p>This delay is in increments of 10 ms. For example, a value of two in this register provides 20 ms delay before role switch.</p> <p>The default setting is 0x00.</p>

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## APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00005057A (07-19-23)	Initial release	

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