PolarFire FPGA 10GBASEKR Ethernet

AN5069

Introduction (Ask a Question)

The PolarFire® FPGA 10G Ethernet solution is compliant to IEEE® 802.3ae standard, which supports data transfer rates up to 10.3125 Gbps. The benefits of using PolarFire FPGAs for developing 10G Ethernet solutions include the utilization of low-power transceivers, low-power FPGA fabric, and an in-built SyncE-compliant jitter attenuation. The 10G Ethernet solution is implemented using the Core10GMAC soft IP Media Access Control (MAC) core and 10GBASEKR IP.

This application note includes the 10GBASEKR Libero® project, which is used as a reference design for building a 10GBASEKR Ethernet application. This design is validated with a proven third-party inter-op device, which is Vitesse SparX-5i board, and using two PolarFire Evaluation boards as listed:

- 10GBASEKR Ethernet design using third party link partner
- 10GBASEKR Ethernet design using two PolarFire Evaluation boards

This 10GBASEKR Ethernet demo design is programmed using either of the following options:

- Programming `.job` file: To program the device using the `.job` file provided with the design files, see 7. Appendix 1: Programming the Device Using FlashPro Express.
- Libero SoC: To program the device using Libero SoC, see 5.7. Run Program Action. Use this option when the demo design is modified.

Resource Utilization (Ask a Question)

The resource utilization report is saved in the `BASEKR_TOP_layout_log.log` file. To view this file, go to the **Reports** > **Place and Route** in the Libero tool.

The following table lists the resource utilization of the design after place and route. These values vary slightly for different Libero runs, settings, and seed values.

Table 1. Resource Utilization

Type	Used	Total	Percentage %
4LUT	22461	299544	7.5
DFF	15889	299544	5.3
Logic Element	26130	299544	8.72

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1. Requirements (Ask a Question)

The following table lists the hardware and software requirements for running the demo.

Table 1-1. Requirements

Requirement	Version
Hardware	
PolarFire® Evaluation Kit (MPF300-EVAL-KIT)	Rev D or later
VSC SparX-5i	—
Small form-factor pluggable (SFP+) module - Finisar board	—
Software	
Libero® SoC Design Suite	See the `readme.txt` file provided in the design files for all software versions needed to create this reference design.
FlashPro Express	—
SoftConsole	See the `readme.txt` file provided in the design files for all software versions needed to create this reference design.

Important: Libero SmartDesign and configuration screen shots shown in this guide are for illustration purpose only. Open the Libero design to see the latest updates.

2. Prerequisites (Ask a Question)

1. Download the design files from: www.microchip.com/en-us/application-notes/AN5069. The design files folder contains the following subfolders:
   - Programming_Job: One programming file (.job) is provided
   - Source: Contains the source files required to complete this application note
   - Tcl_Scripts: Contains the Tcl scripts for the design
   - Softconsole: Contains Softconsole project for this design
2. Download and install Libero SoC from: Libero SoC Documentation.
3. Download and install the SoftConsole software from: SoftConsole.
4. From the Libero Catalog, download the latest versions of the IP cores from the warning pop-up as shown in the following figure.

Figure 2-1. Download New Cores Option

5. From the **Project** menu, click **Open** project.
6. Navigate to the `mpf_an5069_v2023p1_df/mpf_10GBaseR_df/Libero_Project` folder, select the `Libero_Project.prjx` file, and click **Open**.

3. Demo Design (Ask a Question)

The Core10GBaseKR_PHY interfaces XGMII compliant MAC with the 10GBaseKR device for the backplane applications. The IP designed is as per the IEEE 802.3-2012 specification and supports XGMII interface towards (MAC side) and PMA interface to the SerDes side. For the 10GBaseKR applications, the transceiver is used in PMA native mode (32-bit only) and connected to the Ethernet MAC through the PCS interface.

For 10GBASEKR configuration, the Link Training and Auto-Negotiation blocks are enabled, and they are accessed from the 32-bit APB slave interface. The provision to disable the Auto-Negotiation and Link Training is provided through parameter static configuration as part of this IP.

Microchip FPGA board interacts with Vitesse SparX-5i board through SFP interface.

The 10GBASEKR Ethernet design includes the following main components:

- **CORE10GMAC**: Serves as a 10 Gbps Ethernet MAC that transmits and receives the Ethernet packets
- **Transceiver**: Acts as a 10GBASEKR physical interface for data transfers; configured for 64b/66b encoding/decoding with scrambler/descrambler enabled with a PCS interface width of 32 bits to the CORE10GMAC
- **MIV_RV32 (Soft Processor)**: Configures the CORE10G_BASEKR registers
- **PF_TX_PLL**: Generates the bit clock required for the transceiver
- **PF_XCVR_REF_CLK**: Generates the fabric clock and the reference clock for the transceiver and the TX_PLL
- **BaseKRPHY**: Implements BASE-KR functionality

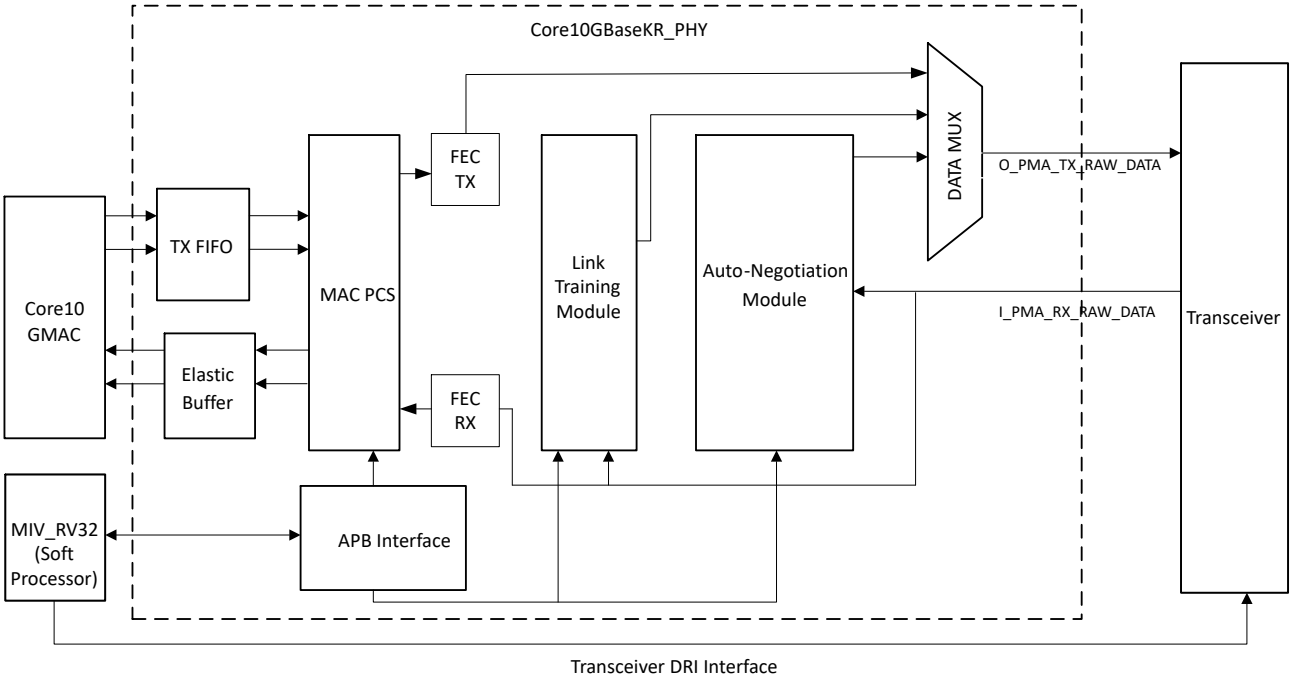
The following table lists the clock frequencies used in the design.

Table 3-1. Hardware Design Clock Frequencies

Clock	Frequency (MHz)
CDR reference clock	156.25
Transceiver bit clock	5156.25
I_SYS_CLOCK	156.25
I_CORE_TX_CLK	322.26
I_CORE_RX_CLK	322.26
PCLK	50

The following figure shows the top-level block diagram of the PolarFire 10GBASEKR hardware implementation.

Figure 3-1. Hardware Implementation Block Diagram



3.1 Design Implementation (Ask a Question)

The following figures show the Libero implementation of the 10GBASEKR Ethernet hardware design.

Figure 3-2. BaseKR TOP

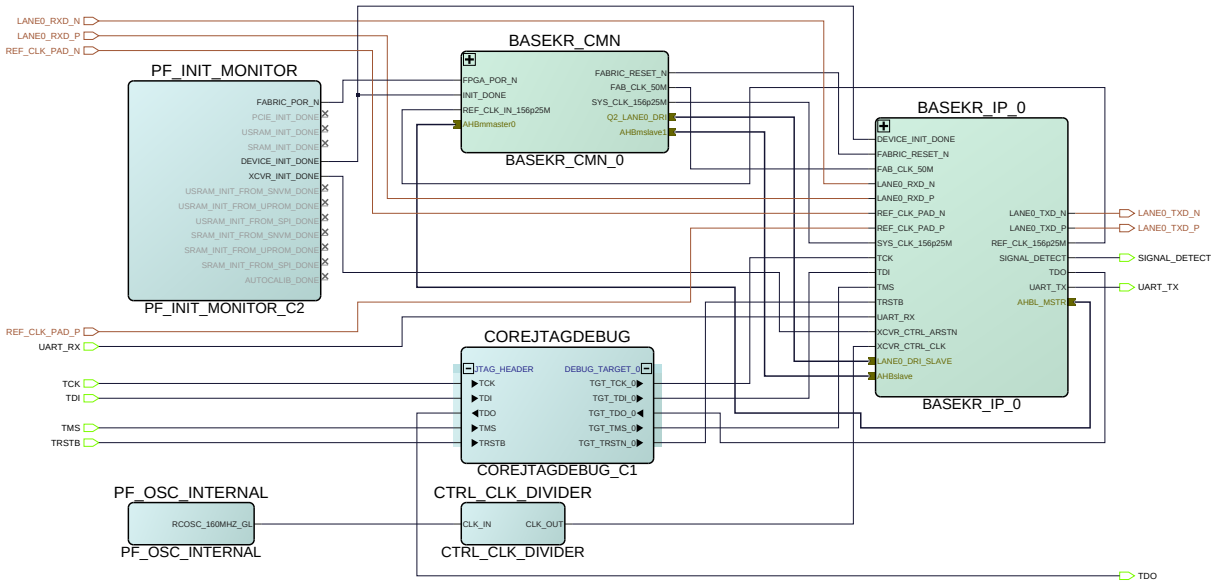


Figure 3-3. BaseKR_CMN_0

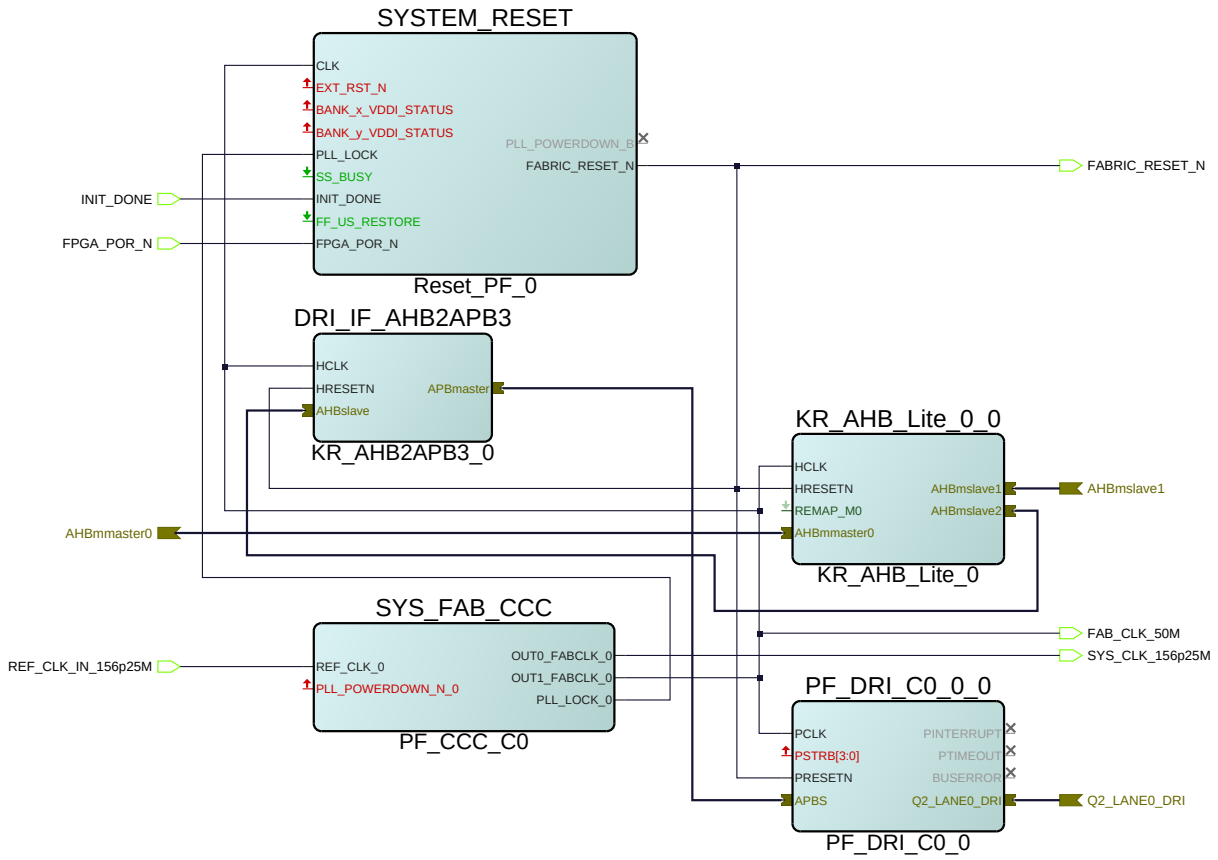
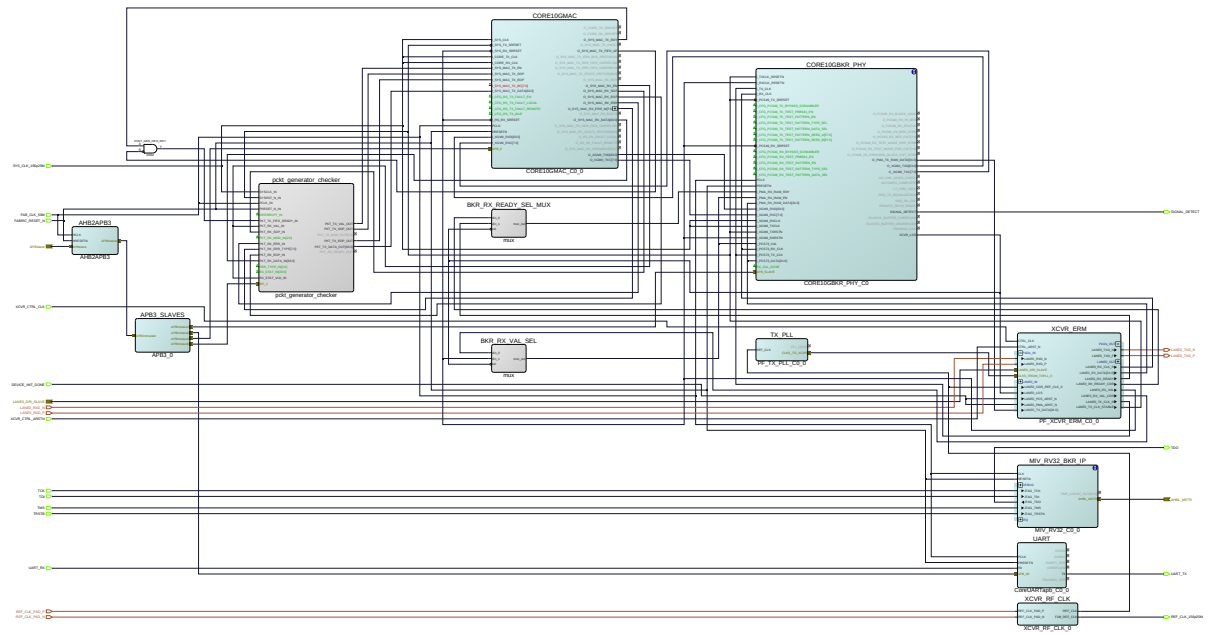


Figure 3-4. BaseKR_IP_0



3.2 Design Blocks and IP Configuration (Ask a Question)

The following IPs are configured before implementing the demo design:

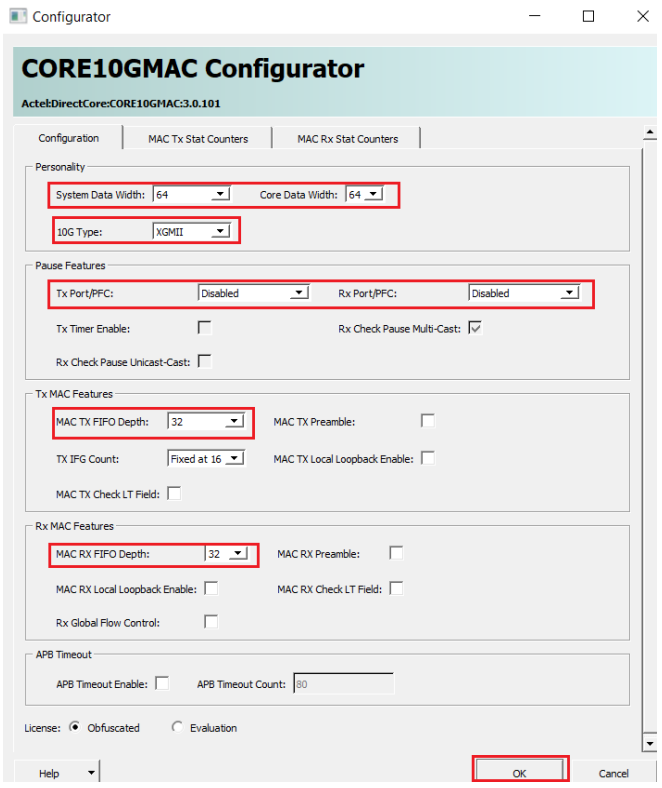
- Core10GMAC
- BaseKR_PHY
- Transceiver Interface
- Transmit PLL
- Transceiver Reference Clock
- MIV_RV32
- CoreAPB3
- PF_POWER_INIT
- PF_CCC_0

3.2.1 Core10GMAC (Ask a Question)

Core10GMAC is configured for XGMII mode with a core data width of 64 bits. Core data width is the width of the data path connected to the BASEKR interface. The system data width, that is, the width of the interface to the user logic, is configured as 64 bits. The Tx and Rx Pause features are disabled, and both the MAC TX FIFO depth and MAC RX FIFO depth are set to 32. The other tab settings are default.

The following figure shows the settings selected in the CORE10GMAC Configurator.

Figure 3-5. CORE10GMAC Configuration

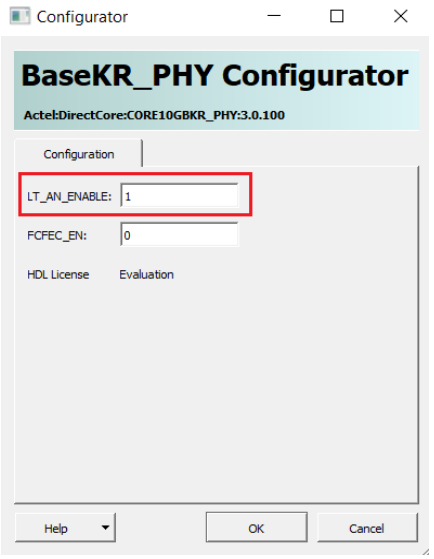


The Core10GMAC IP is configured using the driver which is executed on the MIV_RV32 soft processor. For information about the features and registers of Core10GMAC, see **Libero SoC** > **Catalog** > **Core10GMAC User Guide**.

3.2.2 BaseKR_PHY (Ask a Question)

For 10GBASEKR configuration, the Link Training and Auto-Negotiation blocks are enabled, and they are accessed from the 32-bit APB slave Interface. The provision to disable the Auto-Negotiation and Link Training is provided through parameter static configuration in this IP as shown in the following figure. The PCS encoding is taken care of in this module and XCVR is configured in native PMA mode.

Figure 3-6. BaseKR Configurator

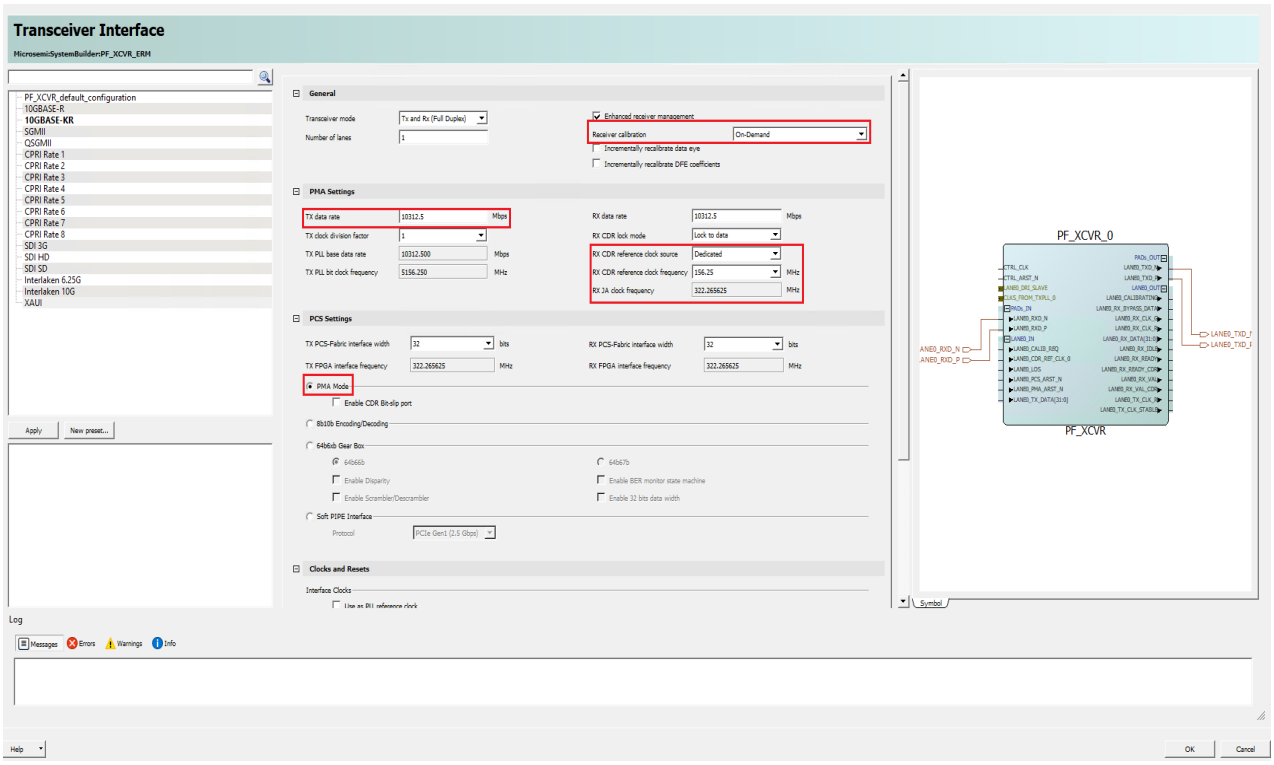


3.2.3 Transceiver Interface (Ask a Question)

The PolarFire high-speed transceiver (PF_XCVR) is a hard IP block and supports data rates ranging from 250 Mbps to 12.5 Gbps. In this demo, PF_XCVR is configured for the data rate of 10312.5 Mbps. It is configured with a CDR reference clock of 156.25 MHz with lock to data selected as the CDR lock mode. The PCS of the transceiver is interfaced with Core10GBaseKR_PHY and it is configured.

The following figure shows the transceiver interface configuration.

Figure 3-7. Transceiver Interface Configuration

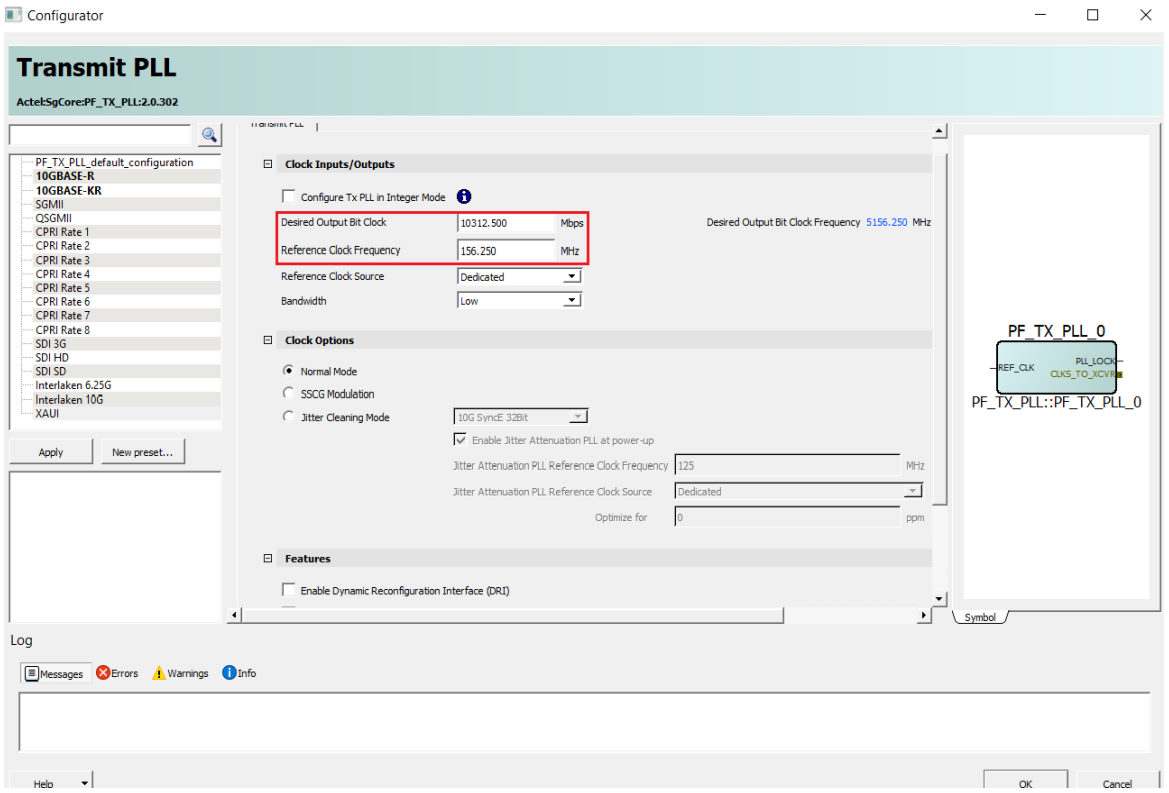


3.2.4 Transmit PLL (Ask a Question)

The PolarFire transmit PLL (PF_TX_PLL) is a hard IP block which provides a bit clock and a reference clock to the transceiver block. The transmit PLL is configured with a reference clock of 156.25 MHz and generates an output clock of 10312.5 Mbps.

The following figure shows the transmit PLL configuration.

Figure 3-8. Transmit PLL Configuration

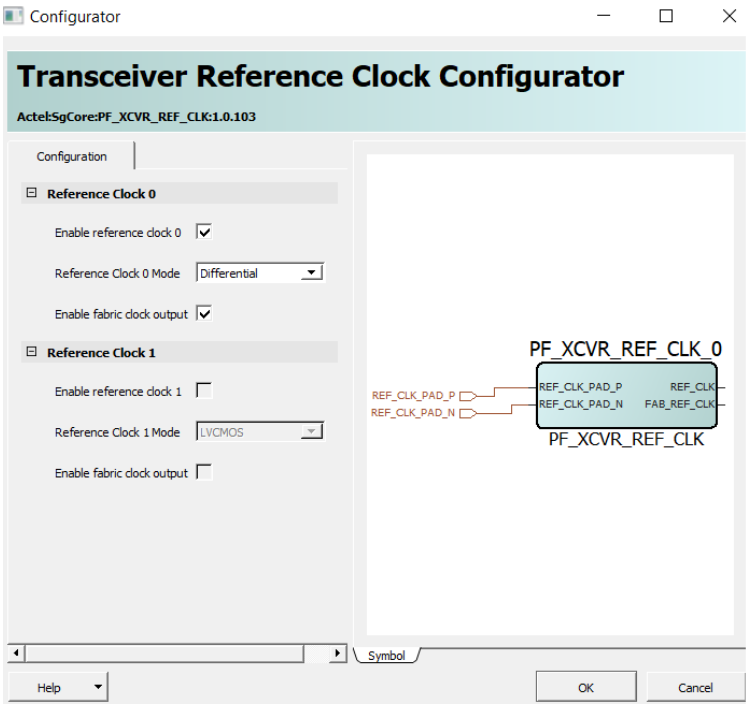


3.2.5 Transceiver Reference Clock (Ask a Question)

The transceiver reference clock (PF_XCVR_REF_CLK) is a hard IP block that provides a reference clock (REF_CLK) of 156.25 MHz to the transmit PLL, and a fabric reference clock (FAB_REF_CLK) which is provided as an input to the Clock Conditioning Circuit (CCC) to generate the PCLK (for configuration) and I_SYS_CLK of the CORE10GMAC.

The following figure shows the transceiver reference clock configuration.

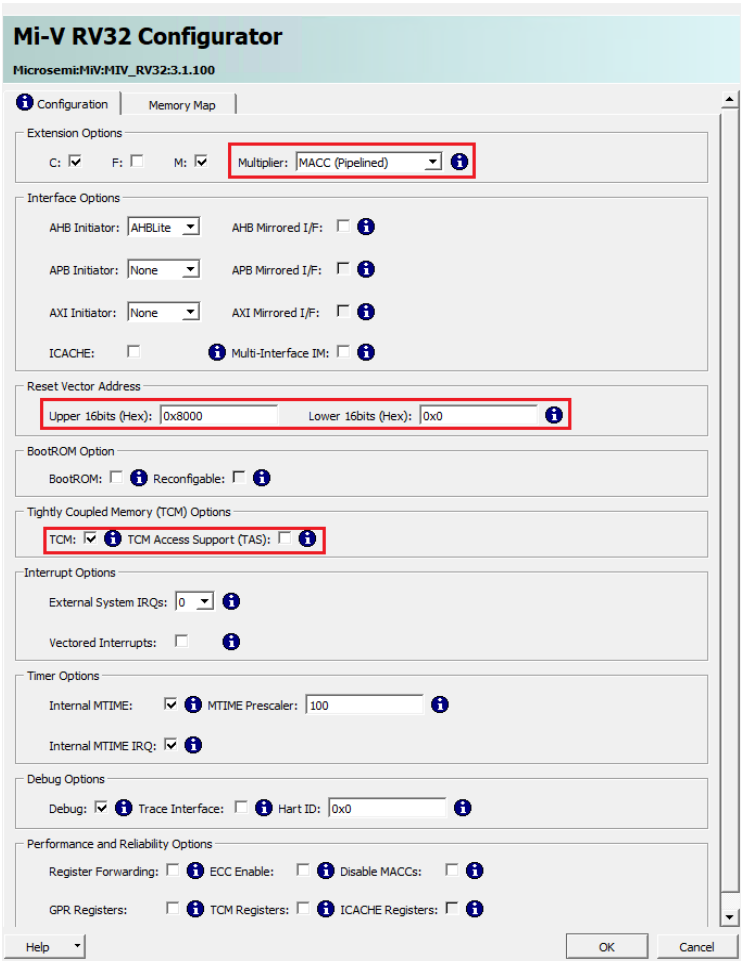
Figure 3-9. Transceiver Reference Clock Configuration



3.2.6 MIV_RV32 (Ask a Question)

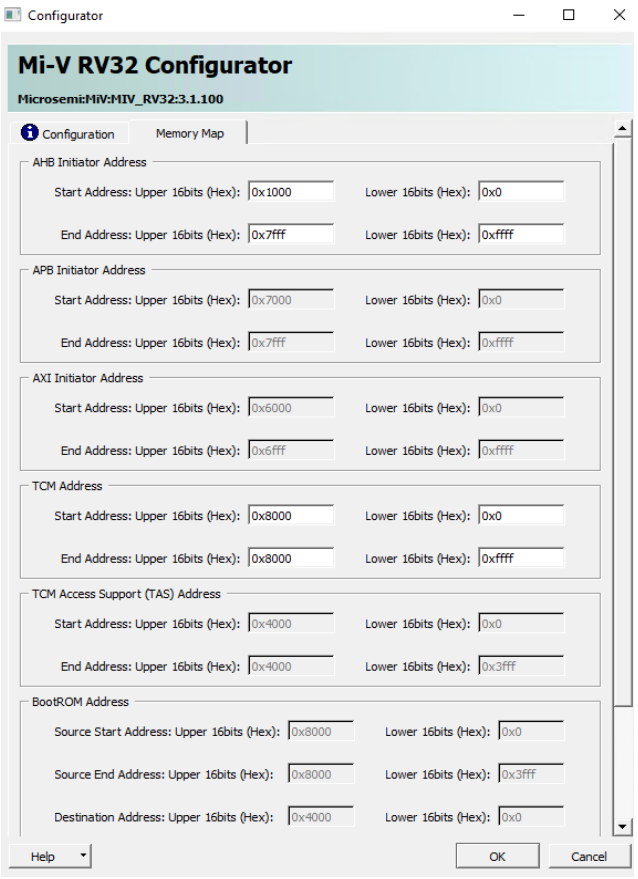
The MIV_RV32 is a processor core designed to implement the RISC-V instruction set for use in Microchip FPGAs. The core includes the industry standard JTAG interface to facilitate debug access. Three optional bus interfaces are available for peripheral and memory accesses: AHB, APB3, and AXI, which is configured as AXI3 or AXI4. This soft processor is responsible for configuring the registers, and the software driver will be running on this processor. In the Configurator window, under the **Configuration** tab, set the following configuration: **Set Reset Vector Address** > **Upper 16bits (Hex) to 0x8000** and retain the default setting for **Lower 16bits (Hex)**, as shown in the following figure. After a reset, the processor will begin executing instructions from this address. TCM RAM is used to load the content of the hex file. For more information about the CoreMi-V, see Mi-V Handbook.

Figure 3-10. MIV_RV32 Configurator



The following figure shows Memory Map tab settings for the MIV_RV32 configurator.

Figure 3-11. MIV_RV32 Configurator (Memory Map Tab Settings)



3.2.7 CoreAHBLite (Ask a Question)

CoreAHBLite implements an Advanced Microcontroller Bus Architecture (AMBA) AHB-Lite bus interconnect fabric. CoreAHBLite provides four initiator interfaces and accommodates up to 16 target interfaces. Each target interface is enabled or disabled for each initiator using the core's configuration Graphical User Interface (GUI).

In this design, a single initiator which is MIV_RV32 processor access two slave slots. These slots addresses are further divided using CoreAPB3.

3.2.8 CoreAPB3 (Ask a Question)

CoreAPB3 is a bus component that provides an AMBA AHB fabric for interconnection between an APB initiator and up to 16 APB targets. CoreAPB3 supports a single APB3 master.

In this design, the CoreAPB3 is connected to the AHB to APB3 converter. On the other end, it serves as the APB master interface, connecting to all other APB slave interfaces.

3.2.9 PF_POWER_INIT (Ask a Question)

The PF_POWER_INIT block ensures the device is powered up, systematically. The process of powering up the device includes three steps:

1. Power-on reset
2. Programmed device boot
3. Design initialization

During design initialization, the transceiver configuration is initialized using the data stored in the non-volatile memory. The output of the PF_POWER_INIT block is ANDed with the resets used in the design to reset the entire logic.

3.2.10 PF_CCC_0 (Ask a Question)

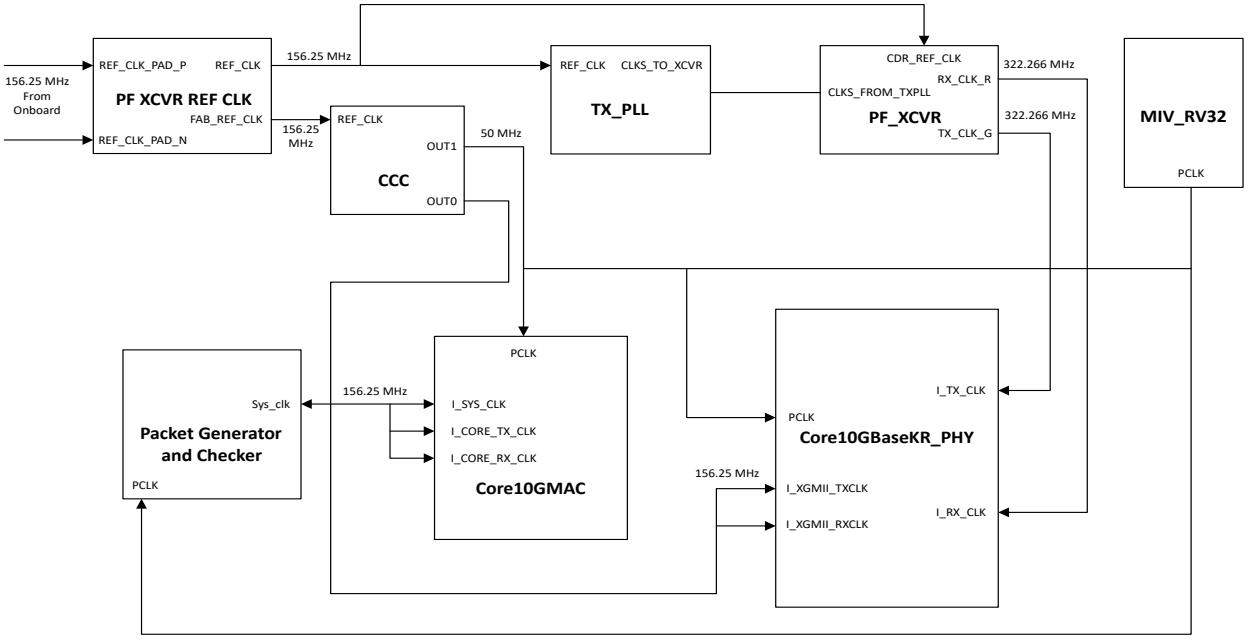
The PolarFire Clock Conditioning Circuitry (CCC) block takes an input clock of 156.25 MHz from the FAB_REF_CLK signal (output of PF_XCVR_REF_CLK) and generates a 50 MHz clock at OUT0 and 156.25 MHz clock at OUT1. The OUT0 port of the CCC is used for the configuration and OUT1 is used for the user logic in the design.

3.3 Clocking Structure (Ask a Question)

- The Clock to the transceiver PF_XCVR is provided by the TX_PLL, the reference clock to the TX_PLL (PF_XCVR_TXPLL, as in block diagram) is sourced from the on-board crystal of 156.25 MHz
- The FAB_REF_CLK is provided as the reference clock to the CCC and the clock of 50 MHz (OUT1) and 156.25 MHz (OUT0) is generated
- The OUT1 is connected as PCLK for Mi-V, Core10GMAC, Core10GBaseKR PHY, and Packet generator and Checker
- The OUT0 clock output of the CCC is connected to Core10GMAC clock inputs, Core10GBaseKR_PHY XGMII clock inputs, and the Packet generator and Checker clock input
- RX_CLK_R is the recovered clock output of the PF_XCVR, and connects to I_RX_CLK and I_PCS73_RX_CLK inputs of Core10GBaseKR_PHY
- TX_CLK_R is the transmit clock output of PF_XCVR, and connects to I_TX_CLK and I_PCS73_TX_CLK inputs of Core10GBaseKR_PHY

The clocking structure of the design is shown in the following figure.

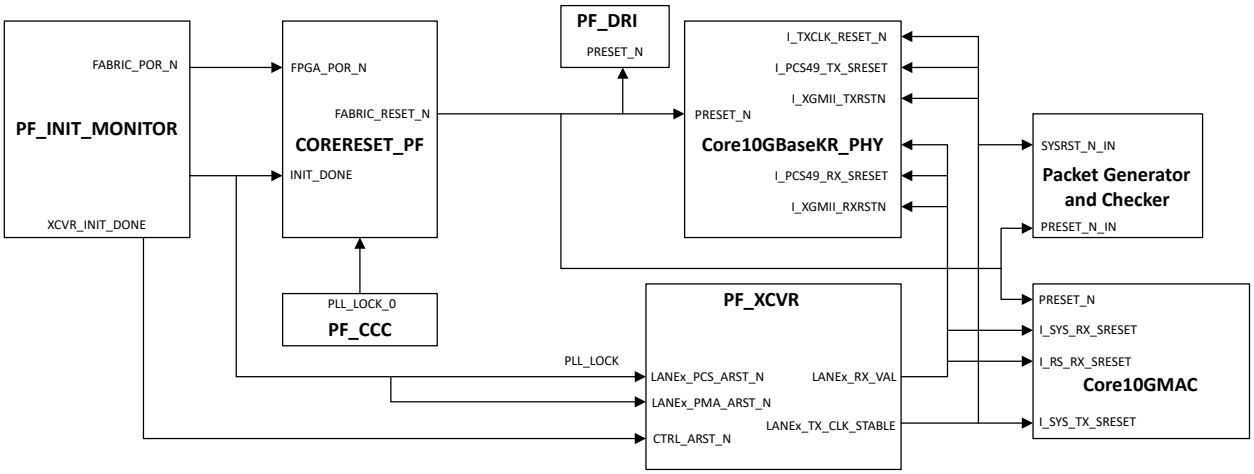
Figure 3-12. Clocking Structure



3.4 Reset Structure (Ask a Question)

The reset structure of the design is shown in following figure. The Reset inputs are synchronized externally with the module clock before connecting to the concerned module.

Figure 3-13. Reset Structure



4. Embedded Software Support (Ask a Question)

The Core10GBaseKR_PHY embedded software driver assists in configuring the Core10GBaseKR_PHY Soft IP and implementing the Auto-Negotiation, and Link Training algorithms. The drive is available on GitHub platform repository. The Core10GBaseKR_PHY IP has a embedded software driver user guide which is available on Github at miv-rv32-documentation repository.

For more information about the recommended sequence and procedure, see Embedded Software Support section of the Core10GBaseKR_PHY Soft IP User Guide.

An embedded software example application is provided as a SoftConsole IDE project, which demonstrates how to use the Core10GbaseKR_PHY embedded software driver along with the PolarFire transceiver, Core10GMAC and a packet generator client. The weblink to the example application on GitHub can be found at the miv-rv32-bare-metal-examples repository.

Important: The job file provided with this application note includes the executable hex file generated using this example project. This executable hex file is attached as a memory client in the FPGA design and runs at the power-up. For detailed information, see 5.5. Configure Design Initialization Data and Memories.

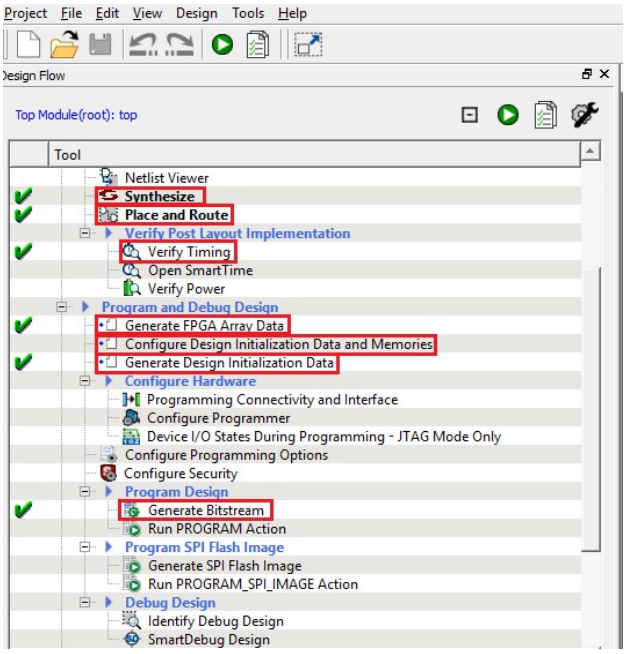
5. Libero Design Flow (Ask a Question)

This section discusses the Libero design flow, which involves the following processes:

- 5.1. Synthesize
- 5.2. Place and Route
- 5.3. Timing Verification
- 5.4. Generate FPGA Array Data
- 5.5. Configure Design Initialization Data and Memories
- 5.6. Generate Bitstream
- 5.7. Run Program Action

The following figure shows these options in the **Design Flow** tab.

Figure 5-1. Libero Design Flow Options



Important: To initialize the TCM in PolarFire using the system controller, a local parameter **l_cfg_hard_tcm0_en**, in the `miv_rv32_subsys_pkg.v` file must be changed to 1'b1 prior to synthesis. See the TCM section in the *MIV_RV32 Handbook*.

5.1 Synthesize (Ask a Question)

To synthesize the design, perform the following steps:

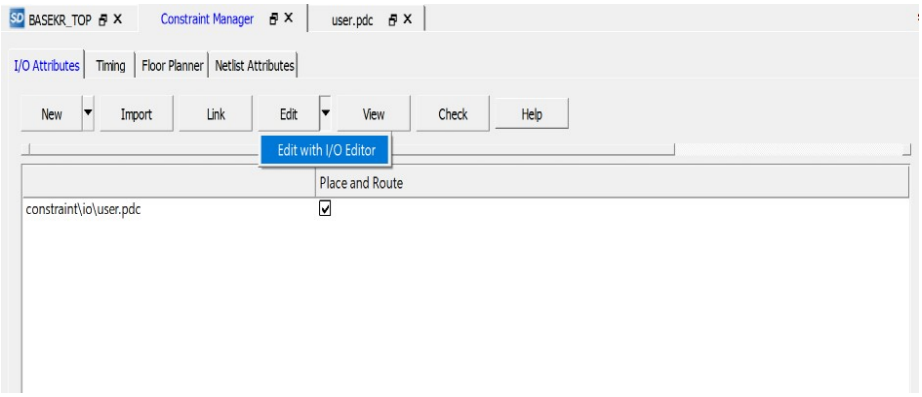
1. On the **Design Flow** window, double-click **Synthesize**. When the synthesis is successful, a green tick mark appears next to **Synthesize**.
2. To view the synthesis report and log files in the **Reports** tab, right-click **Synthesize** and select **View Report**. View the `BASEKR_TOP.srr` for complete details.

5.2 Place and Route (Ask a Question)

To place and route the design, TX_PLL, XCVR_REF_CLK, and PF_XCVR are configured using the I/O Editor. To configure the components and place and route the design, perform the following steps:

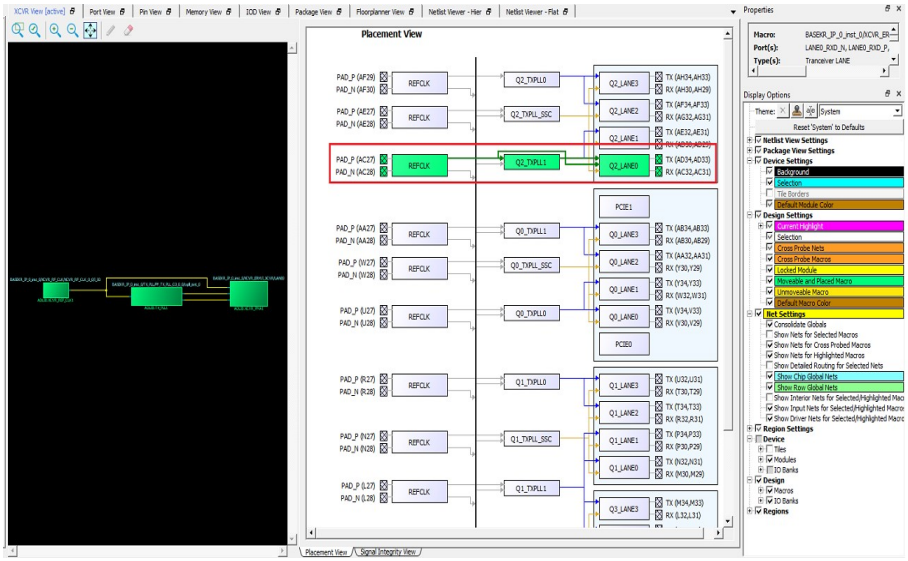
1. On the **Design Flow** window, double-click **Manage Constraints**.
2. On the **I/O Attributes** tab, click **Edit with I/O Editor**, as shown in the following figure.

Figure 5-2. Edit with I/O Editor Option



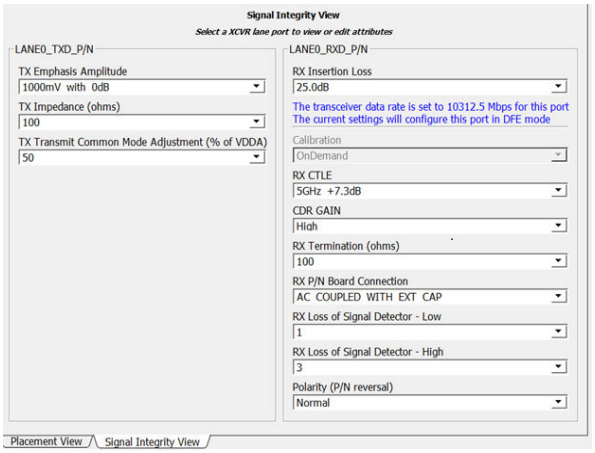
3. Using the **XCVR View** in I/O Editor, place TX_PLL, XCVR_REF_CLK, and PF_XCVR TX as shown in the following figure.

Figure 5-3. I/O Editor Transceiver View



The Signal Integrity View for LANEO_TXD_P/N and LANE0_RX_P/N is shown in the following figure.

Figure 5-4. Signal Integrity View



4. When all the components are placed, the location of the components is updated in the `user_fp.pdc` file (located in **Constraint Manager** > **Floor planner** tab), as shown in the `user_fp.pdc` file.

```
set_location -inst_name BASEKR_IP_0_inst_0/TX_PLL/PF_TX_PLL_C0_0/txpll_inst_0 -fixed true
-x 2460 -y 320
set_location -inst_name BASEKR_IP_0_inst_0/XCVR_ERM/I_XCVR/LANE0 -fixed true -x 2460 -y 317
set_location -inst_name BASEKR_IP_0_inst_0/XCVR_RF_CLK/XCVR_RF_CLK_0_0/I_IO -fixed true -x
2466 -y 317
```

5. On the **Design Flow** window, double-click **Place and Route**. When place and route is successful, a green tick mark appears next to **Place and Route**, as shown in Figure 5-1.
6. Right-click **Place and Route** and select **View Report** to view the place and route report and log files in the **Reports** tab. View the `BASEKR_TOP_place_and_route_constraint_coverage.html` file for place and route constraint coverage.

5.3 Timing Verification (Ask a Question)

To verify timing, perform the following steps:

1. On the **Design Flow** window, double-click **Verify Timing**. When the design meets the timing requirements, a green tick mark appears next to **Verify Timing**, as shown in Figure 5-1.
2. Right-click **Verify Timing** and select **View Report** to view the verify timing report and log files in the **Reports** tab.

5.4 Generate FPGA Array Data (Ask a Question)

To generate FPGA array data, perform the following steps:

1. On the **Design Flow** tab, double-click **Generate FPGA Array Data**
2. When the FPGA array data is generated, a green tick mark appears next to **Generate FPGA Array Data**, as shown in Figure 5-1.

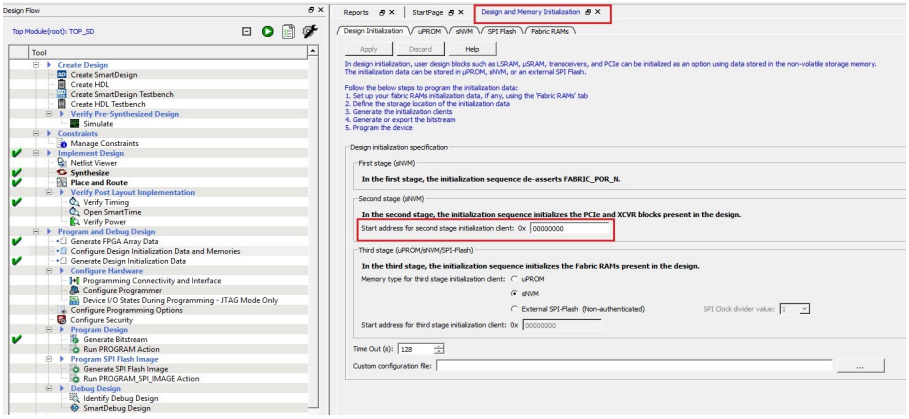
5.5 Configure Design Initialization Data and Memories (Ask a Question)

The **Configure Design Initialization Data and Memories** option creates the non-PCIe transceiver initialization client, which initializes the transceiver block when the PolarFire device powers up.

To create the transceiver initialization client, perform the following steps:

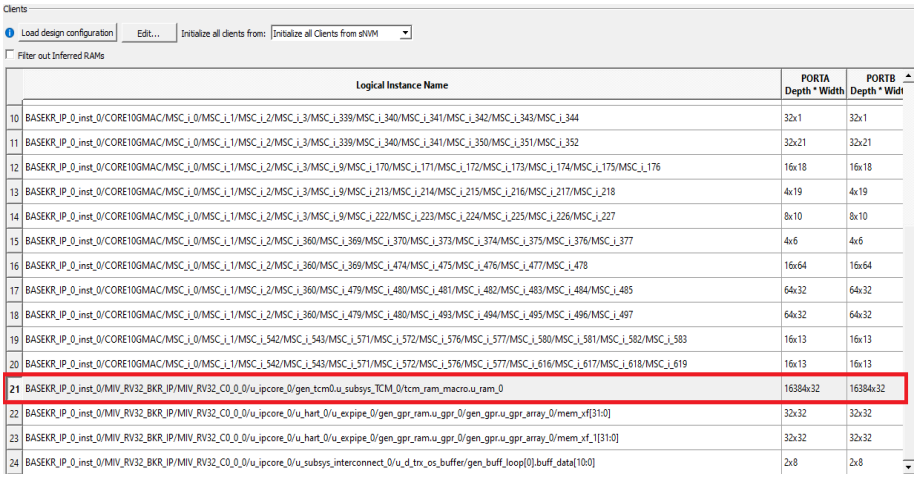
1. On the **Design Flow** window, double-click **Configure Design Initialization Data and Memories**. The **Design and Memory Initialization** window opens, as shown in the following figure.

Figure 5-5. Design and Memory Initialization Window



2. Under **Second stage (sNVM)** pane, enter the start address where the transceiver initialization client must be created in the sNVM, as shown in the preceding figure.
3. The hex file generated from the embedded software example project using the SoftConsole IDE is configured as a memory client. This embedded software application will start executing at the power-on. The Optional Tightly Coupled Memory (TCM) which is available in the MIV_RV32 soft processor is enabled in this design.
4. Under **Fabric RAMs** section, configure the TCM memory with associated hex file. The following figure depicts the same.

Figure 5-6. Fabric RAMs Section



	Logical Instance Name	PORTA Depth * Width	PORTB Depth * Widt
10	BASEKR_IP_0_inst_0/CORE10GMAC/MSC_i_0/MSC_i_1/MSC_i_2/MSC_i_3/MSC_i_339/MSC_i_340/MSC_i_341/MSC_i_342/MSC_i_343/MSC_i_344	32x1	32x1
11	BASEKR_IP_0_inst_0/CORE10GMAC/MSC_i_0/MSC_i_1/MSC_i_2/MSC_i_3/MSC_i_339/MSC_i_340/MSC_i_341/MSC_i_350/MSC_i_351/MSC_i_352	32x21	32x21
12	BASEKR_IP_0_inst_0/CORE10GMAC/MSC_i_0/MSC_i_1/MSC_i_2/MSC_i_3/MSC_i_9/MSC_i_170/MSC_i_171/MSC_i_172/MSC_i_173/MSC_i_174/MSC_i_175/MSC_i_176	16x18	16x18
13	BASEKR_IP_0_inst_0/CORE10GMAC/MSC_i_0/MSC_i_1/MSC_i_2/MSC_i_3/MSC_i_9/MSC_i_213/MSC_i_214/MSC_i_215/MSC_i_216/MSC_i_217/MSC_i_218	4x19	4x19
14	BASEKR_IP_0_inst_0/CORE10GMAC/MSC_i_0/MSC_i_1/MSC_i_2/MSC_i_3/MSC_i_9/MSC_i_222/MSC_i_223/MSC_i_224/MSC_i_225/MSC_i_226/MSC_i_227	8x10	8x10
15	BASEKR_IP_0_inst_0/CORE10GMAC/MSC_i_0/MSC_i_1/MSC_i_2/MSC_i_360/MSC_i_369/MSC_i_370/MSC_i_373/MSC_i_374/MSC_i_375/MSC_i_376/MSC_i_377	4x6	4x6
16	BASEKR_IP_0_inst_0/CORE10GMAC/MSC_i_0/MSC_i_1/MSC_i_2/MSC_i_360/MSC_i_369/MSC_i_474/MSC_i_475/MSC_i_476/MSC_i_477/MSC_i_478	16x64	16x64
17	BASEKR_IP_0_inst_0/CORE10GMAC/MSC_i_0/MSC_i_1/MSC_i_2/MSC_i_360/MSC_i_479/MSC_i_480/MSC_i_481/MSC_i_482/MSC_i_483/MSC_i_484/MSC_i_485	64x32	64x32
18	BASEKR_IP_0_inst_0/CORE10GMAC/MSC_i_0/MSC_i_1/MSC_i_2/MSC_i_360/MSC_i_479/MSC_i_480/MSC_i_493/MSC_i_494/MSC_i_495/MSC_i_496/MSC_i_497	64x32	64x32
19	BASEKR_IP_0_inst_0/CORE10GMAC/MSC_i_0/MSC_i_1/MSC_i_542/MSC_i_543/MSC_i_571/MSC_i_572/MSC_i_576/MSC_i_577/MSC_i_580/MSC_i_581/MSC_i_582/MSC_i_583	16x13	16x13
20	BASEKR_IP_0_inst_0/CORE10GMAC/MSC_i_0/MSC_i_1/MSC_i_542/MSC_i_543/MSC_i_571/MSC_i_572/MSC_i_576/MSC_i_577/MSC_i_616/MSC_i_617/MSC_i_618/MSC_i_619	16x13	16x13
21	BASEKR_IP_0_inst_0/MIV_RV32_BKR_IP/MIV_RV32_C0_0_0/u_ipcore_0/gen_tcm0.u_subsys_TCM_0/tcm_ram_macro.u_ram_0	16384x32	16384x32
22	BASEKR_IP_0_inst_0/MIV_RV32_BKR_IP/MIV_RV32_C0_0_0/u_ipcore_0/u_hart_0/u_expipe_0/gen_gpr_ram.u_gpr_0/gen_gpr.u_gpr_array_0/mem_xf[31:0]	32x32	32x32
23	BASEKR_IP_0_inst_0/MIV_RV32_BKR_IP/MIV_RV32_C0_0_0/u_ipcore_0/u_hart_0/u_expipe_0/gen_gpr_ram.u_gpr_0/gen_gpr.u_gpr_array_0/mem_xf_1[31:0]	32x32	32x32
24	BASEKR_IP_0_inst_0/MIV_RV32_BKR_IP/MIV_RV32_C0_0_0/u_ipcore_0/u_subsys_interconnect_0/u_d_trx_os_buffer/gen_buff_loop[0].buff_data[10:0]	2x8	2x8

5. On the **Design Flow** window, double-click on **Generate Design Initialization Data** to generate the initialization client. When the initialization client is generated, a green tick mark appears next to **Generate Design Initialization Data**, as shown in Figure 5-1.

5.6 Generate Bitstream (Ask a Question)

To generate the bitstream, perform the following steps:

1. On the **Design Flow** tab, double-click **Generate Bitstream**.
2. When the bitstream is successfully generated, a green tick mark appears next to **Generate Bitstream**, as shown in Figure 5-1.
3. Right-click **Generate Bitstream** and select **View Report** to view the corresponding log file in the **Reports** tab.

5.7 Run Program Action (Ask a Question)

Program the PolarFire device with the bitstream which was generated in the previous step. To program the PolarFire device, perform the following steps:

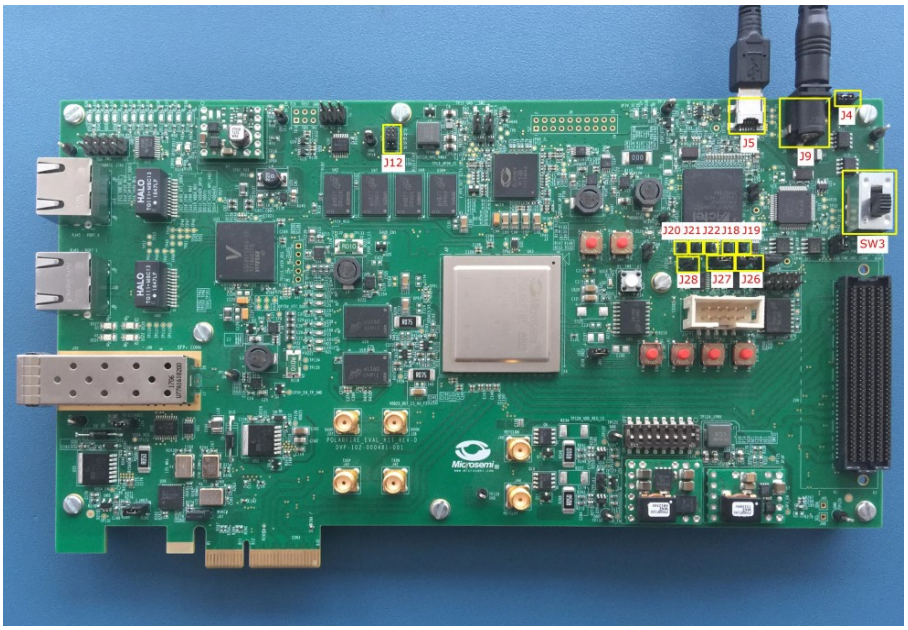
1. Ensure that the jumper settings on the board are listed in the following table.

Table 5-1. Jumper Settings for PolarFire Device Programming

Jumper	Description
J18, J19, J20, J21, and J22	Short pin 2 and 3 for programming the PolarFire® FPGA through FTDI
J28	Short pin 1 and 2 for programming through the on-board FlashPro Express
J26, J27	Short pin 1 and 2 for programming through the FTDI SPI
J39	Short pin 1 and 2 for enabling the Tx
J4	Short pin 1 and 2 for manual power switching using SW3

2. Connect the power supply cable to the J9 connector on the board.
3. Connect the host PC to the J5 connector (FTDI port) on the board using a USB cable.
4. Power on the board using the SW3 slide switch.
   The following figure shows the PolarFire Evaluation Board setup for programming the device and running the reference design.

Figure 5-7. PolarFire Evaluation Board Setup



5. Double-click **Run PROGRAM Action** from the **Libero** > **Design Flow** tab. When the device is successfully programmed, a green tick mark appears next to **Run PROGRAM Action**.

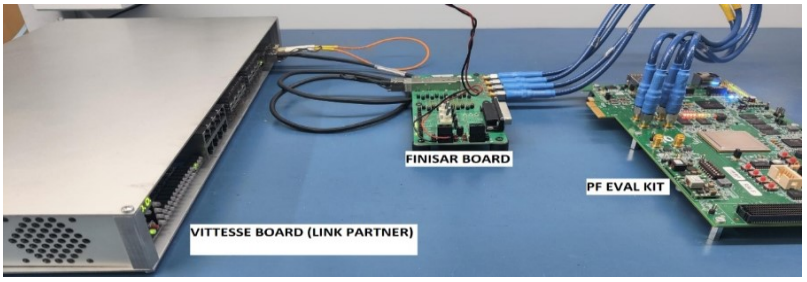
6. Running the Demo (Ask a Question)

This demo design runs with inter-op device and using two PolarFire evaluation boards.

6.1 10GBASEKR Demo using Vitesse Link Partner and PolarFire Evaluation Board (Ask a Question)

The following figure shows the hardware setup.

Figure 6-1. Inter-op Setup of Vitesse LP and PolarFire Eval Board



Follow these steps to run the PolarFire 10GBASEKR loopback hardware demo design on the PolarFire Evaluation Board.

1. Insert the copper cable to Finisar board using SFP module and connect the other end to Link Partner (LP)
2. Connect the SMA cables from the PolarFire board to Finisar board as listed:
   a. J41 (TXP of PolarFire) -> TXP of Finisar SFP+ -> Copper cable -> Port 1 of VSC SparX-5i
   b. J42 (TXN of PolarFire) -> TXN of Finisar SFP+ -> Copper cable -> Port 1 of VSC SparX-5i
   c. J37 (RXP of PolarFire) -> RXP of Finisar SFP+ -> Copper cable -> Port 1 of VSC SparX-5i
   d. J38 (RXN of PolarFire) -> RXN of Finisar SFP+ -> Copper cable -> Port 1 of VSC SparX-5i
   Using optical fiber cable loop back from port 1 to port 2. (In this demo, it is Port //1/2.)
3. Connect the USB to serial converter cable from Link partner to host PC
4. Open the associated serial terminal of LP and PolarFire board to control and monitor the status
5. Program the PolarFire board with the job file
6. Configure the Link Partner to support in 10GBASEKR mode. Refer to the Link Partner user manual for the commands.
7. Enter the following commands:

```
Terminal in Link Partner
# show interface 10GigabitEthernet 1/1 status details clause-73
10GigabitEthernet 1/1:
Configuration
  Desription:
  Mode:                     Enabled
  Speed/Duplex:             Forced Clause 73
  Media-type:               SFP
  Flowcontrol:              Off
  Priority-based F/C:
  Max. Frame:               10240 bytes
  Excessive Collision:      Discard
  Frame Length Check:       Disabled
  FEC Mode:                 Auto
Status:
  Aneg:                     Yes (C173)
  Link:                     10Gfdx
  Operational Warnings:     None
  FEC Mode:                 None
  SFP Family:               10G DAC
  SFP Vendor Name:          CISCO
  SFP Vendor P/N:           SPT-SFP+C1
  SFP Vendor S/N:           201110127104
  SFP Vendor Revision:      N
  SFP Date Code:            11101200
  SFP Transceiver:          10GBASEKR
Clause 73 Aneg Status:
  Completed:                Yes
  Time since start:         24 seconds
  Training complete:        Yes
  Training time:            2347 ms
   CM OB tap (7-bit signed): -2 (126)
   CP OB tap (7-bit signed): -3 (125)
   C0 OB tap (7-bit signed): +22 (22)
```

Once Auto-Negotiation and Link Training is done, the link is considered as established. The status of the link is observed in the terminal console of the Link Partner and in the UART terminal connected to PolarFire Evaluation Kit.

```
Terminal in PolarFire Evaluation board
*** Core10GBaseKR PHY ***
Starting Auto-Negotiation!!
LT Link Established!!
Link: Good!!
Packet Testing:
         Total packets (msb): 0
         Total packets (lsb): 42745121
         Good packets (msb):  0
         Good packets (lsb):  42745105
         Bad packets (msb):   0
         Bad packets (lsb):   0
```

Traffic Test

Continuous traffic is sent from the PolarFire Evaluation Kit to the Link Partner. The Link Partner then loops back the same data and sends it back to the PolarFire Evaluation Kit. The following command shows the LP data statistics.

```
 # show interface 10GigabitEthernet 1/1 statistics:
10GigabitEthernet 1/4 Statistics:
Rx Packets:              253434502 Tx Packets:              253434502
Rx Octets:               65892970520           Tx Octets:               65892970520
Rx Unicast:              253434502             Tx Unicast:              253434502
Rx Multicast:            0                     Tx Multicast:            0
Rx Broadcast:            0                     Tx Broadcast:            0
Rx Pause:                0                     Tx Pause:                0

Rx 64:                   0                     Tx 64:                   0
Rx 65-127:               0                     Tx 65-127:               0
Rx 128-255:              0                     Tx 128-255:              0
Rx 256-511:              253434502             Tx 256-511:              253434502
Rx 512-1023:             0                     Tx 512-1023:             0
Rx 1024-1518:            0                     Tx 1024-1518:            0
Rx 1519-    :            0                     Tx 1519-    :            0

Rx Priority 0:           253434502             Tx Priority 0:           253434502
Rx Priority 1:           0                     Tx Priority 1:           0
Rx Priority 2:           0                     Tx Priority 2:           0
Rx Priority 3:           0                     Tx Priority 3:           0
Rx Priority 4:           0                     Tx Priority 4:           0
Rx Priority 5:           0                     Tx Priority 5:           0
Rx Priority 6:           0                     Tx Priority 6:           0
Rx Priority 7:           0                     Tx Priority 7:           0

Rx Drops:                0                     Tx Drops:                0
Rx CRC/Alignment:        0                     Tx Late/Exc. Coll.:      0
Rx Undersize:            0
Rx Oversize:             0
Rx Fragments:            0
```

Important: In the preceding data statistics generated by the PolarFire Evaluation board, the text in:

Orange	Represents the *Received packets from PolarFire Evaluation Kit*
Blue	Represents the *Looped back packets from the Vitesse LP*

The following command shows the PolarFire Evaluation board data statistics.

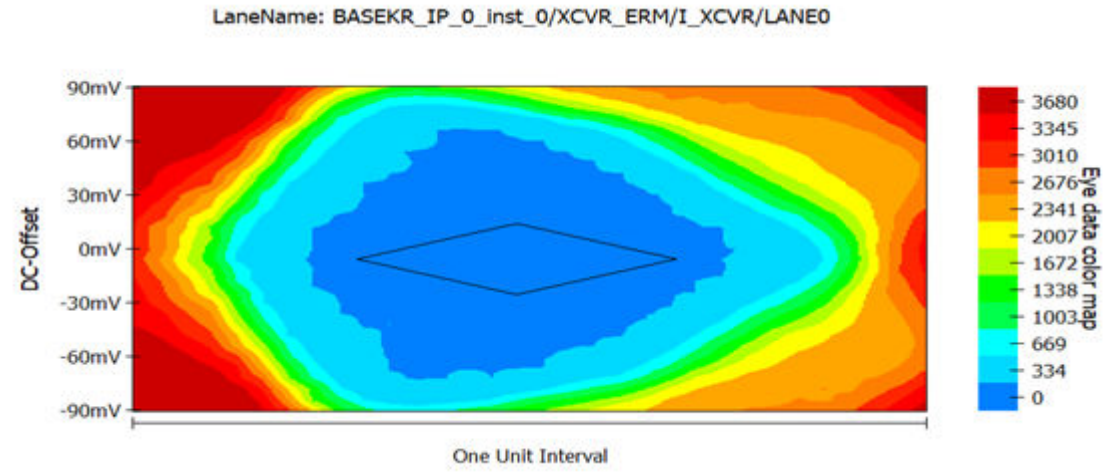
```
*** Core10GBaseKR PHY ***

Starting Auto-Negotiation!!
LT Link Established!! Link: Good!!
Packet testing:
     Total packets (msb):  0
     Total packets (lsb):  253434502
     Good packets (msb):   0
     Good packets (lsb):   253434502
     Bad packets (msb):    0
     Bad packets (lsb):    0
```

Important: In the preceding data statistics generated by the PolarFire Evaluation board, the text in:

Orange	Represents the *Transmitted packets from PolarFire Evaluation Kit*
Blue	Represents the *Received packets from the Vitesse LP*

The following figure shows the Eye diagram with LP.

Figure 6-2. Eye Diagram with LP



Break Link Test

The test is performed by pulling the Copper cable connected between PolarFire Evaluation board and Vitesse LP. In this case, the link will be lost. Once the cable is connected back, observe that the link is re-established.

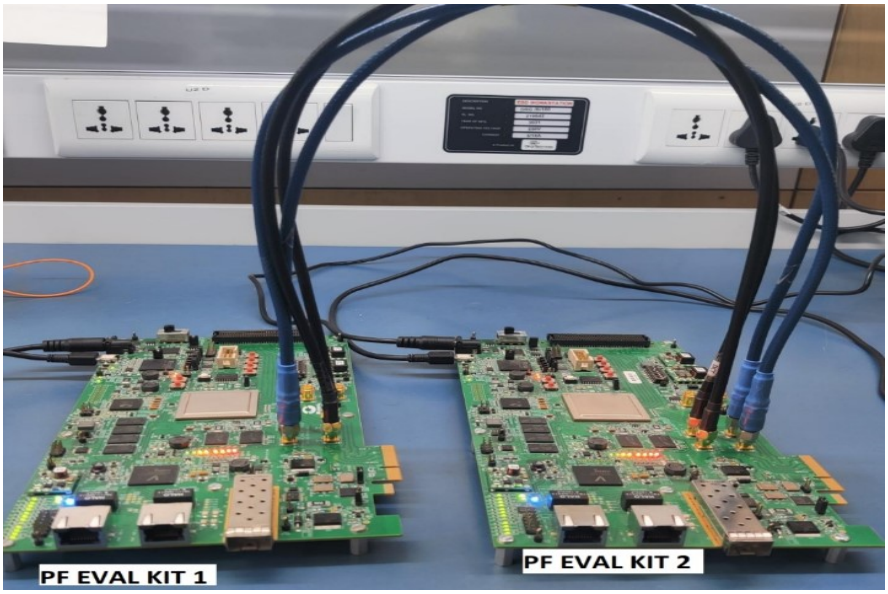
The following command shows the break link results.

```
Link: Broken!!
Starting Auto-Negotiation!!
LT Link Established!! Link: Good!!
Packet Testing:
     Total packets (msb):  0
     Total packets (lsb):  167147494
     Good packets (msb):   0
     Good packets (lsb):   122898839
     Bad packets (msb):    0
```

6.2 10GBASEKR Demo using Two PolarFire Evaluation Boards (Ask a Question)

The following figure shows the setup of two PolarFire Evaluation boards with short reach.

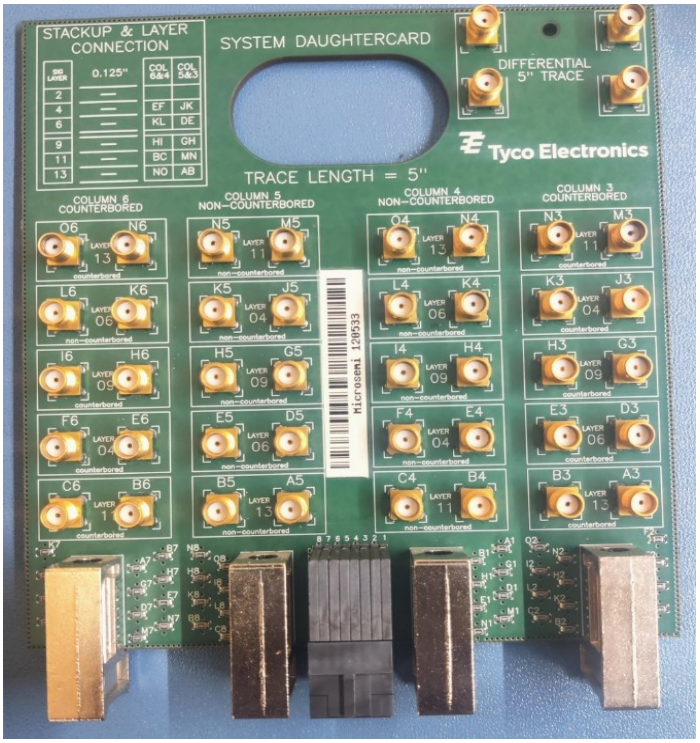
Figure 6-3. Short Reach Connection between Two PolarFire Evaluation Boards



The boards which are used in backplane setup are shown in following figure.

Figure 6-4. Backplane

Figure 6-5. Daughter Board



By using a backplane setup with varying channel lengths, the induced loss can be adjusted. The following tables list the loss associated with the channel length.

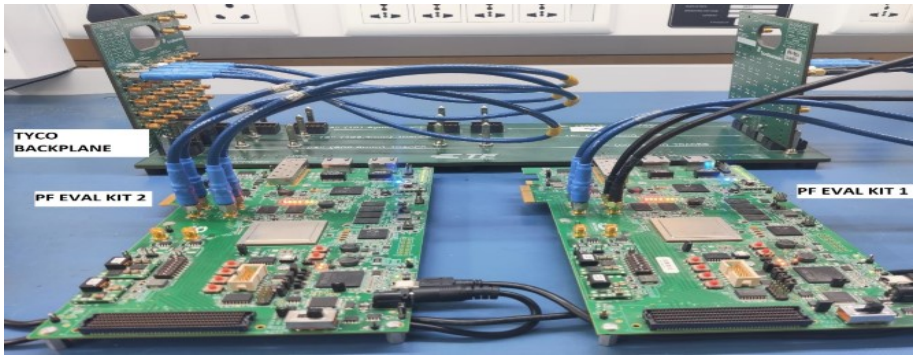
Important: The daughter cards connected at both ends of the backplane has loss of 5 dB each. Hence, the total loss induced by the daughter cards is 10 dB.

Table 6-1. Recommended Settings for Different Loss

Reach	Channel Loss (in dB)	CTLE	Tx Emphasis	RX Insertion Loss
Short	4	5GHz+7.3 dB	1000 mv+ 0 dB	25 dB
Medium	18			
Long	24			

The setup with two PolarFire boards, connected with a 16-inch backplane, is shown in the following figure.

Figure 6-6. Two PolarFire Evaluation Boards with Backplane



To setup the two PolarFire boards with backplane, perform the following steps:

1. Connect two PolarFire Evaluation boards using SMA cables for short reach as listed. The following connections must be followed while using the backplane.
   - Connect J41 (TXP) of PolarFire Evaluation board 1 to F6 connector of daughter card 1 of Backplane. At the other end, the F6 connector from daughter card 2 of backplane must be connected to J37(RXP) of PolarFire Evaluation board 2.
   - Connect J42 (TXN) of PolarFire Evaluation board 1 to E6 connector of daughter card 1 of Backplane. At the other end, the E6 connector from daughter card 2 of backplane must be connected to J38(RXN) of PolarFire Evaluation board 2.
   - Connect J37 (RXP) of PolarFire Evaluation board 1 to O6 connector of daughter card 1 of Backplane. At the other end, the O6 connector from daughter card 2 of backplane must be connected to J41(TXP) of PolarFire Evaluation board 2.
   - Connect J38 (RXN) of PolarFire Evaluation board 1 to N6 connector of daughter card 1 of Backplane. At the other end, the N6 connector from daughter card 2 of backplane must be connected to J42(TXN) of PolarFire Evaluation board 2.
2. Ensure that the preceding listed connections are made while using the backplane
3. Connect the 12V DC power supply and USB serial connector to PolarFire Evaluation boards
4. Open the associated serial terminals of two PolarFire boards to control and monitor the status
5. Program the PolarFire boards with the job file

Link Status

Once the Auto-Negotiation and Link Training is done, the link is established. The status of the link is observed using LED11 (H21), glowing of this LED indicates the Link Training completion and prints are seen in the UART terminal connected to PolarFire Evaluation Kit.

The following command shows the terminal status in PolarFire Evaluation board 1.

```
*** Core10GBaseKR PHY ***

Starting Auto-Negotiation!!
LT Link Established!!
Link: Good!!
Packet testing:
     Total packets (msb):  0
     Total packets (lsb):  42744986
     Good packets (msb):   0
     Good packets (lsb):   42744775
     Bad packets (msb):    0
     Bad packets (lsb):    0
```

The following command shows the terminal status in PolarFire Evaluation board 2.

```
*** Core10GBaseKR PHY ***

Starting Auto-Negotiation!!
LT Link Established!!
Link: Good!!
Packet testing:
     Total packets (msb):  0
     Total packets (lsb):  42745001
     Good packets (msb):   0
     Good packets (lsb):   42745578
     Bad packets (msb):    0
     Bad packets (lsb):    0
```

Break Link Test

The test is performed by turning off one of the PolarFire Evaluation Kits. In this case, PolarFire Evaluation Kit 1 is off. It was observed that the link is broken in PolarFire Evaluation Kit 2, which is on. After turning on the power of the PolarFire Evaluation Kit 1, the link re-establishes. This is observed in the UART terminal of PolarFire Evaluation Kit 2, as shown in the command.

```
Link: Broken!!
Starting Auto-Negotiation!!
LT Link Established!!
Link: Good!!
Packet Testing:
     Total packets (msb):  0
     Total packets (lsb):  167147494
     Good packets (msb):   0
     Good packets (lsb):   122898839
     Bad packets (msb):    0
```

Traffic Test with Two PolarFire Evaluation Kits

To perform the traffic test with two PolarFire Evaluation Kits, perform the following steps:

1. Traffic is sent continuously between two PolarFire Evaluation Kits. The data statistics of PolarFire Evaluation Kit 1 and PolarFire Evaluation Kit 2 are shown in the following command terminals.
2. From the following command terminals, we can observe that the Transmitted packet count matches with Received packet count in PolarFire Evaluation Kit 1 and vice-versa.
3. No errors are observed in the received packets (No bad packets).
4. Eye diagram is captured in two kits using the Smart Debug tool to observe eye opening which is shown in the following eye diagram figures.

Important: To stop the packet transmission, open **Smart Debug** tool, go to **pckt_generator module**, and assert the stop bit.

The following command shows the PolarFire Evaluation Kit 1 board data statistics.

```
Link: Good!!
Packet testing:
     Total packets (msb):  0
     Total packets (lsb):  1117149554
     Good packets (msb):   0
     Good packets (lsb):   1065094727
     Bad packets (msb):    0
     Bad packets (lsb):    0
```

Important: In the preceding data statistics generated by the PolarFire Evaluation board, the text in:

Orange	Represents the *Transmitted Packet count*
Blue	Represents the *Received Packet count*

The following command shows the PolarFire Evaluation Kit 2 board data statistics.

```
Link: Good!!
Packet testing:
     Total packets (msb):  0
     Total packets (lsb):  1065094727
     Good packets (msb):   0
     Good packets (lsb):   1117149554
     Bad packets (msb):    0
     Bad packets (lsb):    0
```

Important: In the preceding data statistics generated by the PolarFire Evaluation board, the text in:

Orange	Represents the *Transmitted Packet count*
Blue	Represents the *Received Packet count*

Transmitted packet count of PolarFire 1 board matches with Received packet count of PolarFire 2 board and vice-versa. With these statistics, it is confirmed that there is no packet loss during transmission with two PolarFire Evaluation boards connected to each other. The same behavior is observed with 6.5 dB, 17 dB, and 25 dB loss. These loss values are calculated based on channel lengths.

The following eye diagrams depict the packet transmission with different channel losses.

Figure 6-7. Eye Diagram with 6.5 dB Loss

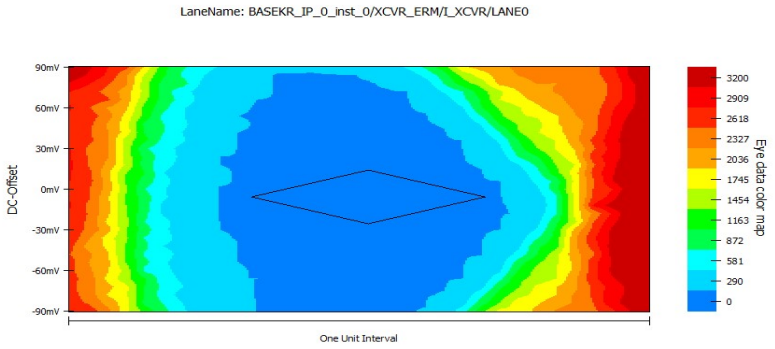


Figure 6-8. Eye Diagram with 17 dB Loss

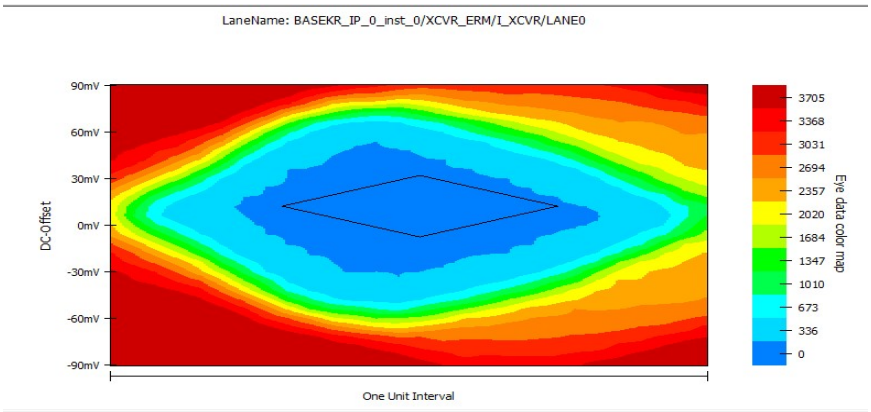
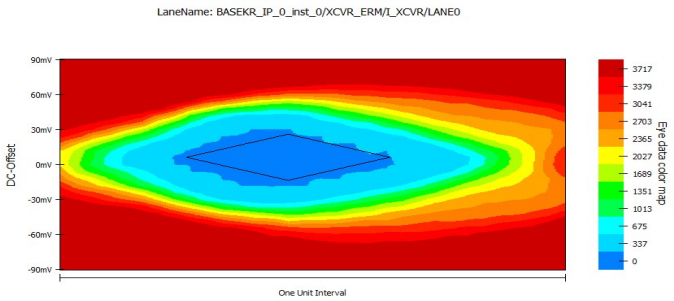


Figure 6-9. Eye Diagram with 25 dB Loss



7. Appendix 1: Programming the Device Using FlashPro Express (Ask a Question)

This section discusses how to program the PolarFire device with the Job programming file using a FlashPro programmer.

The default location of the Job file is located at the following location:
`mpf_an5069_v2023p1_df\Programming_Files\BASEKR_TOP.job`

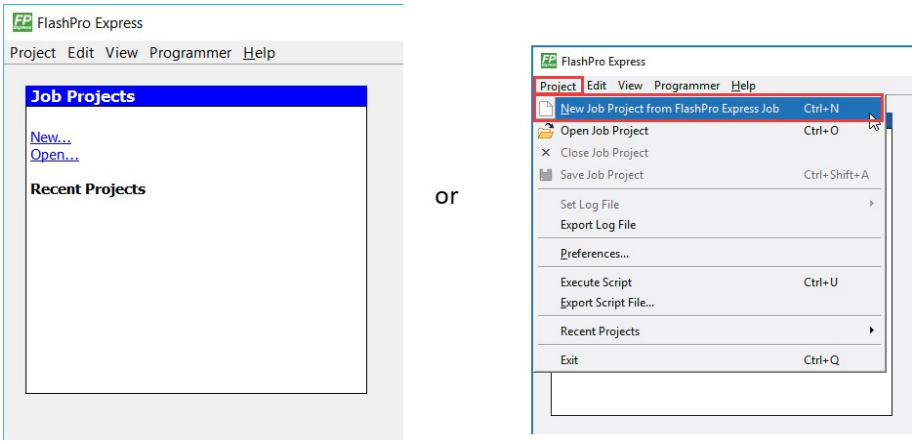
To program the PolarFire device using FlashPro Express, perform the following steps:

1. Ensure that the jumper settings on the board are the same as listed in Table 5-1

> **Important:** The power supply switch must be switched off while making the jumper connections.

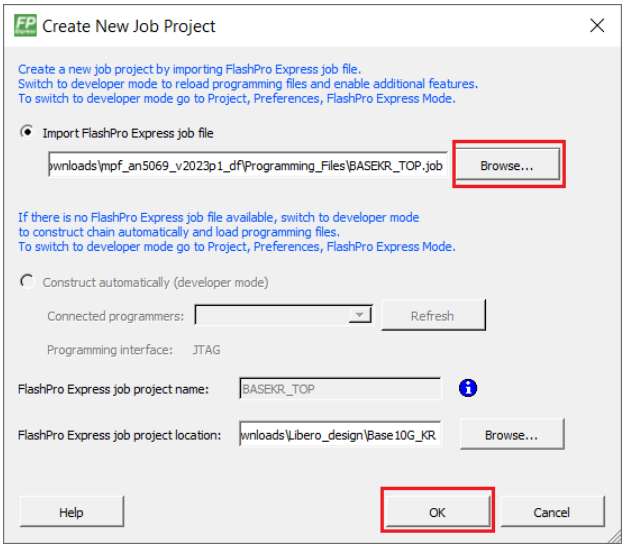
2. Connect the power supply cable to the **J9** connector on the board
3. Connect the USB cable from the Host PC to the **J5** (FTDI port) on the board
4. Power on the board using the SW3 slide switch
5. On the host PC, launch the **FlashPro Express** software
6. To create a new job project, click **New** or in the **Project** menu, select **New Job Project from FlashPro Express Job**, as shown in the following figure

Figure 7-1. FlashPro Express Job Project



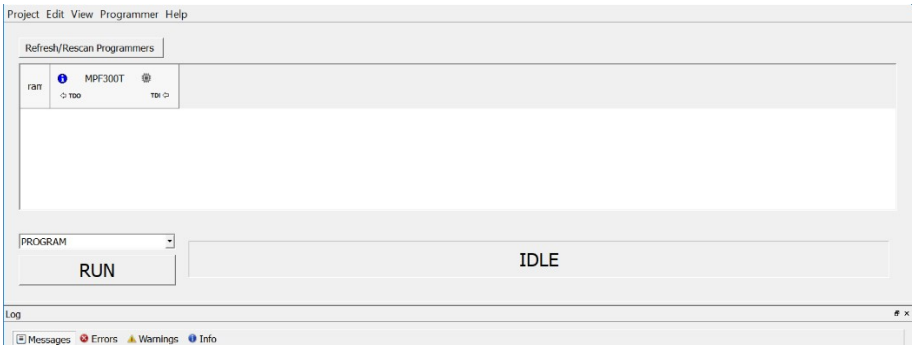
7. Enter the following in the New Job Project from FlashPro Express Job dialog box as shown in the following figure:
   - **Programming job file**: Click **Browse**, and navigate to the location where the .job file is located and select the file. The default location is `<download_folder>\mpf_an5069_v2023p1_df\Programming_Files` and `<download_folder>mpf_an5069_v2023p1_df\Programming_Files`
   - **FlashPro Express job project location**: Click **Browse** and navigate to the location where you want to save the project

Figure 7-2. New Job Project from FlashPro Express Job



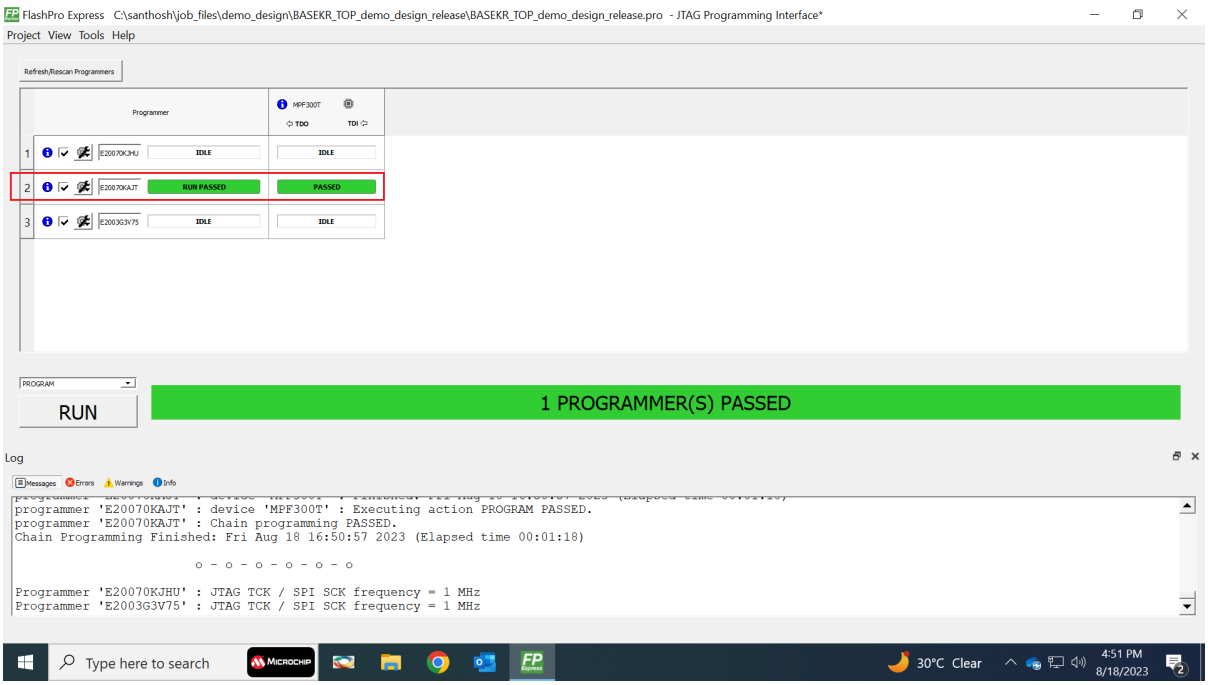
8. Click **OK**. The required programming file is selected and ready to be programmed in the device
9. The FlashPro Express window appears, as shown in the following figure. Confirm that a programmer number appears in the Programmer field. If it does not, confirm the board connections and click **Refresh/Rescan Programmers**.

Figure 7-3. Programming the Device



10. Click **RUN**. When the device is programmed successfully, a RUN PASSED status is displayed as shown in the following figure.

Figure 7-4. FlashPro Express—RUN PASSED



11. Close **FlashPro Express** or in the **Project** tab, click **Exit**.

8. References (Ask a Question)

This section lists documents that provide more information about the concepts and features covered in this application note:

- For more information about 10G Ethernet, see IEEE 802.3 standard in the IEEE website.
- For more information about PolarFire transceiver blocks, see UG0677:PolarFire FPGA Transceiver User Guide.
- For more information about the Core10GMAC and Core10GBaseKR_PHY, see Core10GMAC User Guide and Core10GBaseKR_PHY User Guide.
- For information about Libero, ModelSim, and Synplify, visit Microchip Libero SoC webpage.
- For information about Smart Debug, see Smart Debug User Guide.

9. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 9-1. Revision History

Revision	Date	Description
A	12/2023	Initial Release

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