

ATA6560 - CAN Transceiver VHDL-AMS Model (Level 1)

ATAN0131

Introduction

This document contains the documentation for the simulatable, simulation-runtime-optimized behaviorally modeled high-speed-CAN transceiver Atmel® ATA6560 according to [1] and was tested according to [2]. The implementation level of the provided model is according to the “Level 1” model requirements of [1], see [Section 1. “Implementation” on page 3](#) for more details. This “Level 1” model is intended to be used only for bus signal integrity checks and does not cover the full functionality of the real transceiver device.

Terms, Definitions and Abbreviations

Table 1. Terms, Definitions and Abbreviations

Short Name	Definition
BUS	CAN BUS
CANH	CAN BUS high channel
CANL	CAN BUS low channel
CM	Common mode = $(CANH + CANL) / 2$
CAND	Differential mode = $(CANH - CANL)$
RXD	Receiver pin / receiver signal
TXD	Transceiver pin / transceiver signal
VCC	Supply pin / supply level / supply signal
GND	Ground pin / ground level / ground signal
TEMP	High level model parameter with selects one of three possible scenarios

List of References

- [1] Requirement Specification for Transceiver Simulation Models V1.1, ICT/GIFT, 2010-02-22
- [2] Model Conformance Test Specification V1.1, ICT/GIFT, 2010-02-22
- [3] Road vehicles – Controller Area Network, Highspeed medium access unit, ISO 11898-2, 2003
- [4] Road vehicles – Controller Area Network, Highspeed medium access unit with low power mode, ISO 11898-5, 2007

1. Implementation

1.1 Implementation Language

The provided model is completely implemented in VHDL-AMS (IEEE 1076.1-1999). The implementation body is encrypted according to VHDL (IEEE 1076-2008) directives under SABER framework. An encrypted version for SystemVision framework may be available on customer demand. The model is implemented and tested to be compliant and executable at the following simulator environment:

- Synopsys SABER (Version B-2008.09-SP2 or newer)
- Mentor Graphics SystemVision (Version 5.9 or newer)

1.2 Functionalities and Properties

The model is implemented as a “Level 1” model according to [1] and therefore covers the following functionalities:

- Transmitter function (output voltages and currents, rise and fall times, propagation delays, ground offset)
- Receiver function (thresholds, propagation delays, ground offset)
- Bus biasing (impedances)

1.3 Functionalities not Implemented

The current model implementation does not cover correct short circuit behavior in terms of flowing currents and their value. The real device sets an internal flag, when the current exceeds some limits, but this diagnosis functionality is not required for a “Level 1” model.

2. Interface

As required, the level 1 of the model is pin-out compatible with the real device, with exception of NSIL and STBY pins (see [Figure 2-1](#)) and the interface is implemented according to section 3.3 and 3.6 of [1] with all mandatory pins and parameters. Refer to [Table 2-1](#) for a short description of each pin.

Figure 2-1. Real Device Pin-out

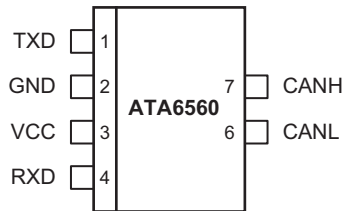


Table 2-1. Model Interface for Level 2

PIN Name	Description
CANH	CAN BUS high channel
CANL	CAN BUS low channel
RXD	Receiver
TXD	Transceiver
VCC	Supply
GND	Ground

3. Parameters

The model is parameterized regarding the high, low and typical characteristics of the device. The interface contains the model parameter “TEMP”. The following values are possible:

Table 3-1. Parameter “TEMP”, Possible Values

TEMP” Value	Description
–1	This setting covers the low temp behavior based on real device measurements and minimal characteristics as stated in the device datasheet
0	This setting covers the room temp behavior based on real device measurements and typical characteristics as stated in the device datasheet
1	This setting covers the high temp behavior based on real device measurements and maximal characteristics as stated in the device datasheet

3.1 Time Delays Implementation

In order to reach a balance between the specification in datasheet and the values obtained from the verification process measures, an interpolation was made with the delays parameters. In [Table 3-2](#), the parameters from datasheet are shown while in [Table 3-3](#) the interpolated values implemented in this model are shown.

It is worth to mention that the delay at the edge from dominant to recessive state was over-delayed with respect to the interpolation rule. This was done in order to achieve a typical delay based in our laboratory measurements, as no information was provided from the manufacturer. The results are clearly visible for a Room temperature in a Star topology ringing behavior (see [Section 6. “Network behavior” on page 11](#)).

Table 3-2. Propagation Delays from Datasheet

Delay	Transition	Measurement			Unit
		Low	Room	Max	
TXD to RXD	DOM to REC	40	-	200	ns
	REC to DOM	40	-	200	ns
TXD to CAN	DOM to REC	40	-	200	ns
	REC to DOM	40	-	200	ns
CAN to RXD	DOM to REC	20	-	100	ns
	REC to DOM	20	-	100	ns

Table 3-3. Propagation Delays, Implemented Values

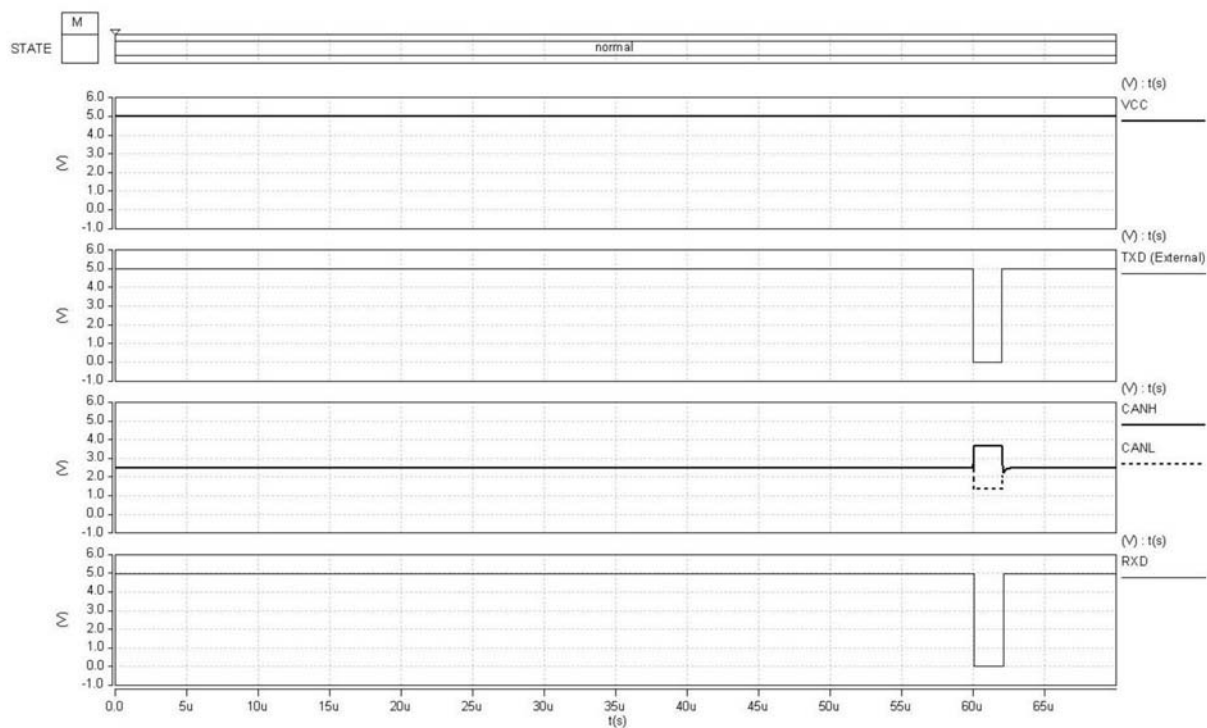
Delay	Transition	Implemented Values			Unit
		Low	Room	Max	
TXD to RXD	DOM to REC	40	163	195.5	ns
	REC to DOM	40	116.25	195.5	ns
TXD to CAN	DOM to REC	26.666	67.083	110.5	ns
	REC to DOM	26.666	67.083	110.5	ns
CAN to RXD	DOM to REC	13.333	49.1666	85	ns
	REC to DOM	13.333	49.1666	85	ns

4. Modeled States

For a Level 1 implementation, the device will always be in normal mode when the supply is connected. No other state implementation is required in [1].

4.1 Initial Conditions

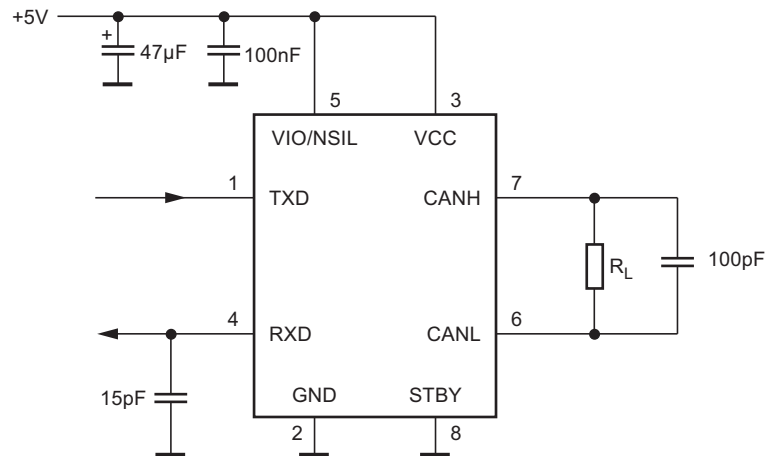
Figure 4-1. Initialization of the Model



5. Signal Matching

In this section is shown a match between the measured waveforms and the simulation results of the model. This test was performed in the 3 temperatures scenarios and analyzed in maximal detail for dominant to recessive and recessive to dominant edges. The results are shown from [Figure 5-2](#) to [Figure 5-7](#) on page 10. [Figure 5-1](#) shows the implemented test circuit, which is the same as the datasheet specifies. R_L is 62Ω .

Figure 5-1. Test Circuit



5.1 Dominant to Recessive Edge

Figure 5-2. Dominant to Recessive Edge (High)

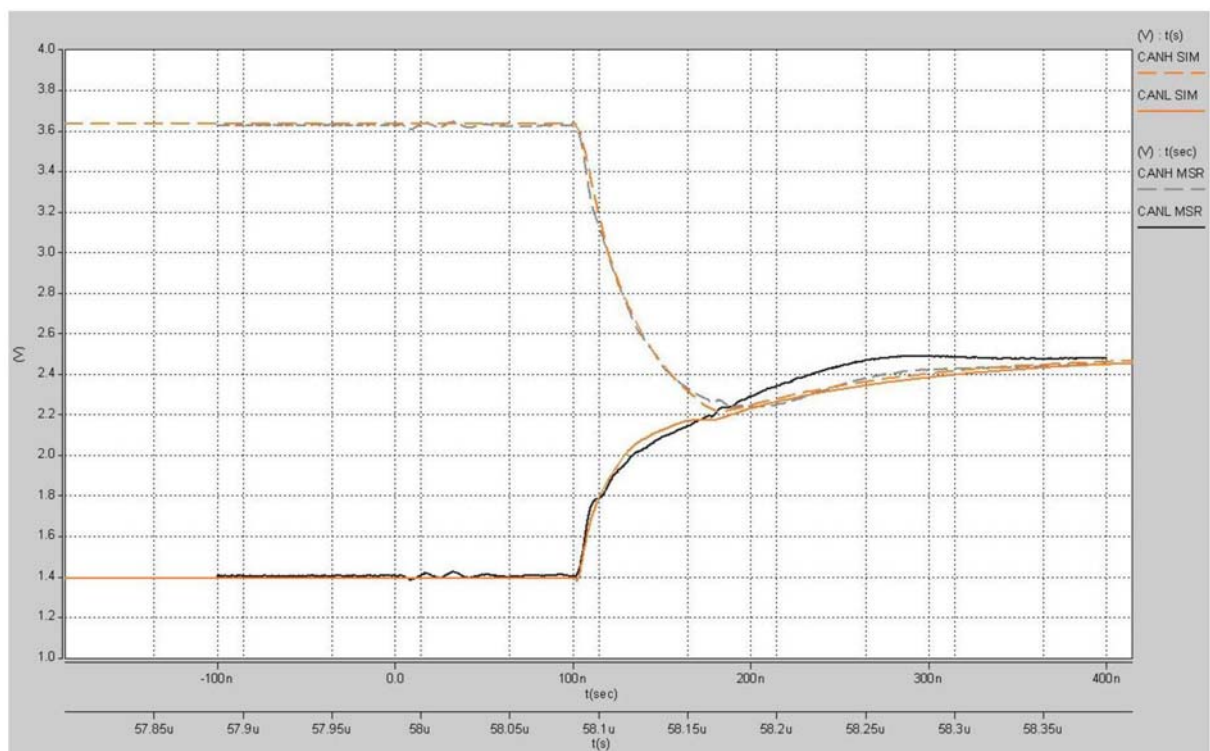


Figure 5-3. Dominant to Recessive Edge (Low)

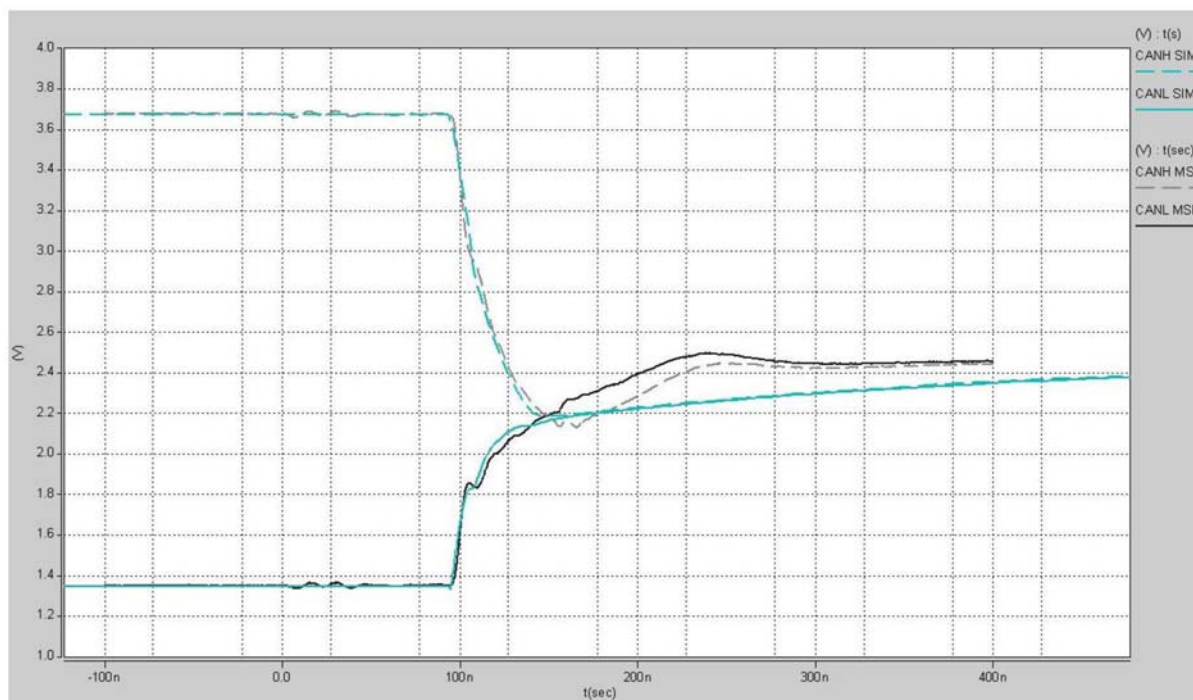
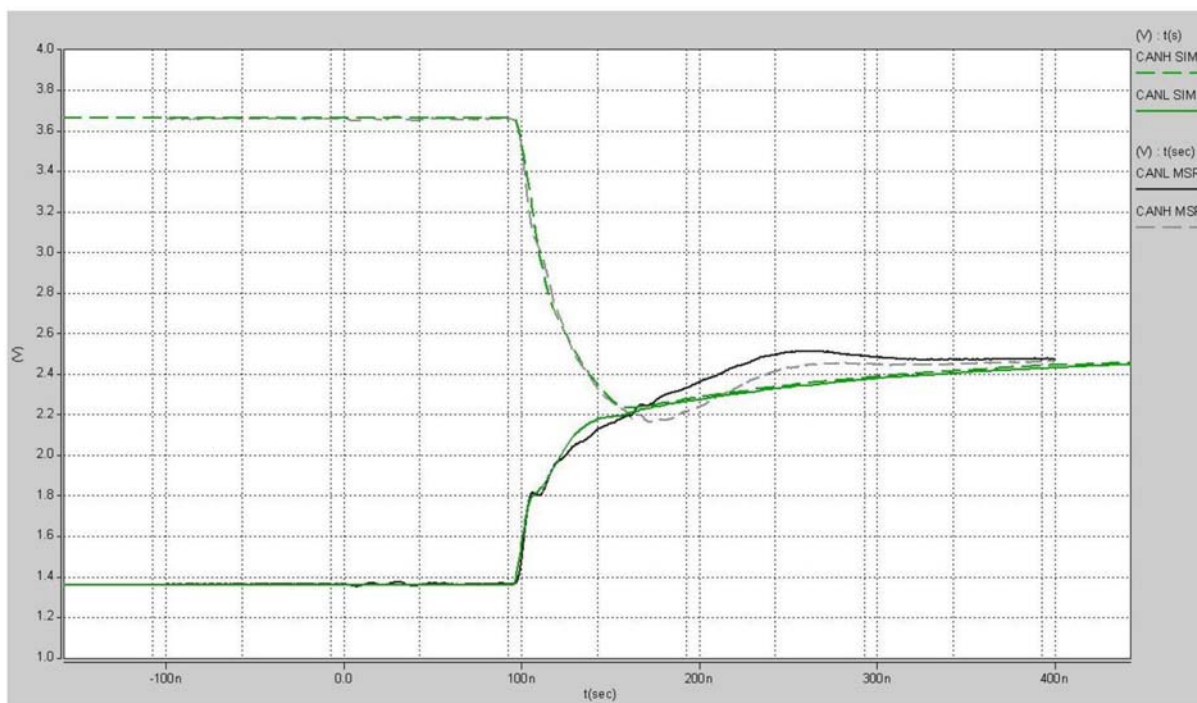


Figure 5-4. Dominant to Recessive Edge (Room)



5.2 Recessive to Dominant Edge

Figure 5-5. Recessive to Dominant Edge (High)

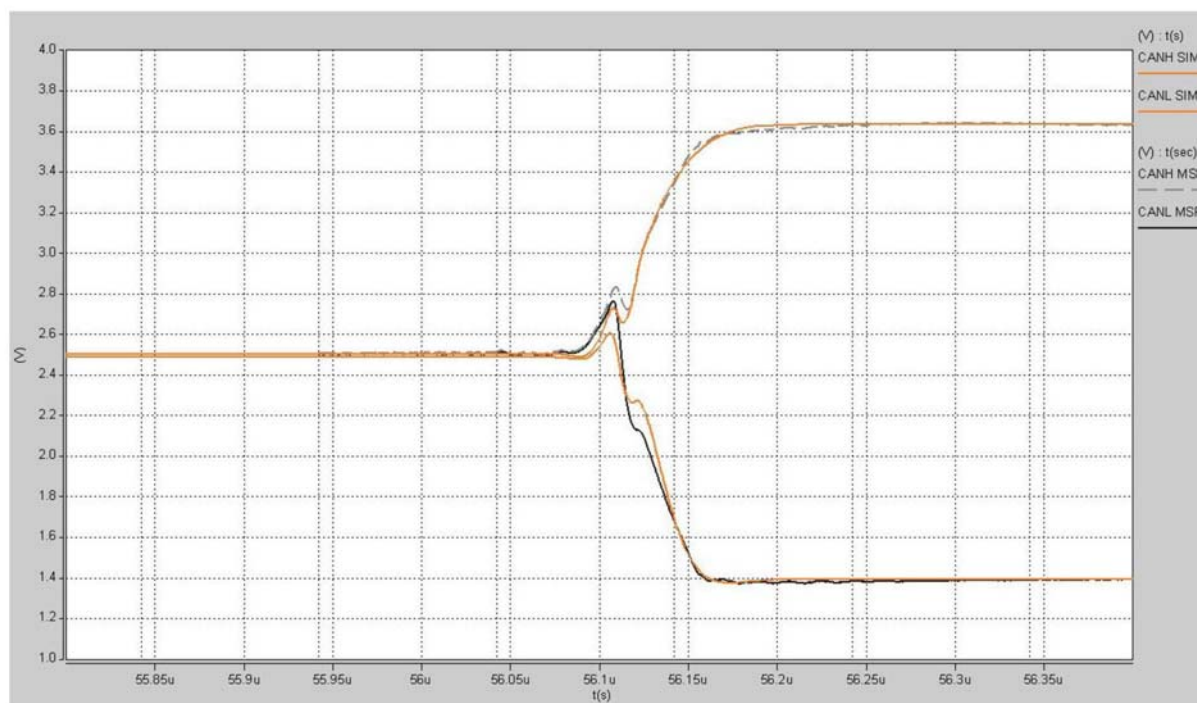


Figure 5-6. Recessive to Dominant Edge (Low)

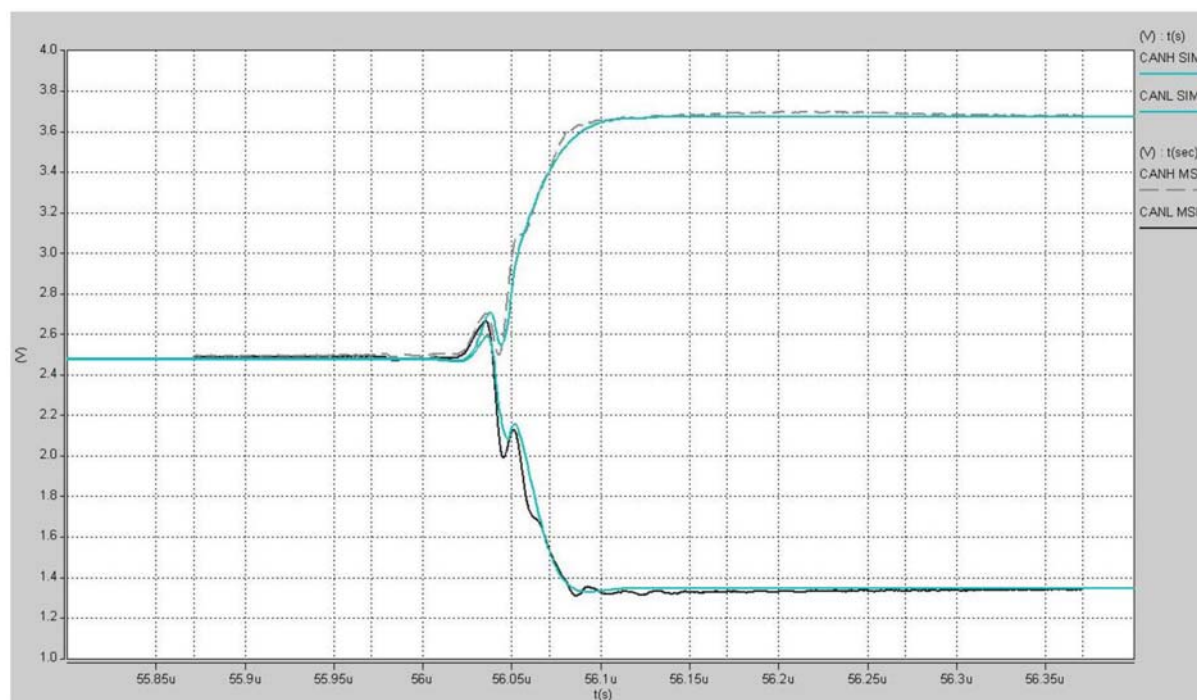
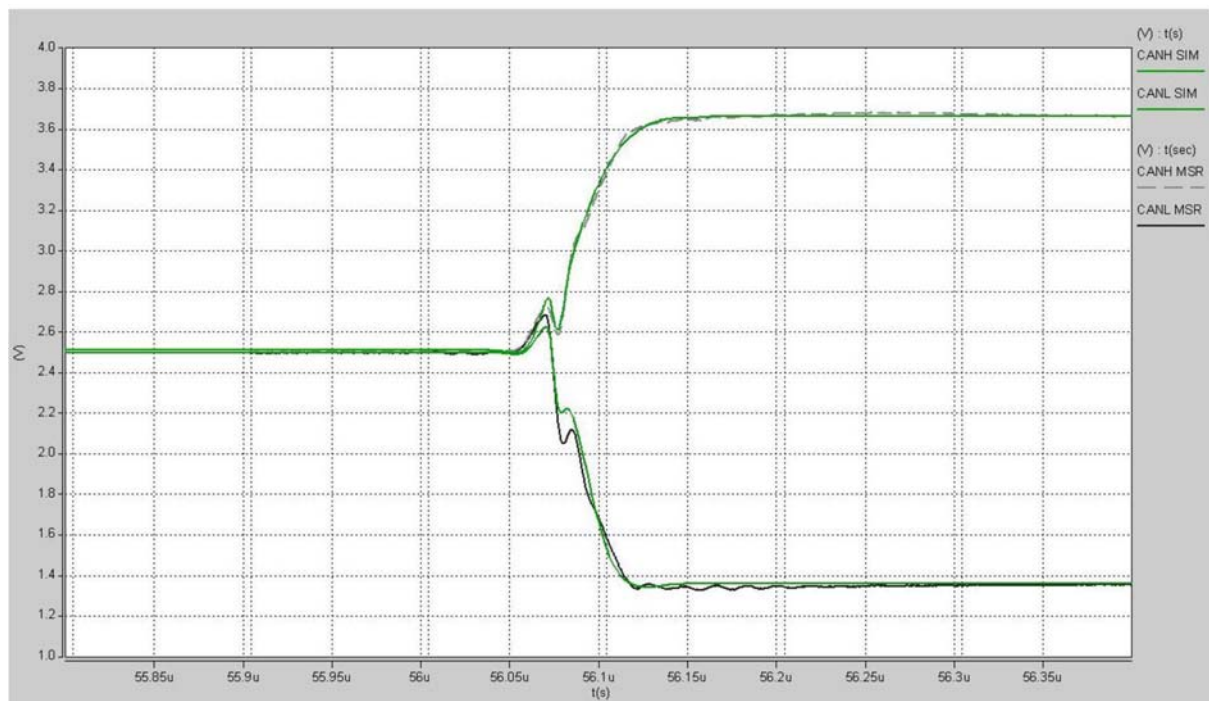


Figure 5-7. Recessive to Dominant Edge (Room)



6. Network behavior

A test was performed in order to analyze the behavior of the model in a network of 8 devices. The network, as defined in [2], contains the characteristics described in [Figure 6-1](#) and [Table 6-1](#). The network topology is a Star ended with typical application resistor which in this case was 62Ω and no load capacitance was implemented.

Figure 6-1. Network Topology

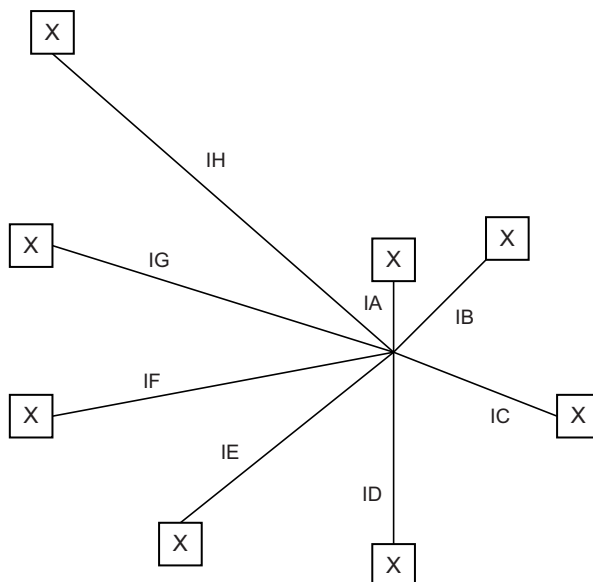


Table 6-1. Network Characteristics

Name	Node Number	Length [m]
IA	1	1.2
IB	2	2
IC	3	3.1
ID	4	4.5
IE	5	5.2
IF	6	5.9
IG	7	7.1
IH	8	8.1

[Figure 6-2](#) and [Figure 6-3 on page 12](#) show the behavior of the model in this kind of network. These figures show the measured signals CANH and CANL and the simulated signals as well. Common mode (CM) and differential mode (CAND) are computed from the mentioned signals.

Only the best and worst case are here shown, i.e. Node 1 and Node 8. The rest of the nodes show a behavior which can be interpreted as interpolation between the behavior of Node 8 and the behavior of Node 1. In this way Node 7 behaves worse than Node 2 but better than Node 8 and so on. This is understandable when looking at [Table 6-1](#), which shows the length of each stub. The non-perfect-matching ringing signals are because of the mismatch between the characteristics of the real components (termination, transmission line, connections, etc.) and the ones used for simulation.

In [Figure 6-2 on page 12](#) a dominant bit is generated in Node 1 and observed with the scope on its output. In [Figure 6-3 on page 12](#) a dominant bit is generated in Node 8 and observed with the scope on its output.

Figure 6-2. Node 1 Sending and Observed

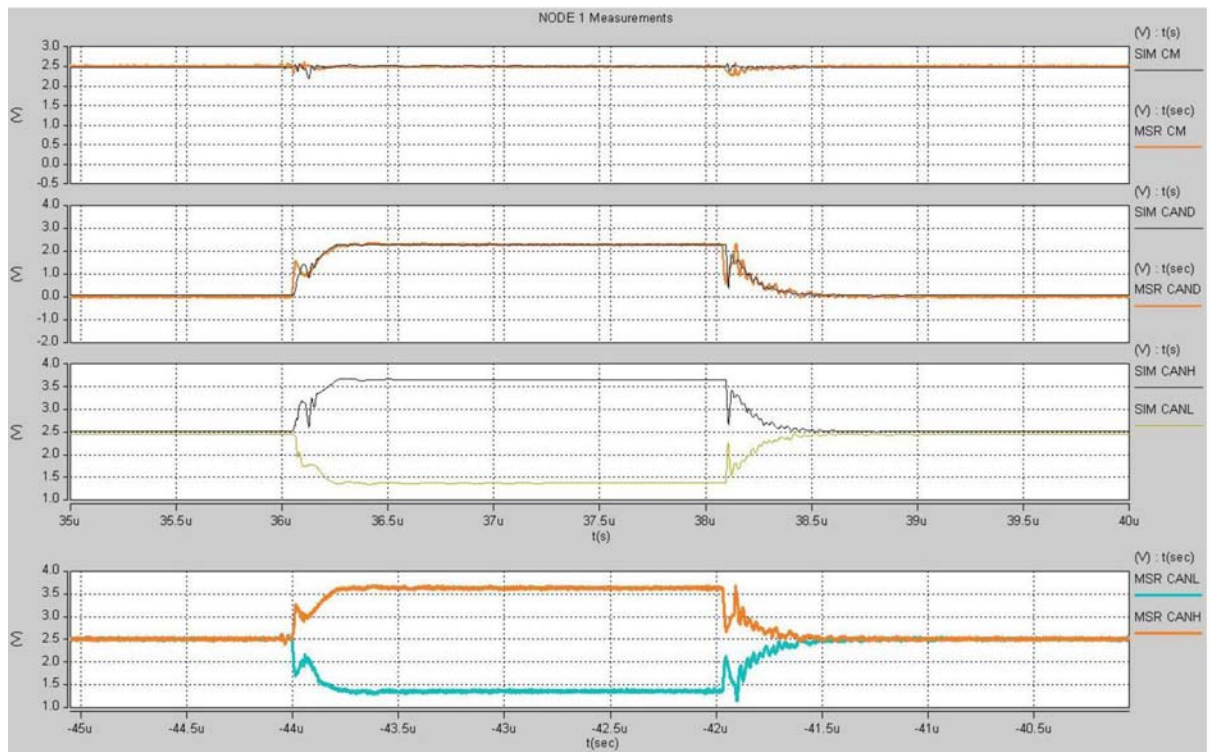


Figure 6-3. Node 8 Sending and Observed

