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DOCUMENT DESCRIPTION
Routing Checklist for the LAN91C111, 128-pin TQFP Package

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Routing Checklist for LAN91C111

Information Particular for the 128-pin TQFP Package

1. The traces connecting the transmit outputs (TPO+, pin 14) & (TPO-, pin 15) to the magnetics must be run as differential pairs. The differential impedance should be 100 ohms.
2. The traces connecting the transmit outputs from the magnetics to pins 1 & 2 on the RJ45 connector must be run as differential pairs. Again, the differential impedance should be 100 ohms.
3. The traces connecting the receive inputs (TPI+, pin 17) & (TPI-, pin 18) from the magnetics must be run as differential pairs. The differential impedance should be 100 ohms.
4. The traces connecting the receive inputs on the magnetics from pins 3 & 6 on the RJ45 connector must be run as differential pairs. Again, the differential impedance should be 100 ohms.
5. Typically, all planes are cleared out from under the differential pairs connecting the RJ45 and the magnetics. The plane clear out boundary is usually halfway through the magnetics.
6. Trace impedance depends upon many variables (PCB construction, trace width, trace spacing, etc.). The electrical engineer needs to work with the PCB designer to determine all these variables.
7. Try to keep all other signals out of the Ethernet front end (RJ45 through the magnetics to the LAN chip). Any noise from other traces may couple into the Ethernet section and cause problems.
8. Also recommended, is the construction of a separate chassis ground that can be easily connected to digital ground at one point. This plane provides the lowest impedance path to earth ground.
9. The routing for the crystal or clock circuitry should be kept as small as possible and as short as possible.
10. The MII interface on the LAN91C111 should be constructed using 68 ohm traces.
11. The RBIAS resistor (pin 12) should be routed with a short, wide trace. Any noise induced onto this trace may cause system failures.
12. Route the (10) decoupling capacitors for the LAN91C111 as short as possible to each separate power pin. There should be a short, direct copper connection as well as a connection to each power plane on each cap.
13. SMSC recommends utilizing at least a four-layer design for boards for any LAN design.
14. Bulk capacitors for each power plane should be routed immediately into power planes with traces as short as possible and as wide as possible.
15. Following these guidelines and other general design rules in PCB construction should ensure a clean operating system.