Design Guide
for Atmel's C51 Standard Devices

C51 MCU's

Introduction

The aim of this document is to help customers to avoid errors that are frequently done in order save efforts and time during hardware debugging sessions.

This document relates only to Atmel's C51 standard devices. It is the responsability of the user to read the datasheet of his own device and check if the features and procedures described here are applicable.

Abbreviations

- ISP: In-System Programming
- FLIP: FLexible In-system Programmer
- GUI: Graphical User Interface
- BLJB: Boot Loader Jump Bit
- HPC: High Pin Count
- LPC: Low Pin Count
- HSB: Hardware Security Byte

Application Notes used as references

- How to calculate the capacitor of the reset input of a C51 microcontroller
  (doc 4284.pdf)
- External Brown-out Protection for C51 microcontrollers with Active High Reset Input
  (doc 4183.pdf)
- How to use a third Overtone crystal with a 80C51 family microcontroller
  (doc397c496b2072e.pdf)

7764A–8051–11/07

1. Basics of ATMEL's C51 Standard devices

1.1 Program memory configurations

1.1.1 Scope

Figure 1-1. Code fetched from external program memory

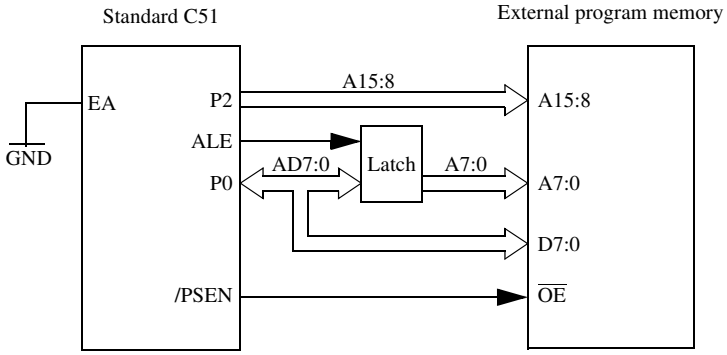


Figure 1-2. Code fetched from internal program memory

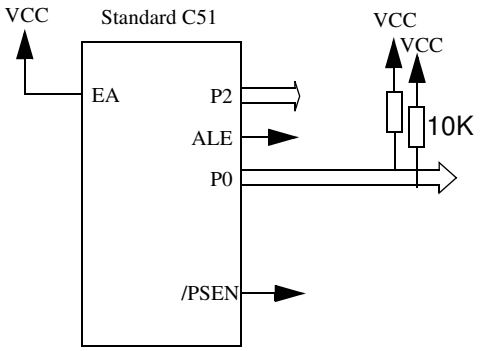


Table 1-1. Pin description

PIN	I/O	External Code	Internal Code
EA	Input	Must be connected to GND	Must be connected to VCC, directly or through a 10K resistor.
ALE	Output signal	This signal is used to clock the Least Significant Byte into the address latch.	Not used. Must be left unconnected in normal operation
PSEN	Output signal	This signal is used to strobe the external program memory when the MCU fetches the code byte.	Not used. Must be left unconnected in normal operation
P0	I/O port	Port 0 serves as a multiplexed address/data bus. It emits the low byte of the Program Counter (PCL) as an address, and then goes into a float state awaiting the arrival of the code byte from the Program Memory.	Can be used as a general purpose I/O port. In this case external 10K pull-up's must be provided.
P2	I/O port	Port 2 emits the high byte of the Program Counter (PCH)	Can be used as a general purpose I/O port. No external pull-up's are needed as this port owns internal pull-up's

1.1.2 Type of package

In most of the products, two kind of packages are proposed: the HPC (High Pin Count) and the LPC (Low Pin Count).

The HPC packages support the external code and therefore provide the appropriate pins (EA, ALE, PSEN, P0, P2), while the LPC packages do not support the external code and do not provide any of the dedicated pins.

1.1.3 Hardware Security Byte (HSB)

WARNING

Parts are delivered by default with HSB set to maximum security (see product datasheet for further information). This configuration prevents the MCU from fetching external code.

On ROM products the user will need to take care about the HSB configuration at the time he orders the mask ROM if the external code mode is needed on his application.

On FLASH products the user will need to perform a full chip erase by means of an external programmer before using the parts if the external code mode is needed on his application.

1.1.4 Reduced EMI Mode

The ALE signal is used to demultiplex address and data buses on port 0 when used with external program or data memory. Nevertheless, during internal code execution, ALE signal is still generated. In order to reduce EMI, ALE signal can be disabled by setting AO bit.

The AO bit is located in AUXR register at bit location 0. As soon as AO is set, ALE is no longer output but remains active during MOVX and MOVC instructions and external fetches. During ALE disabling, ALE pin is weakly pulled high.

1.2 Hardware reset

1.2.1 Internal features

Some C51 devices may implement the following features:

- Power On Reset (POR)
- Power Fail Detector (PFD)
- Hardware Watch-Dog Timer (WDT)
- Internal Pull-up on reset pin

There are different ways to drive the reset pin depending on which features are implemented in the device. The user is invited to carefully read the product datasheet to know which features are or are not implemented.

Figure 1-3. Reset bock diagram

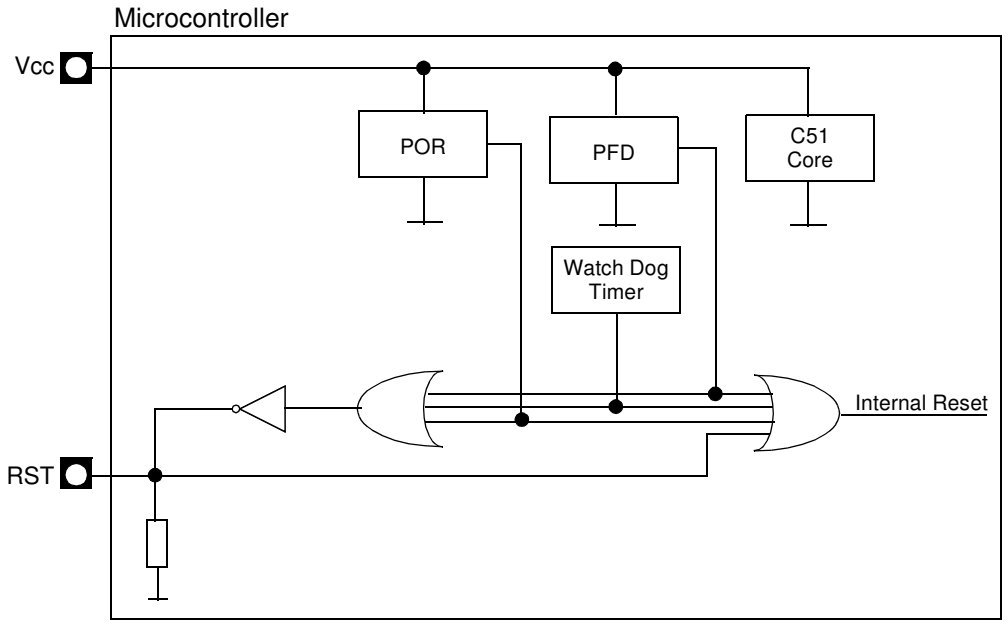
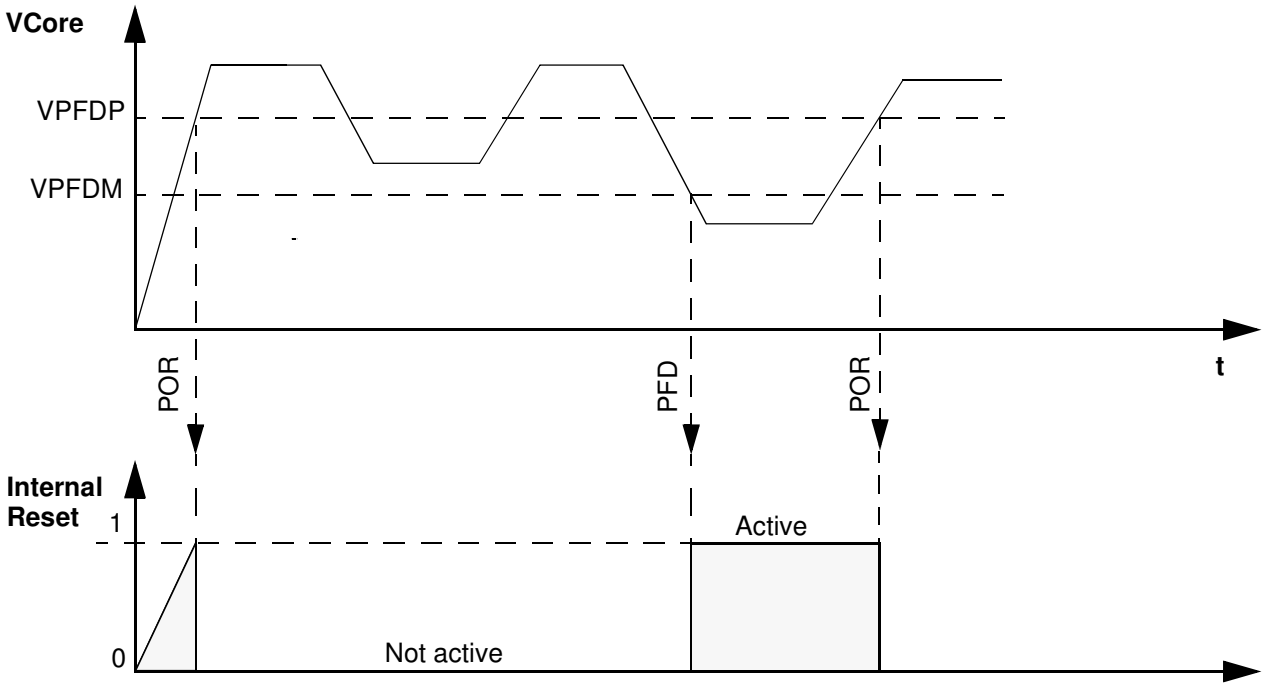


Table 1-2. Features descriptions

Feature	Description	Impact on RST pin
PFD	The role of the PFD is to monitor the power supply drops during a steady state condition in order to suspend the microcontroller's activity. When the PFD is active, it holds the MCU under a reset state to prevent the MCU from having unpredictable behaviour. Optional feature	While the PFD is active, the reset pin is driven by the PFD.
POR	The role of the POR is to monitor the rising of internal power supply of the microcontroller core. It releases the internal reset only when the internal voltage is enough for the core to operate. Optional feature	- No external components or superviser devices are needed to drive the reset pin - While the POR is active, the reset pin is driven by the POR - RST pin may be left unconnected
WDT	The WDT automatically resets the chip if the software fails to reset the WDT before the selected time interval has elapsed. Basic feature of C51 devices	While the WDT is active, the reset pin is driven by the WDT.
Internal Pull-up	Saves an external component	No external pull-up needed

Figure 1-4. Behaviour of POR and PFD



1.2.2 How to drive the RST pin according to the features implemented on the device

This procedure is only applicable to Active High reset pins. However, this procedure can be easily adapted for microcontrollers with Active Low Reset pins.

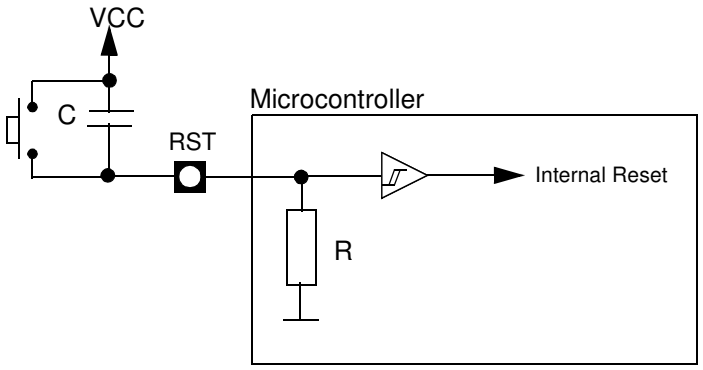
1.2.2.1 POR not implemented

When the POR is not implemented, it is necessary to implement external components to assure a correct reset of the MCU.

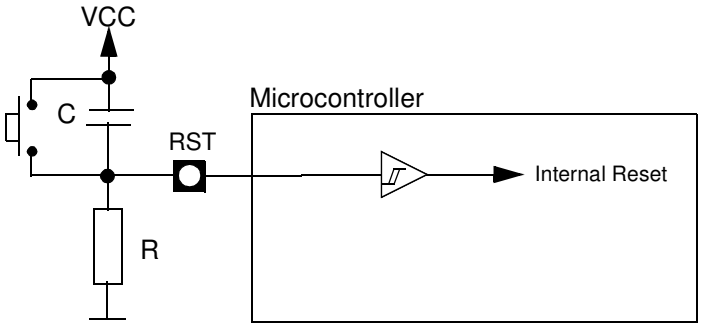
a) Using an external capacitor

Read application note " How to calculate the capacitor of the reset input of a C51 microcontroller" (doc 4284).

Internal pull-up



External Pull-up

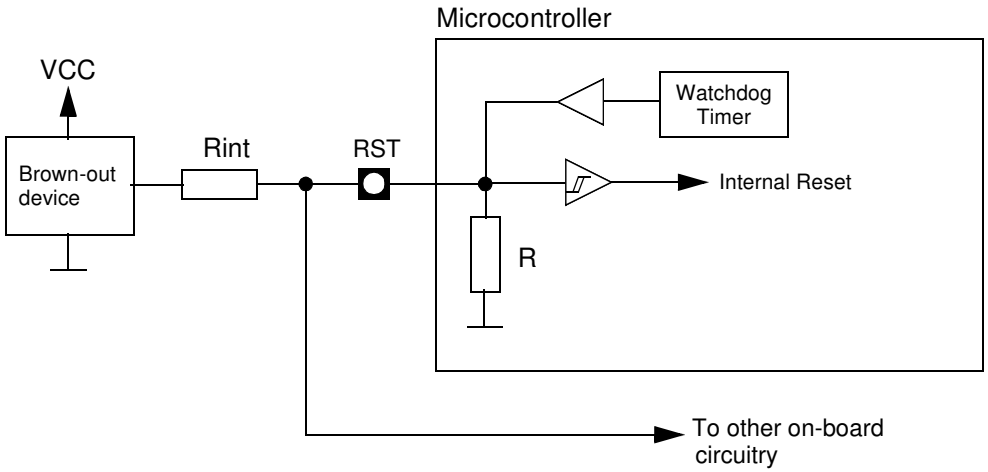


b) Using an external Brown-out device

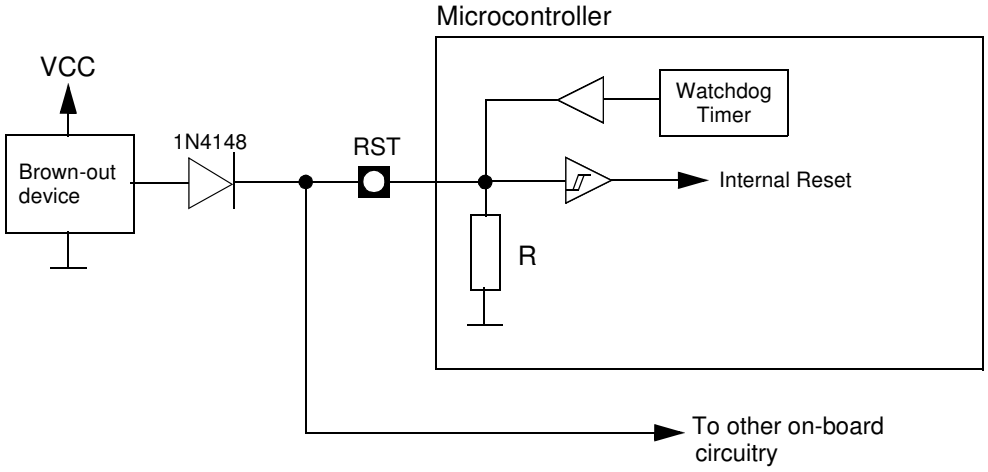
Read application note “External Brown-out Protection for C51 microcontrollers with Active High Reset Input“ (doc 4183).

Sometimes the RST pin may be internally forced by the WDT so that the external peripherals if any are reset at the same time as the MCU. While the WDT is active the RST pin operates as an output. Therefore the RST pin cannot be externally forced to a permanent level. If the external Brown-out device operates in this way, an intermediate resistor Rint or a diode must be implemented between the Brown-out device and the RST pin.

Brown-out device with an intermediate resistor



Brown-out device with a diode

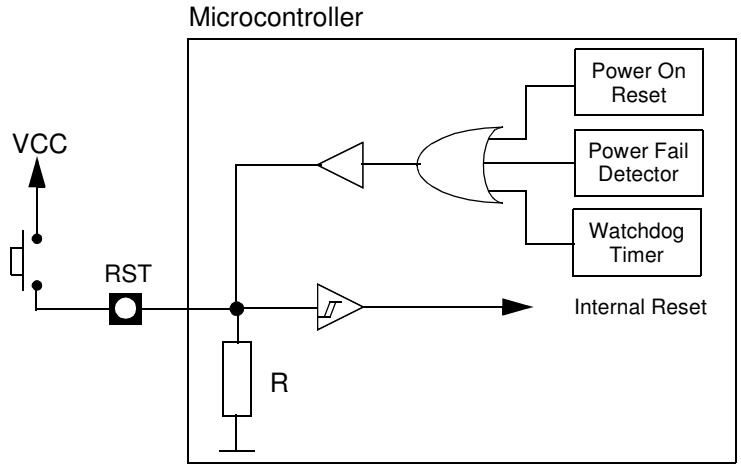


1.2.2.2 POR implemented

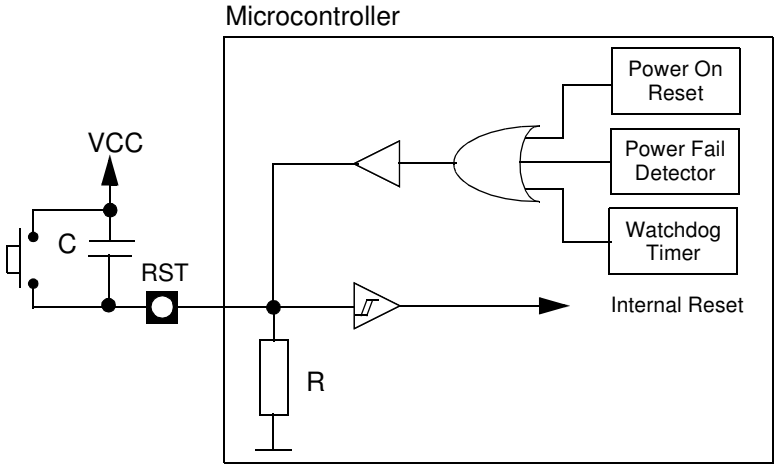
When the POR is implemented, the use of external components is optional.

The RST pin may be left unconnected.

a) No external components used



b) Using an external capacitor

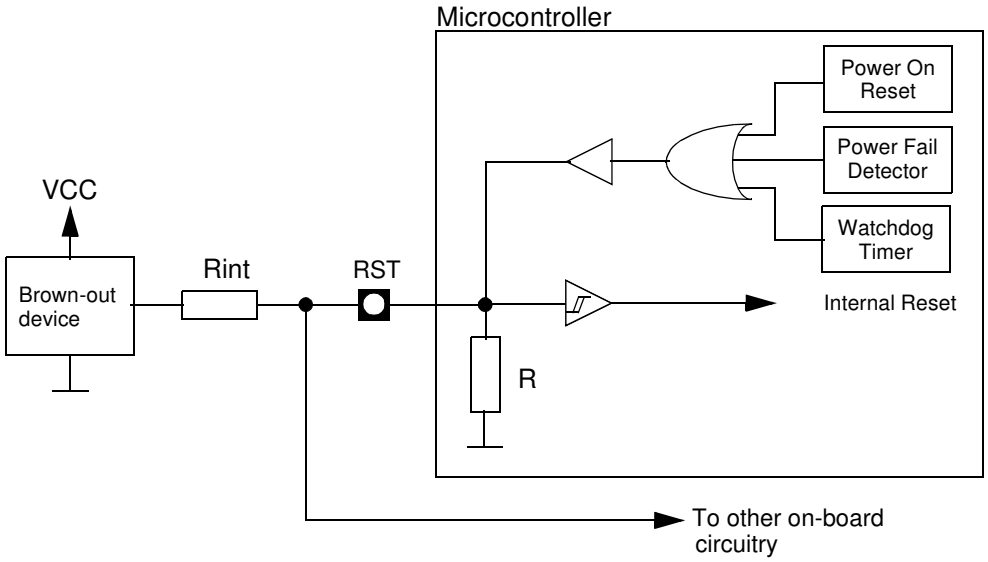


c) Using an external Brown-out device

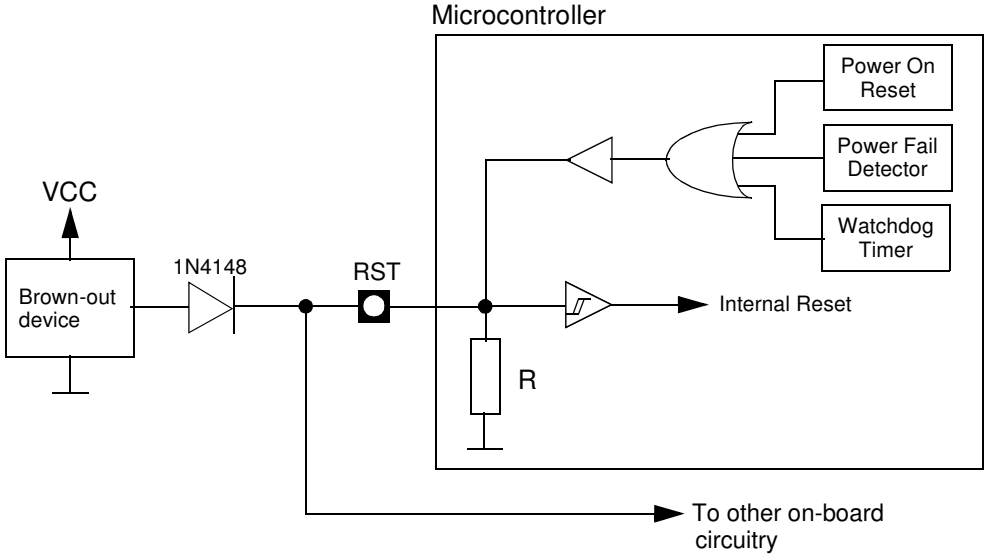
Read application note “External Brown-out Protection for C51 microcontrollers with Active High Reset Input“ (doc 4183).

Sometimes the RST pin may be internally forced by the POR or the PFD or the WDTso that the external peripherals if any are reset at the same time as the MCU. While the POR or the PFD or the WDT are active the RST pin operates as an output. Therefore the RST pin cannot be externally forced to a permanent level. If the external Brown-out device operates in this way, an intermediate resistor Rint or a diode must be implemented between the Brown-out device and the RST pin.

Brown-out device with an intermediate resistor



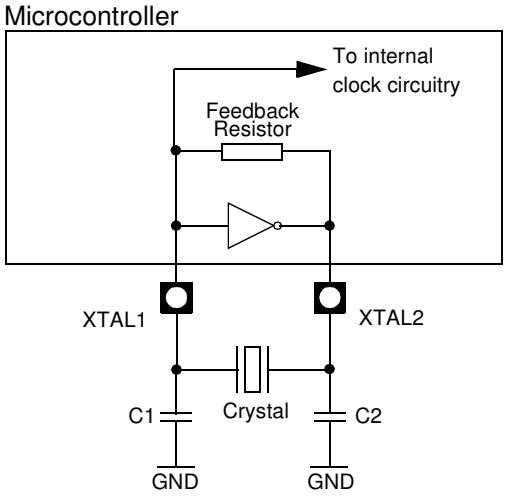
Brown-out device with a diode



1.3 Oscillator circuit

The on-chip oscillator is composed of a single-stage inverter and a parallel feedback resistor. The XTAL1 and XTAL2 pins are respectively the input and the output of the inverter, which can be configured with off-chip components as a Pierce oscillator.

Figure 1-5. Oscillator Schematic



CL: load capacitance given by crystal's manufacturer

CI: internal capacitance of the MCU (given by the product datasheet)

CS: Stray capacitance of the circuit board

C1, C2: external capacitors

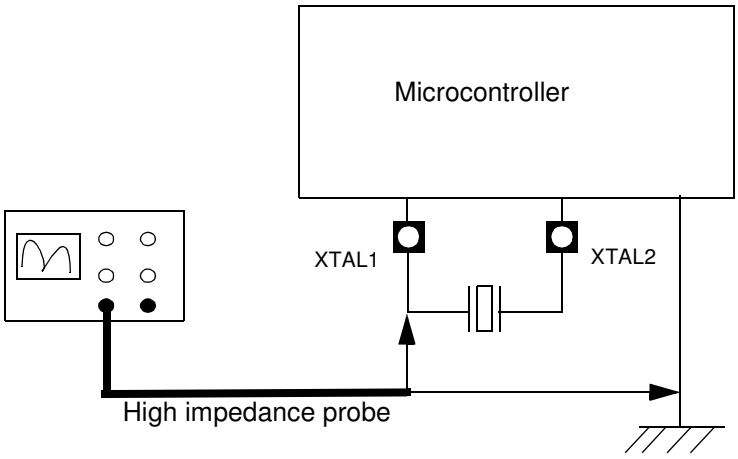
We have the following equation: CL = (C1xC2)/(C1+C2)+CI+CS

If C1=C2=CF and CS is negligible then CL = CF/2+CI and CF=2x(CL-CI)

1.3.1 Test conditions

It is recommended to monitor the clock on XTAL2 pin.

Special care must be taken when measuring XTAL1 signal. A high impedance probe must be used to avoid any distorsion of the signal.



Test condition: probe's impedance > 1 MOhm

This means that oscilloscope's active probes are prohibited due to their weak impedance (usually around 100KOhm)

1.3.2 Relationship between oscillator and ALE frequencies

Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of the oscillator frequency and can be used for external timing or clocking.

Note that one ALE pulse is skipped during each access to external data memory.

ALE can be disabled by setting SFR's AUXR.0 bit. When this bit is set, ALE will be inactive during internal fetches.

MCU's Clock mode	ALE frequency
X1 mode	Freq(ale) = Freq(osc)/6
X2 mode	Freq(ale) = Freq(osc)/3

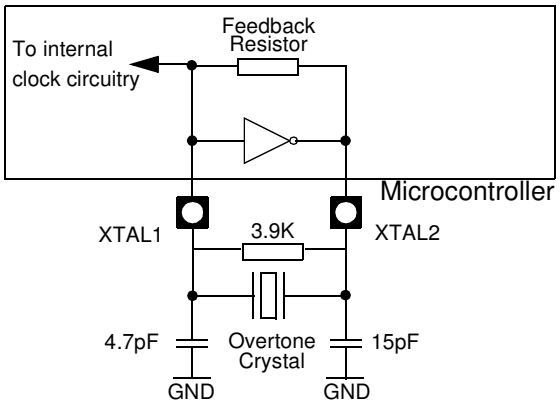
1.3.3 Overtone crystals

Problem: Sometimes overtone crystals are used with a standard oscillator circuit where a specific one is required to make the crystal to oscillate on its third overtone.

Consequence: an overtone crystal used with a standard oscillator circuit, oscillates on its fundamental frequency instead of oscillating on its third overtone frequency. The clock frequency seen by the MCU is 1/3 of the expected frequency.

Action: check the type of the crystal you are using. If you really want to use an overtone crystal, apply one of the following solutions.

1. A resistor of 3.9K between Xtal1 et Xtal2, a cap of 4.7 pF between Xtal1 and Vss, and a cap of 15pF between Xtal2 and Vss



2. Read application note “How to use a third Overtone crystal with a 80C51 family microcontroller” (doc397c496b2072e.pdf). Apply the following component values :
   L1= 1.5 µH
   C3=4.7nF
   CP1=12pF
   CP2=27pF
   C2 : not needed

3. Same solution as number 2 except the LC network is, in this case, connected to Xtal1 :
   L1= 1.5 µH
   C3=4.7nF
   CP1=10pF
   CP2=10pF

1.4 Microcontroller status

During hardware or firmware debugging, it is sometimes interesting to know what the state of the microcontroller is. See table below for details.

Hardware conditions		Microcontroller status							
RST	**EA**	**ALE**	**PSEN**	**XTAL2**	**Mode**	**P0**	**P1**	**P2**	**P3**
Active	1	1	1	Flat	Reset		FF	FF	FF
Not active	1	Toggling	1	Toggling	Operating mode Fetches internal code				
Not active	1	1	1	Toggling	Idle mode Does not fetch code	Port Data(1)	Port Data	Port Data	Port Data
Not active	1	0	0	Flat	Power down mode Does not fetch code	Port Data(1)	Port Data	Port Data	Port Data
Active	0	1	1	Flat	Reset	FF	FF	FF	FF
Not active	0	Toggling	1	Toggling	Operating mode Fetches external code				
Not active	0	1	1	Toggling	Idle mode Does not fetch code	Floating	Port Data	Address	Port Data
Not active	0	0	0	Flat	Power down mode Does not fetch code	Floating	Port Data	Port Data	Port Data

Note: Port 0 can force a 0 level. A "one" will leave port floating.

2. In-System Programming (ISP)

The In-System Programming feature will be referenced as ISP in the rest of the document.

Most of Atmel's C51 devices support the ISP mode. This feature enables the user to program the device directly on his application without having to unsolder the device or using an external programmer. This feature is made by means of a bootloader firmware embedded in the device itself. A PC based application like FLIP (FLexible In-system Programmer) or any equivalent custom software enables to communicate with the bootloader to perform the part programming.

FLIP can be downloaded free of charge from the Atmel's web site. It supports different interfaces like RS232, USB, and CAN following the used device. Ensure you are always using the latest version of FLIP.

The ISP mode is invoked by applying an hardware condition. The hardware condition differs between a HPC and a LPC package (See "Type of package" on page 3.)

2.1 HPC package

2.1.1 Hardware settings

The following hardware settings must be applied in normal mode (execution) before starting the ISP mode (programming).

- EA pin must be tied to Vcc. The bootloader is only active when internal program memory is used.
- ALE pin cannot be forced by an external signal. This pin is driven by the MCU. Leave this pin unconnected if not used.
- PSEN pin cannot be forced by an external signal. This pin is driven by the MCU. Leave this pin unconnected if not used.

2.1.2 Starting the ISP mode

Software condition: there are some configuration bits available in the part which enables to configure the bootloader behaviour. Refer to the product's bootloader datasheet for further information. These bits are accessible from the GUI of FLIP. The BLJB bit is part of these. Most of the time, it is activated at manufacturing level on new chips to have the device run in ISP mode at first power on. When the BLJB is active, the user does not need to apply the hardware condition described here after. It may be usefull at production level for instance. The BLJB bit is deactivated by the bootloader after the first programming. It is then the responsability of the user to re-activate it.

Hardware condition: when the BLJB bit is inactive, the only way to have the device run in ISP mode, is to apply the hardware condition.

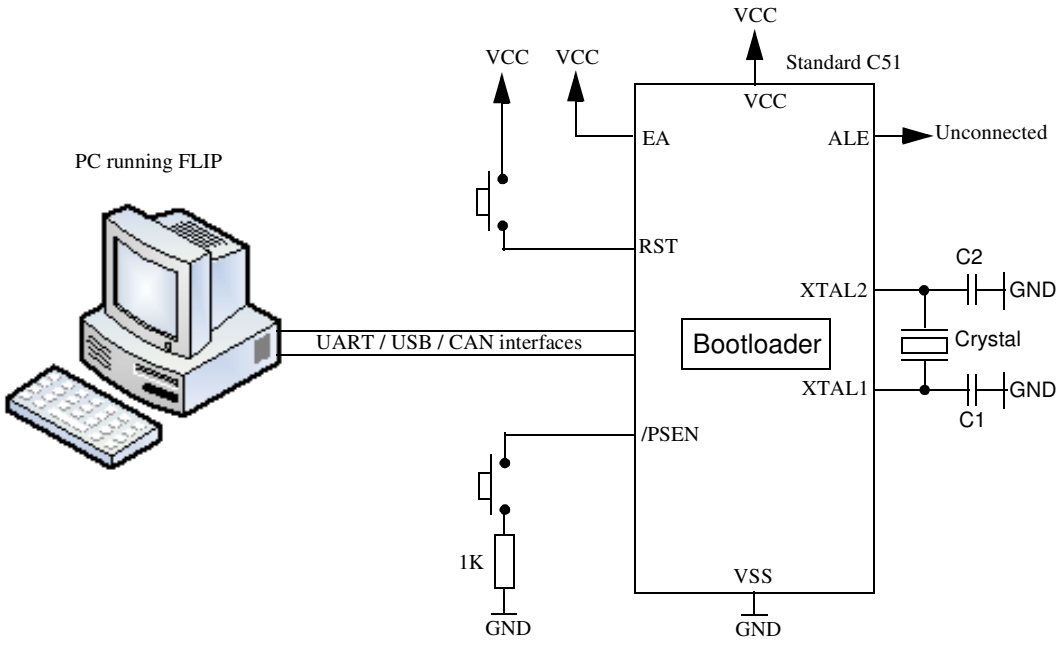
The hardware condition consists to apply an hardware reset while pulling the PSEN pin to ground then to release the PSEN pin once the hardware reset has been applied.

It is recommended to pull the PSEN pin to ground through a 1K resistor to prevent the PSEN pin from being damaged.

WARNING

Do not apply the hardware condition at power up otherwise the ISP mode may fail to start. The hardware condition must be applied only when the device has started and when the power supplies are stables.

Figure 2-1. HPC hardware condition



2.2 LPC package

2.2.1 Hardware settings

There are no specific hardware settings to apply.

2.2.2 Starting the ISP mode

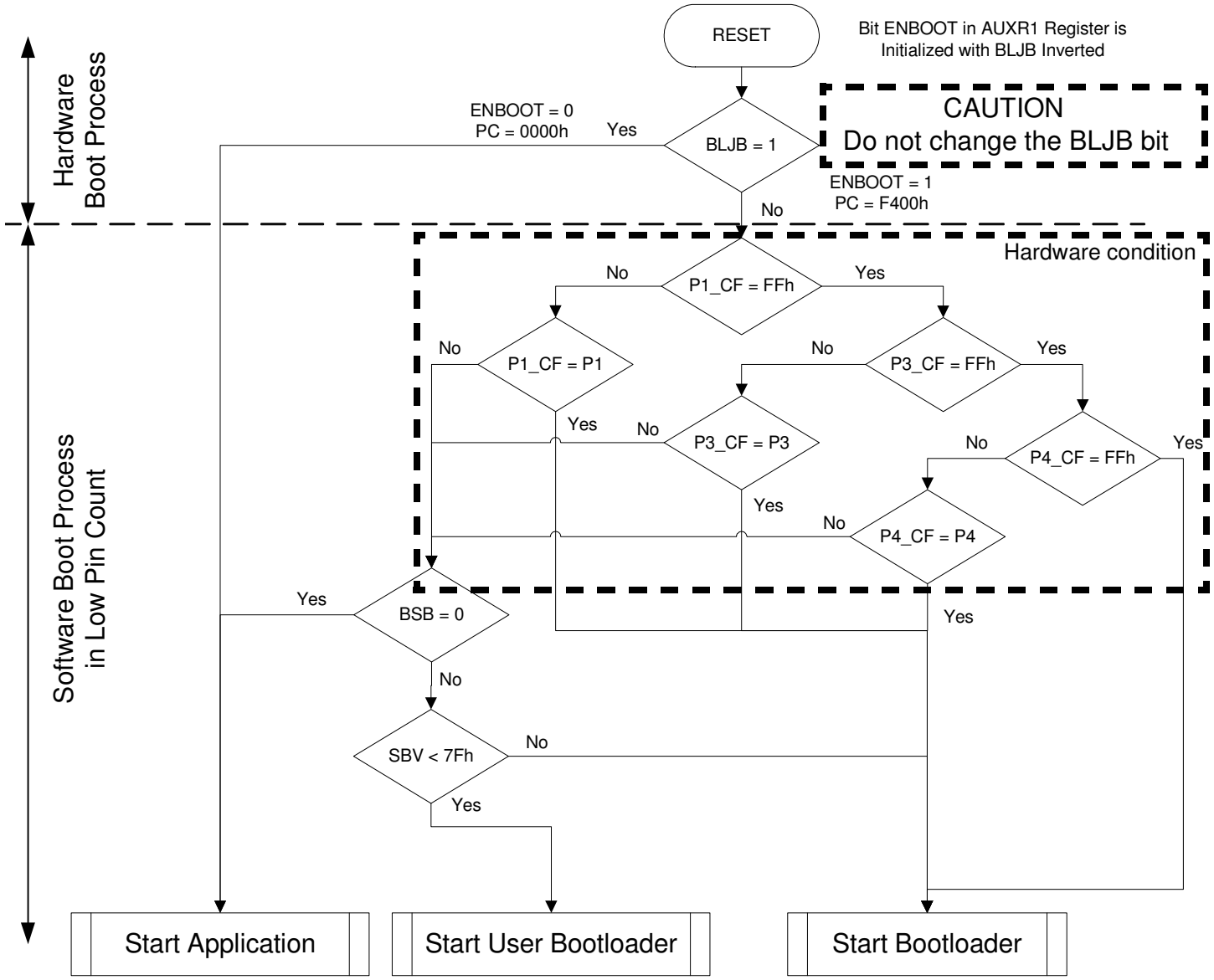
Software condition:

WARNING

For LPC packages the BLJB bit is activated at manufacturing level and MUST NEVER be changed by the user. If this ever occurs, the only way to restore the ISP mode is to re-program the device by an external programmer.

Normally the BSB (Boot Status Byte) is activated (0xFF) at manufacturing level on new chips to have the device run in ISP mode at first power on. When the BSB is active, the user does not need to apply the hardware condition described here after. It may be useful at customer's production level for instance. The BSB is deactivated (0x00) by the bootloader after the first programming. It is then the responsability of the user to re-activate it.

Figure 1. Low Pin Count regular boot process

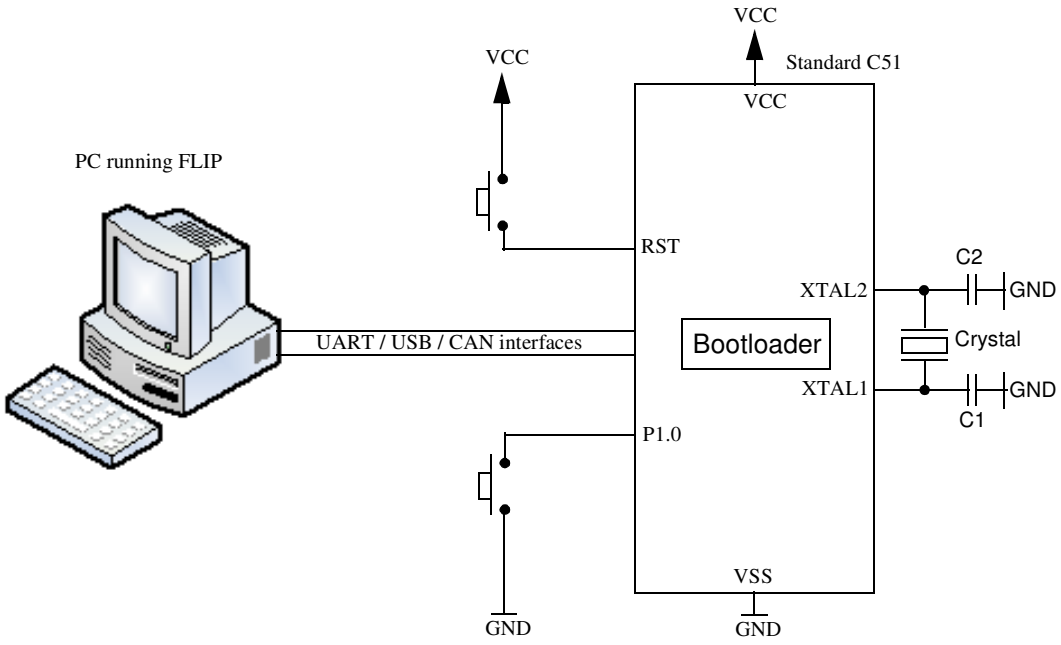


Hardware condition: when the BSB is inactive, the only way to have the device run in ISP mode, is to apply the hardware condition.

As the PSEN pin is not available in LPC packages, a port pin is used instead to apply the hardware condition which consists by default to apply a hardware reset while pulling P1.0 pin to ground then to release P1.0 pin once the hardware reset has been applied.

P1.0 is an Atmel default setting which can be easily changed by FLIP. The user can select a another port if P1.0 is inappropriate for his application. Refer to the product's bootloader datasheet for further information.

Figure 2-2. LPC hardware condition



2.3 Using the ISP mode over RS232 interface

2.3.1 Baudrate

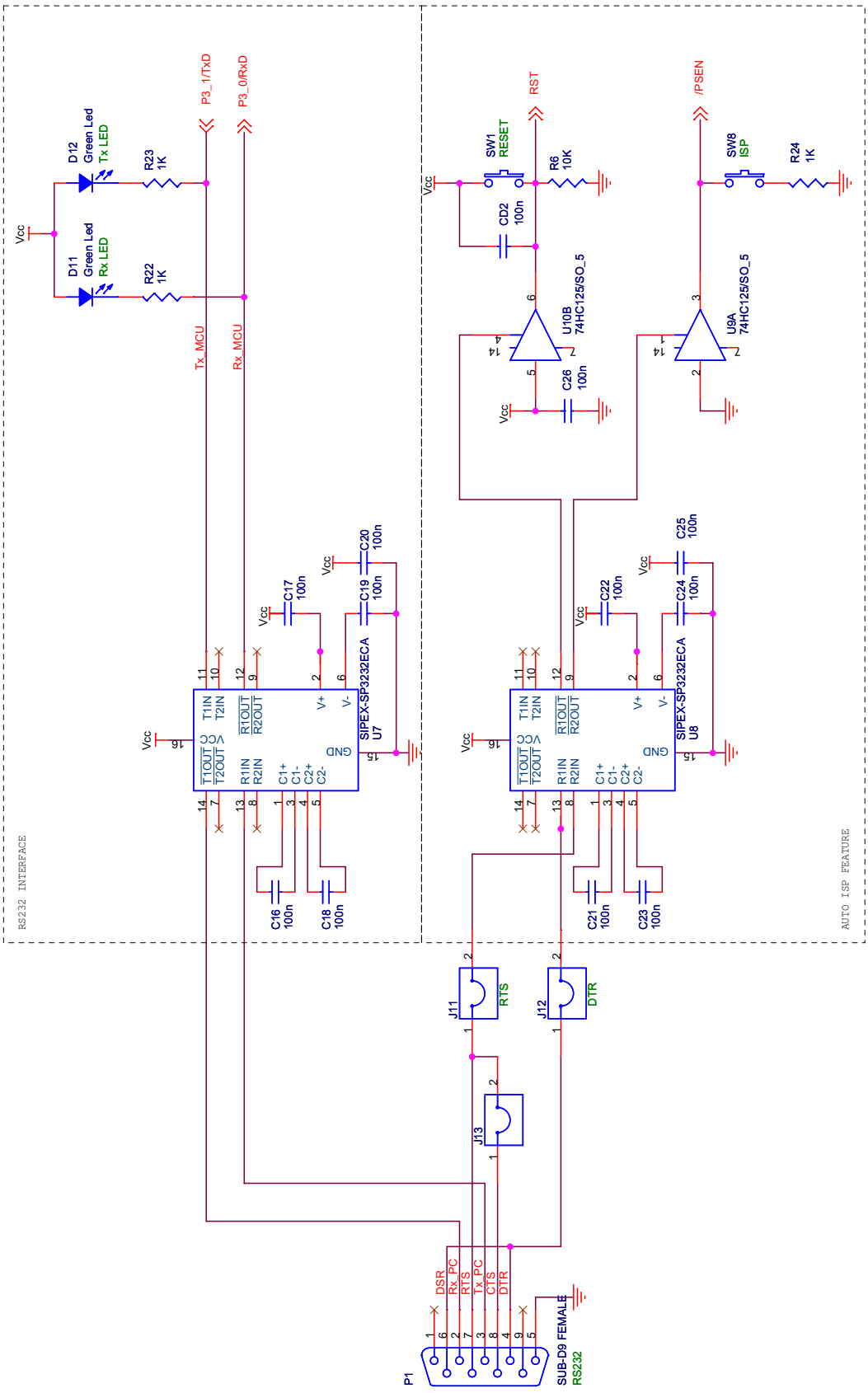
The maximum baudrate supported by the device depends on the crystal value or signal frequency injected on XTAL1 pin. Refer to product datasheet for further information.

2.3.2 Hardware

The schematics of the interface are given here after.

Auto ISP feature: the implementation of this feature is optional.

When this feature is supported by the hardware, the same option can be activated in the preferences menu of FLIP. This option enables FLIP to manage and set automatically the hardware condition to have the device run in ISP and to proceed with the part programming.


RS232 INTERFACE
AUTO ISP FEATURE
D12
Green Led
Tx LED
D11
Green Led
Rx LED
R23
1K
R22
1K
Vcc
P3_1/TxD
P3_0/RxD
Tx_MCU
Rx_MCU
SW1
RESET
RST
R6
10K
CD2
100n
SW8
ISP
/PSEN
R24
1K
U10B
74HC125/SO_5
U9A
74HC125/SO_5
C26
100n
C17
100n
C20
100n
C19
100n
C22
100n
C25
100n
C24
100n
C16
100n
C18
100n
C21
100n
C23
100n
SIPEX-SP3232ECA
U7
SIPEX-SP3232ECA
U8
T1IN
T2IN
R1OUT
R2OUT
T1OUT
T2OUT
R1IN
R2IN
V+
V-
GND
C1+
C1-
C2+
C2-
J11
RTS
J12
DTR
J13
P1
SUB-D9 FEMALE
RS232
DSR
Rx_PC
RTS
Tx_PC
CTS
DTR

3. Troubleshooting

3.1 MCU not starting or operating in a reliable way

Possible root cause	I/O	External Code	Internal Code
POWERS and GND delivered to the device	Input	- Must be stables - Monitor power supplies - Check if GND is properly supplied to device	
XTA2 pin	Output	- Monitor XTAL2 to see if the oscillator has started and is working properly. Check if your crystal is not an overtone part.	
RST pin	I/O	- If RST pin is not correctly driven, MCU is not properly reset. - If the device does not have an internal POR, read application note: “how to calculate the capacitor of the reset input of a C51 microcontroller” (doc 4284)” - If an external Brown-out device is used, an intermediate resistor or diode must be implemented between RST pin and the Brown-out device	
EA pin	Input	- Must be connected to GND	- Must be connected to VCC, directly or through a 10K resistor. - MCU may not work properly, if this pin is left floatting
ALE pin	Output signal	- This signal is used to clock the Least Significant Byte into the address latch - the frequency of this signal enables to guess the frequency that the core runs at. (See “Relationship between oscillator and ALE frequencies” on page 11.)	- Not used. - Must be left unconnected in normal operation - If ALE is not disabled by firmware, the frequency of this signal enables to guess the frequency that the core runs at. See “Relationship between oscillator and ALE frequencies” on page 11.)
PSEN pin	Output signal	- This signal is used to strobe the external program memory when the MCU fetches the code byte. - Monitor ALE and PSEN pins to get the status of the MCU. (See “Microcontroller status” on page 13.)	- Not used. - Must be left unconnected in normal operation - If ALE is not disabled by firmware, monitor ALE and PSEN pins to get the status of the MCU. (See “Microcontroller status” on page 13.)
P0	I/O port	Port 0 serves as a multiplexed address/data bus. It emits the low byte of the Program Counter (PCL) as an address, and then goes into a float state awaiting the arrival of the code byte from the Program Memory	Can be used as a general purpose I/O port. In this case external pull-up’s must be provided.
P2	I/O port	Port 2 emits the high byte of the Program Counter (PCH)	Can be used as a general purpose I/O port. No external pull-up’s are needed as this port owns internal pull-up’s
HSB set to maximum security		Does not work	No impact
Device is damaged		Try another device	

3.2 In-System Programming does not work

Possible root cause	External Code	Internal Code
MCU is not working in ISP mode	NOT APPLICABLE	Apply the hardware condition. See “In-System Programming (ISP)” on page 14. and read the device’s bootloader datasheet.
MCU does not work properly		Monitor power supplies, XTAL2, RST, EA, ALE, PSEN (See “MCU not starting or operating in a reliable way” on page 19.)
Device is damaged		Try a new or another device

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