Atmel AT02865: RF Layout with Microstrip

Atmel Wireless

Features

- Practical PCB design techniques for wireless ICs
- Controlled impedance layout
- 50Ω unbalanced transmission lines
- 100Ω balanced transmission lines
- 2.4GHz, 915MHz, 868MHz systems
- Layout for ZigBee®, IEEE®802.15.4, Bluetooth®, Wi-Fi systems
- Connecting to baluns
- PCB stack-up
- Production quality controls

Description

Poor layout can seriously degrade wireless performance. This application note outlines practical microstrip layout techniques to connect wireless microcontrollers with baluns and antennas. Unbalanced and balanced (differential) microstrip techniques are discussed for 4-layer PCBs using FR-4. Other design topics include PCB stack-up and ground layer practice, QA and PCB production strategies.

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1. Background

Wireless microcontrollers use Radio Frequency (RF) transmission lines to connect to antennas. At radio frequencies the Printed Circuit Board (PCB) is a complex circuit element and should not be compromised. This connection needs to be efficient to deliver strong RF power and receive clean signals. Although most PCB designs using wireless MCUs are relatively small compared to the RF wavelength, the Characteristic Impedance (Z_0) of the transmission line still impacts signal quality. Modern integrated circuits and PCB fabrication techniques impose practical constraints that are usually overlooked in individual datasheets and need to be harmonized by the astute design engineer.

2. 50Ω Unbalanced Microstrip

The microstrip technique has been used for decades. This technique uses the trace width and dielectric thickness to control the Z_0 of RF transmission lines on Printed Circuit Boards (PCB). There are many microstrip calculators available on the internet and included in RF modeling software. Specific recommendations are beyond the scope of this paper, but the reader is encouraged to obtain a microstrip calculator for both unbalanced and balanced (differential) microstrip.
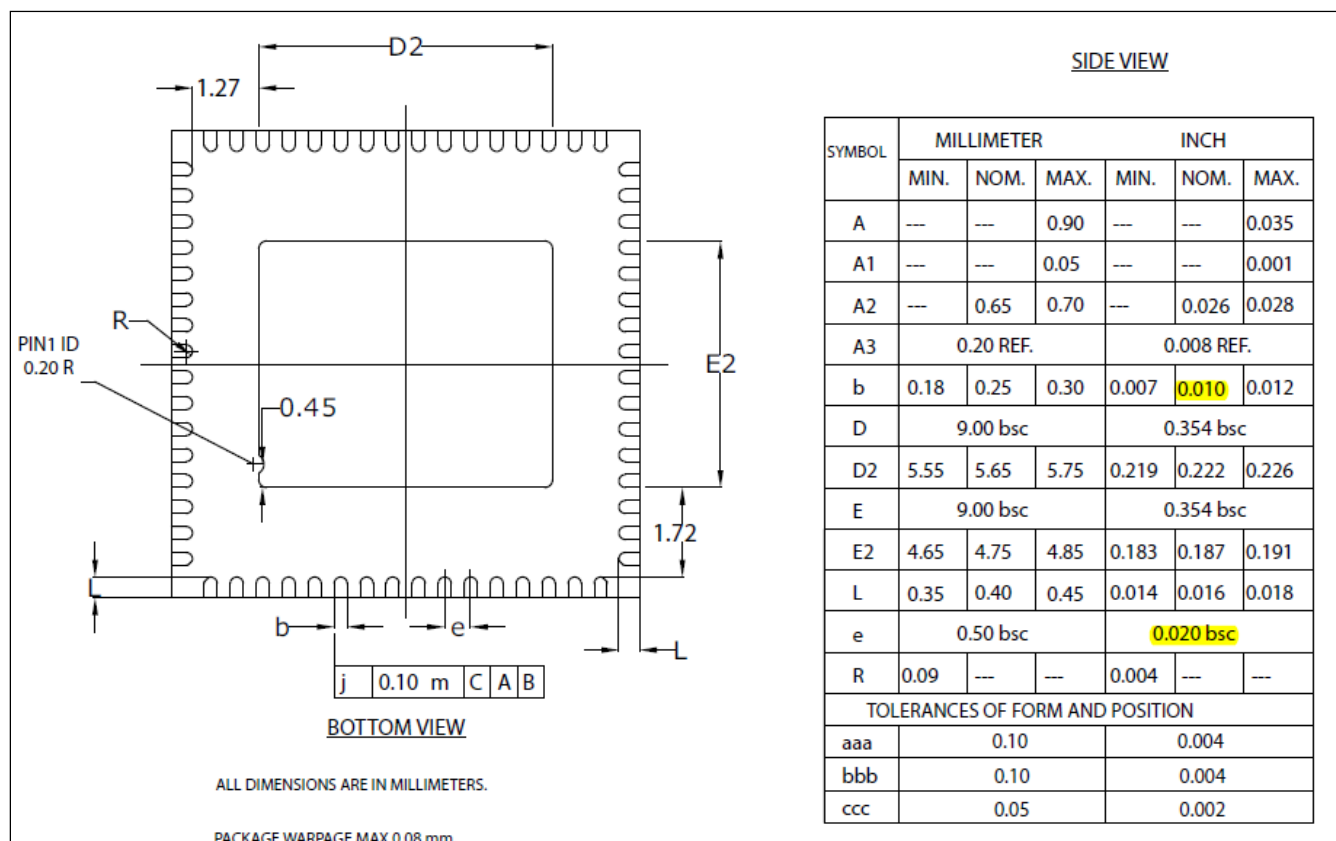
Figure 2-1.   Classic Microstrip Model.
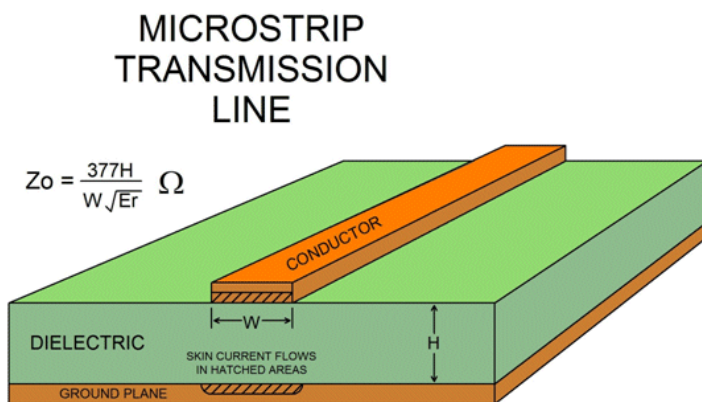
50Ω unbalanced transmission lines are common in the RF world. Most connectors and interfaces are 50Ω. Devices such as antennas, bandpass filters, SMA connectors, RF power amplifiers and RF switches all use 50Ω unbalanced connections. For practical PCB design using FR-4 dielectric and ISM frequencies (2450, 915 and 868Mhz) a trace-width to dielectric-thickness ratio of 2 to1 results in approximately 50Ω Z_0. This 2:1 rule of thumb scales within practical limitations of PCB dimensions and can be verified with a microstrip calculator.

To define the microstrip dimensions, the overarching constraint of layout is the pin-pitch, or pin-to-pin distance, of the IC package. See dimension "e" in Figure 2-2. Also note; the pin-width, dimension "b", is 10 mils. These dimensions cannot be changed.

Figure 2-2. Pin-pitch Dimensions.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.90	---	---	0.035
A1	---	---	0.05	---	---	0.001
A2	---	0.65	0.70	---	0.026	0.028
A3	0.20 REF.			0.008 REF.		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	9.00 bsc			0.354 bsc		
D2	5.55	5.65	5.75	0.219	0.222	0.226
E	9.00 bsc			0.354 bsc		
E2	4.65	4.75	4.85	0.183	0.187	0.191
L	0.35	0.40	0.45	0.014	0.016	0.018
e	0.50 bsc			0.020 bsc		
R	0.09	---	---	0.004	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

SIDE VIEW

BOTTOM VIEW

ALL DIMENSIONS ARE IN MILLIMETERS.

PACKAGE WARPAGE MAX 0.08 mm.

Also, to a lesser degree the component sizes constrain the layout. For example, using 20 mil traces and 0402 components has a nice clean fit. It would be impractical to use huge 120 mil traces and 62 mil (1.5mm) dielectric with 0402 SMT components. This is why 4-layer microstrip is a preferred technique for tighter layouts. Some designs require 2-layer stack-ups to reduce cost; these cases are more suitable for Coplainer Waveguide (CPW) transmission lines.

3.   100Ω Balanced Microstrip

One of the commonly overlooked specifications of wireless ICs is the 100Ω balanced output. Balanced outputs are commonly used by IC designers because they have inherently better signal-to-noise ratio and better CMRR, reduced emissions, reduced second-order harmonics and the use of high-speed current steering in driver stages. It can be argued balanced transmission lines are better for long distance runs on PCBs too.

Figure 3-1.   AT86RF231 Datasheet Excerpt.
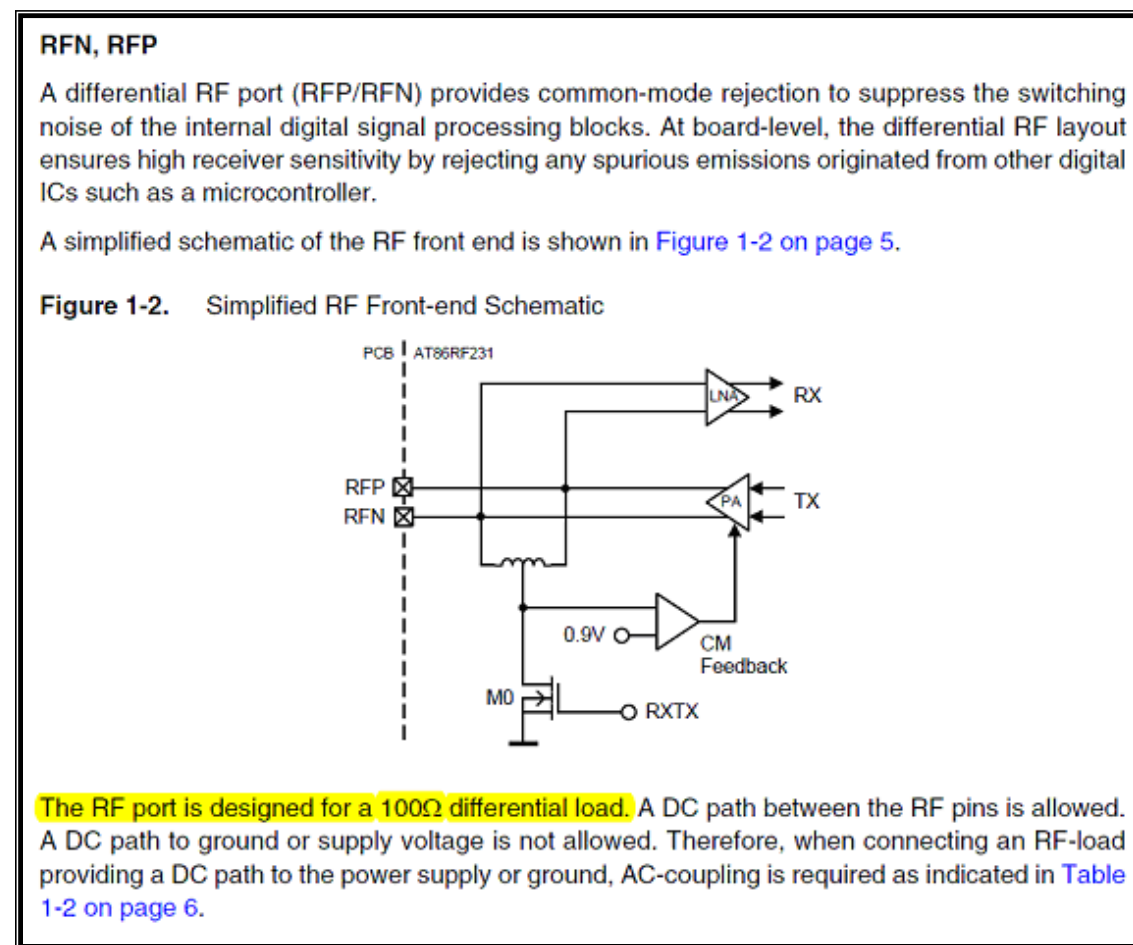
The use of balanced output requires the use of a balun to convert the 100Ω balanced signal to 50Ω unbalanced signal. The word balun is a contraction of balanced and unbalanced. Fortunately, there are many manufacturers of baluns for ISM frequencies. The PCB designer needs to preserve the 100Ω balanced impedance between the wireless MCU output and the balun, even if this distance is relatively short.

Again, the overarching constraint of the PCB layout is the pin-pitch of the wireless IC. This dimension cannot be changed. In the design example shown the pin-pitch is 20 mils and the pin width is 10 mils. This implies a center-to-center distance of 20 mils for the balanced traces.

Figure 3-2.   Balanced Differential Microstrip.
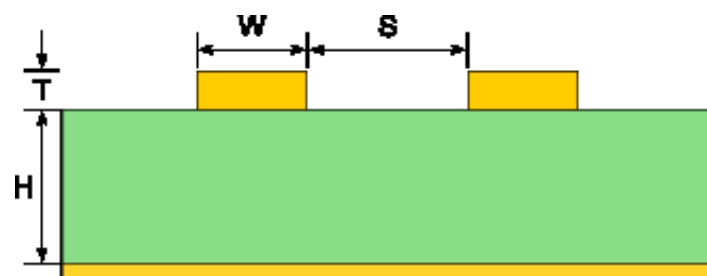
Experimentation with the microstrip calculator will show that balanced microstrip does not follow the 2:1 rule. The additional second line increases the capacitance lowering the impedance. To compensate we can reduce the width of the traces slightly. This will increase the inductance and raise the impedance back up. By skillfully adjusting the trace width and gap we can make the center-to-center distance fit the pin-pitch, while also meeting the 100Ω balanced objective and the 50Ω unbalanced objective simultaneously using the same 10 dielectric. In this way we can create 100Ω balanced lines for the IC to balun connection and 50Ω unbalanced lines for the balun to antenna connection.

For the design shown, the general rules for layout are 10 mil trace and 10 mil space. Observe the microstrip lines deviate slightly from the general trace-space rules. The nominal dimensions of the balanced microstrip between the IC and the balun are 12 mil trace, 8 mil gap and 11 mil dielectric. This results in a center-to-center distance of 20 mils and a prefect fit for the 20 mil pin-pitch of the QFN package. The nominal dimensions for the balanced microstrip between the balun and the antenna feed are 20 mil trace, 11 mil dielectric. The 20 mil trace mates smoothly to 0402 size components in the antenna matching network.

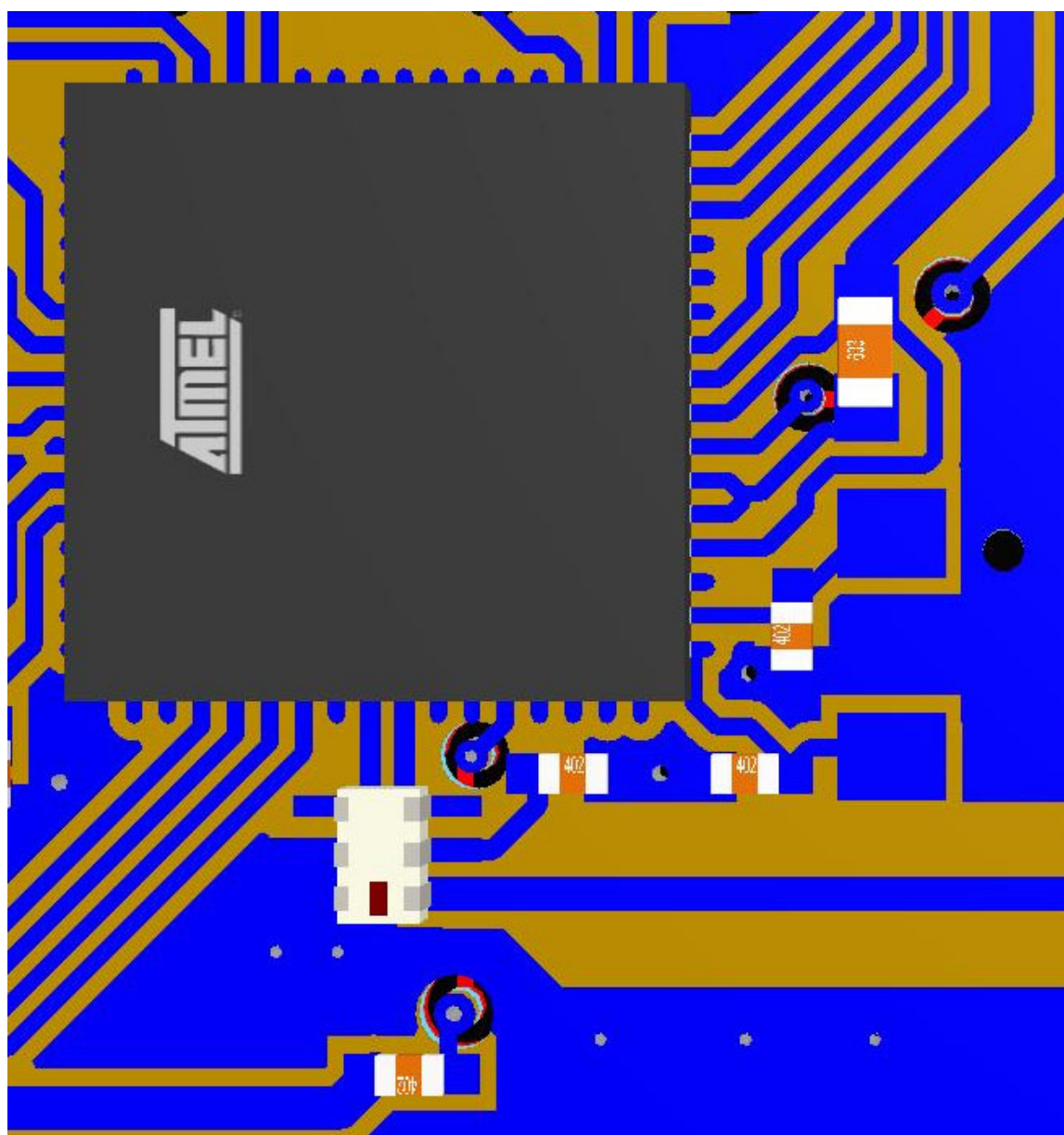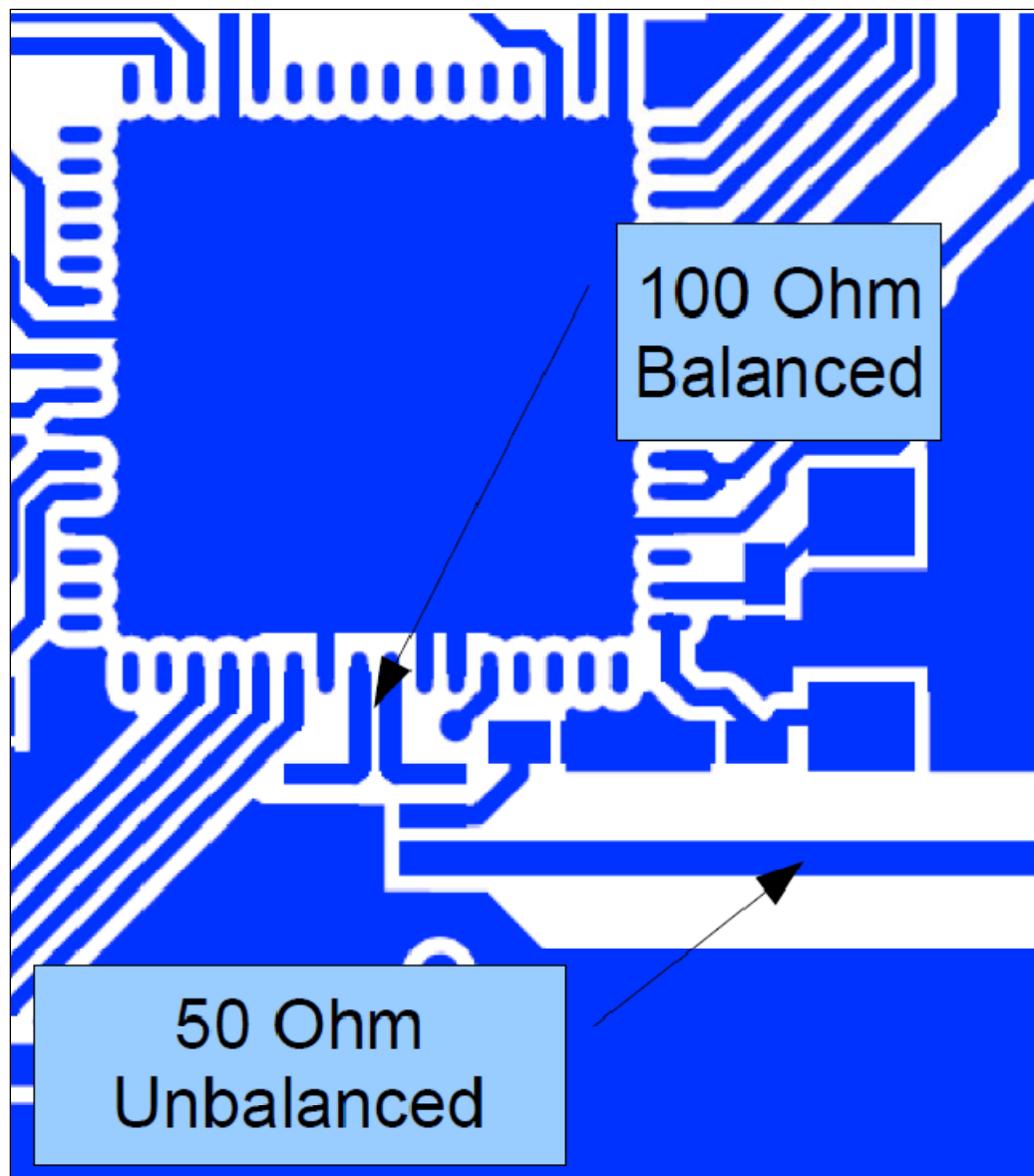**Figure 3-3.   3D Model of Microstrip Layout.**

Figure 3-4.   Metal Layer-1 Detail.

4.   Connecting to Baluns

Many baluns have pin-pitch that is better suited for 2-layer PCBs and CPW techniques. These should be avoided for Microstrip. Baluns with tighter pin-pitch work better because pin spacing has better alignment with the wireless IC.

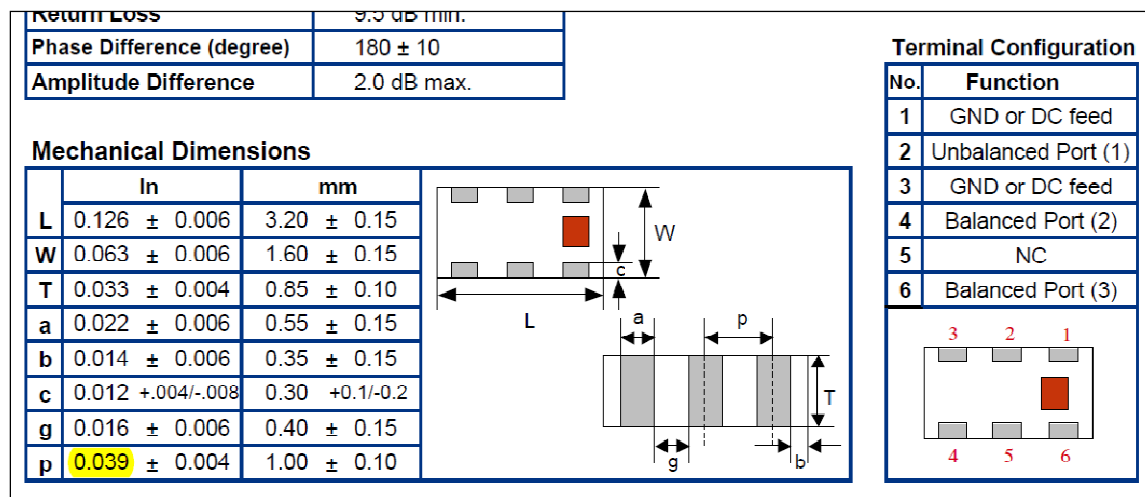**Figure 4-1. Distance Between Balanced RF Ports in 80 mils. Not Recommended for 4-layer Layout.**
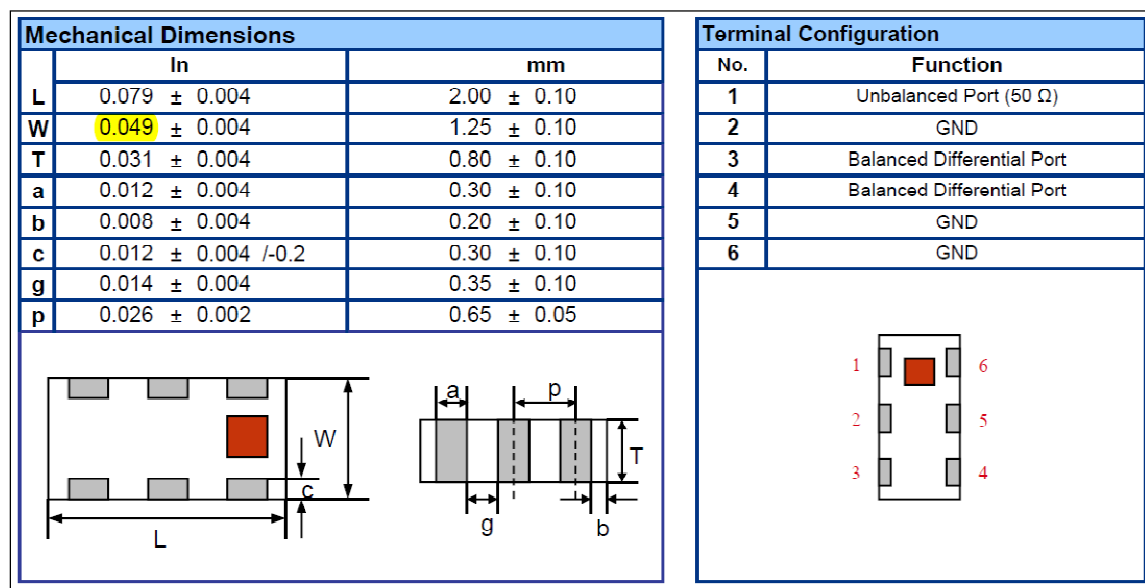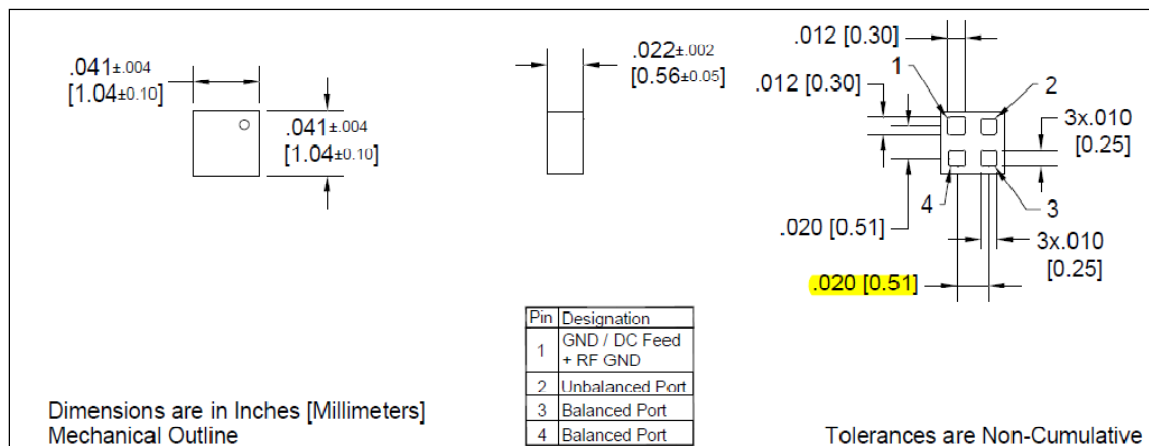
Return Loss	9.5 dB min.	
Phase Difference (degree)	180 ± 10	
Amplitude Difference	2.0 dB max.	

Mechanical Dimensions

	In	mm
L	0.126 ± 0.006	3.20 ± 0.15
W	0.063 ± 0.006	1.60 ± 0.15
T	0.033 ± 0.004	0.85 ± 0.10
a	0.022 ± 0.006	0.55 ± 0.15
b	0.014 ± 0.006	0.35 ± 0.15
c	0.012 +.004/-.008	0.30 +0.1/-0.2
g	0.016 ± 0.006	0.40 ± 0.15
p	0.039 ± 0.004	1.00 ± 0.10

Terminal Configuration

No.	Function
1	GND or DC feed
2	Unbalanced Port (1)
3	GND or DC feed
4	Balanced Port (2)
5	NC
6	Balanced Port (3)

Figure 4-2. Balun Used in Example with Tighter Pin Spacing, but it is Not Ideal.

Mechanical Dimensions

	In	mm
L	0.079 ± 0.004	2.00 ± 0.10
W	0.049 ± 0.004	1.25 ± 0.10
T	0.031 ± 0.004	0.80 ± 0.10
a	0.012 ± 0.004	0.30 ± 0.10
b	0.008 ± 0.004	0.20 ± 0.10
c	0.012 ± 0.004 /-0.2	0.30 ± 0.10
g	0.014 ± 0.004	0.35 ± 0.10
p	0.026 ± 0.002	0.65 ± 0.05

Terminal Configuration

No.	Function
1	Unbalanced Port (50 Ω)
2	GND
3	Balanced Differential Port
4	Balanced Differential Port
5	GND
6	GND

Figure 4-3.   An Attractive Balun Package with 20 mil Pin Spacing.

Additionally, some baluns include DC blocking and some do not. Usually, DC blocking is used on 50Ω systems at some point in the signal chain. This allows the use of ground referenced test equipment and prevents output shorting. In the design shown the balun includes DC blocking. If we were using a non-blocking balun, then we would place DC blocking caps in the balanced lines per the datasheet recommendation. These components would be placed side-by-side to keep the mirrored structure of the balanced conductors.

5.   Putting it Together with the Stack-up

The PCB stack-up is the third variable in the microstrip equation. The 2:1 rule of thumb suggests a dielectric of 10 mils works with the 20 mil transmission line. This would be impractically thin for a two layer PCB, but it works well for a 4-layer (of more) PCB.

In a 4-layer PCB, Layer-1 (top) is used for the RF transmission lines. Layer-2 is used for the RF ground plane. Usually PCBs are symmetrically constructed therefore Layer-3 should be a plane and Layer-4 (bottom) signal traces. Layer-3 can be a power plane, or a partitioned hybrid plane. Layer-4 can be general purpose signal traces, just not RF transmission lines.

If the design requires more layers, they can be inserted in the middle between Layer-2 and the old Layer-3. Or, if the 10 mil dielectric is too thick for dense routing in other areas, blank sub-layers can be used in the RF area as long as the total dielectric thickness between the transmission line and RF ground plane is correct for the transmission line trace width.

For the example board we used the following stack-up.

Table 5-1.   PCB Stack-up.

Item	Material	Thickness	Units	Tolerance	Signal/function
1	SOLDERMASK	1.00	mil	±10%	
2	PLATING	0.20	mil	±50%	
3	1 OZ CU	1.40	mil	±10%	LAYER 1, RF SIG
4	PREPREG	11.00	mil	±10%	DILECTRIC
5	1 OZ CU	1.40	mil	±10%	LAYER 2, RF GND
6	CORE	32.00	mil	±20%	FILLER
7	1 OZ CU	1.40	mil	±10%	LAYER 3, GP SIG3

| 8 | PREPREG | 11.00 | mil | ±10% | DILECTRIC |
9	1 OZ CU	1.40	mil	±10%	LAYER 4, GP SIG4
10	PLATING	0.20	mil	±50%	
11	SOLDERMASK	1.00	mil	±10%	
12	TOTAL PCB	62.00	mil	±10%	OVERALL THICKNESS

If possible designers should not route signals near RF sections or under the microstrip ground plane, but this is not always possible. Layout is the art of compromise. Routing signals under the Layer-2 RF ground plane is low-risk for static control signals because RF only penetrates a few mircometers into the metal. High-speed signals (dv/dt) and high-current (di/dt) signals can couple into the RF system and should be separated from the RF signal area. Additionally power signals should be routed to avoid common impedance coupling.

6. Ground Planes and Microstrip

Mathematically the microstrip model assumes an infinite ground plane. In practice the bigger the RF ground plane the better. Designs that have ground planes less than ½ the wavelength will compromise the far field signal. At a minimum, the RF ground plane must lie directly underneath the transmission line and have a clear and unobstructed path to the balun, MCU IC and antenna launch areas. Watch out for thermal relief cartwheels and via clearances perforating the RF ground path. Many layout tools automatically generate gaps and holes that can ruin ground plane integrity and slip through Design Rule Checks (DRCs.) When in doubt, always check the fabrication outputs; the 'gerbers' or film.

Copper pour on Layer-1 with ground stitching vias is a common practice in RF layout. For microstrip designs the copper pour on layer-1 should be kept away from the transmission line. The underlying Layer-2 ground plane needs to be the dominant ground reference to minimize variables. A keep-away distance of 4x the dielectric thickness will reduce the parasitic effects of copper pour to less than 1%. In other words the gap between the microstrip transmission line and copper pour on layer-1 should be 40 mils or more.

Figure 6-1. Layer-1 Copper Pour with 40 mil Keep-away.

40 mils
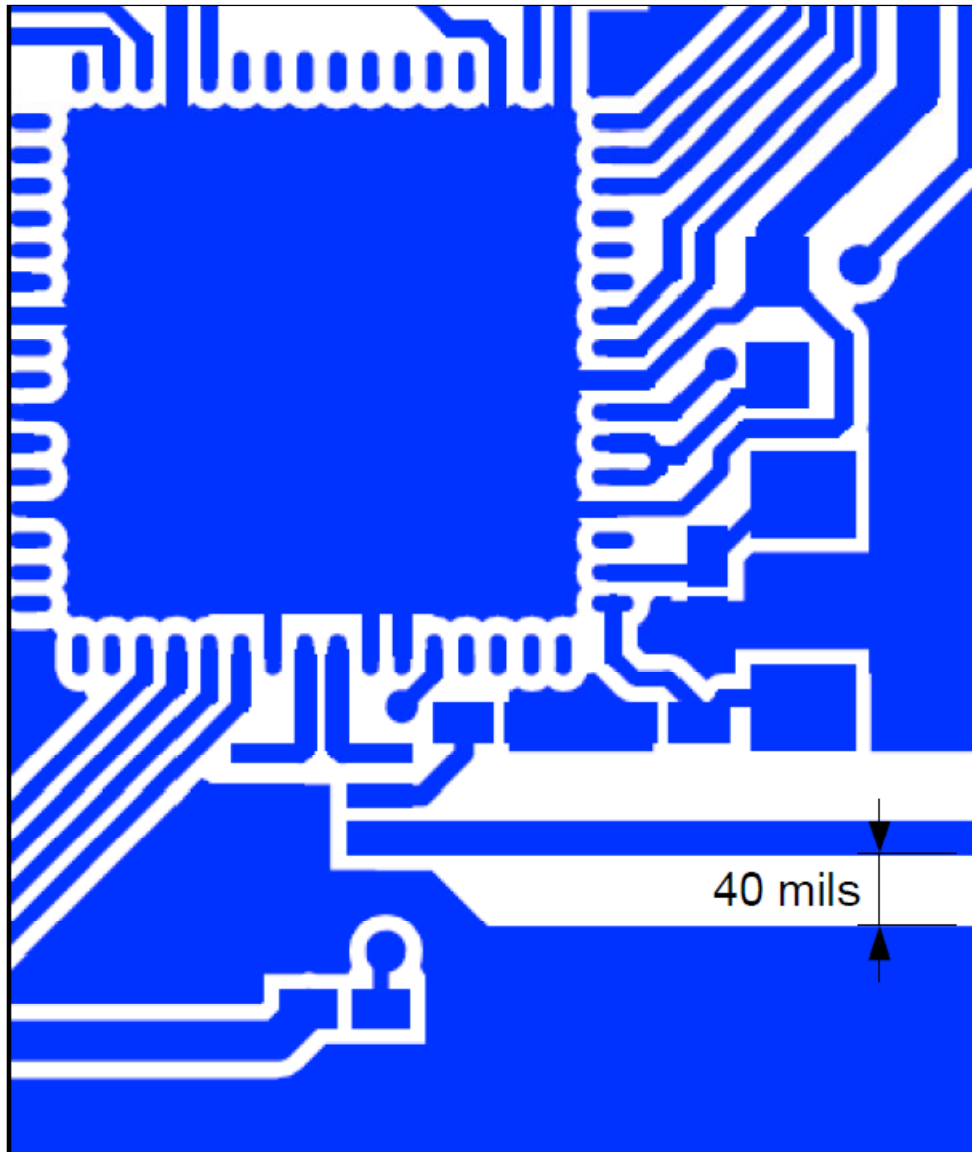
7. Working with the Fab House

Modern PCB fabrication houses work with controlled impedances on a regular basis. Most high-speed digital layouts and high-performance layouts use differential signals and controlled impedance. Designers need to work closely with the process engineer at the fab house to guarantee success with RF circuit boards. The process engineers will know what raw materials are available and the best value from their suppliers. For example, FR-4 laminates properties, common thicknesses use of prepreg or core for the dielectric. Additionally many fab houses have microstrip calculators based on their preferred DFM rules and laboratory characterization of materials. If the fab house does not have a good grasp of these topics, it's probably best to look for a different vendor.

8. Tolerance vs. Testing

To meet the controlled impedance goal for PCB design many designers start by tighten the material specifications; tighter control of the dielectric material, tighter dimension tolerances, tighter control of the stack-up thicknesses and lots of modeling. These methods are a valid solution however they can lead to much more expensive manufacturing costs. When designers start to specify PCB tolerances tighter than 10% the costs are inversely proportional. The dielectric coefficients of in-stock FR-4 maybe limited. In short, the result may not be satisfactory if the fab house is minding the details and oblivious to the overall goal.

Another approach is to specify nominal dimensions and let the fab house adjust the process, within reason, to hit the impedance requirements. Fab houses are familiar with microstrip structures and are usually very good at adjusting their recipes to suit. For verification have a test coupon evaluated using a Time-Domain Reflectometer (TDR). This will insure the 50Ω microstrip transmission line on the finished circuit board is correct. This approach allows different vendors to use their best processes and keeps the quality in check. The design example uses nominal dimensions in the layout and specifies the microstrip areas and impedances in the fabrication drawing.

Figure 8-1. Fabrication Drawing Excerpt.

```
7) Impedance Control:

a) Areas called out as NOTE 7A on fabrication drawing are 50 Ohm
Microstrip. Impedance Control 50 Ohms at 2440 MHz. Vendor shall provide
test coupon on PCB array and test report. The nominal dimensions of 50
Ohm microstrip traces are:

    * 20 mil wide transmission line on layer 1
    * RF ground plane on layer 2
    * 11 mil thick prepreg insulator between layer 1 and layer 2 with a
      dielectric constant of approximately 4.5.

Meeting the 50 Ohm tested impedance is the primary requirement.
These nominal dimensions and material properties can be adjusted (within
reason) by the vendor to meet a tested impedance of 50 Ohms +/- 10% on
the test coupon.

b) Areas called out as NOTE 7B on fabrication drawing are 100 Ohm
Differential Microstrip. Impedance Control 100 Ohms differential at 2440
MHz. Vendor shall provide test coupon on PCB array and test report. The
nominal dimensions of 100 Ohm differential microstrip traces are:

    * Two 12 mil wide transmission lines (differential pair) separated
      by an 8 mil gap on layer 1 (20 mil center to center)
    * RF ground plane on layer 2
    * 11 mil thick prepreg insulator between layer 1 and layer 2 with a
      dielectric constant of approximately 4.5.

Meeting the 100 Ohm tested impedance is the primary requirement. These
nominal dimensions and material properties can be adjusted (within
reason) by the vendor to meet a tested impedance of 100 Ohms
Differential +/- 10% on the test coupon.
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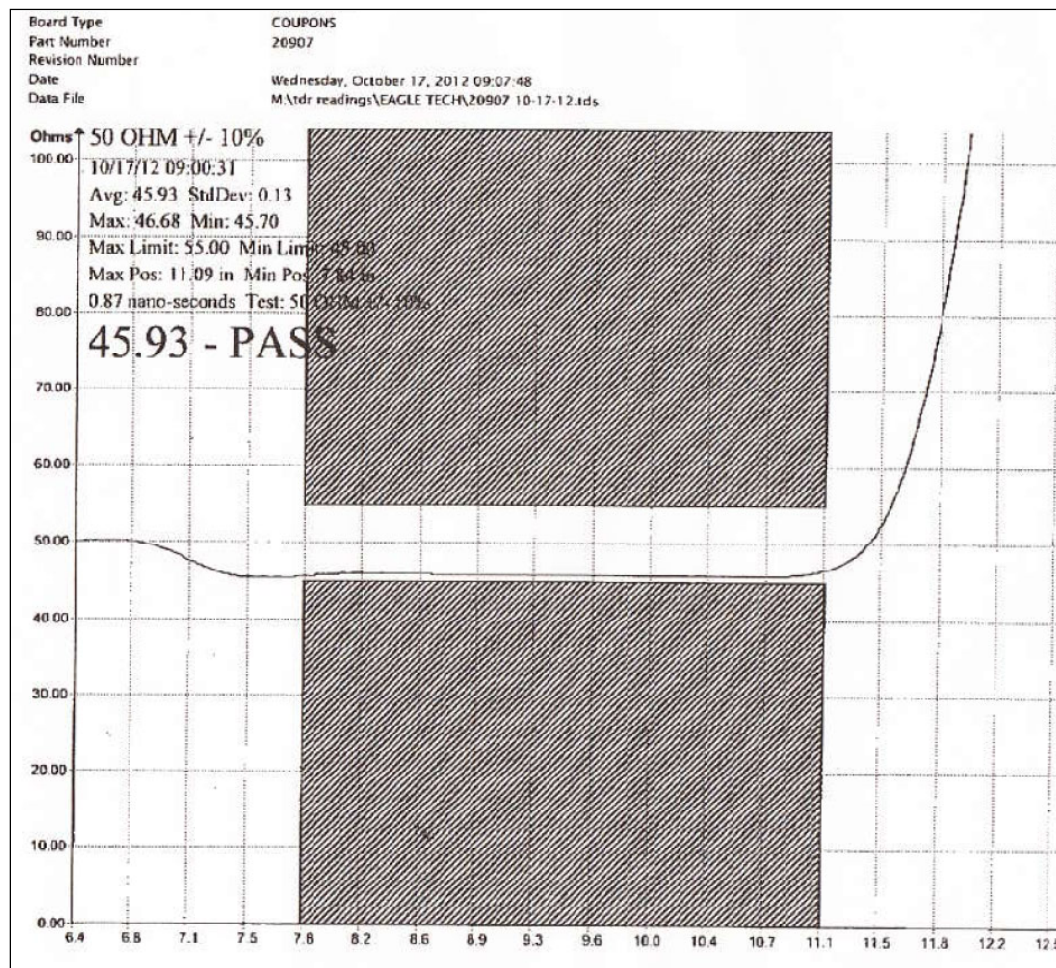
Figure 8-2. TDR Report here Z0 = 50Ω ±10%.

9. Conclusion

Microstrip is a very effective technique to get optimal RF performance from wireless ICs. With skillful planning both unbalanced and balanced microstrip can be implemented on the same PCB. This allows balanced signals from ICs and unbalanced signals from 50Ω antennas to be routed on the same layer of the same PC board. Microstrip works well on 4-layer PCBs and can be adapted to more layers if needed. Working with closely PCB fab house on material selection, tolerance and testing can help reduce costs and greatly improve yield.

10. Revision History

Doc. Rev.	Date	Comments
42131B	05/2013	Corrections in Chapter 2: Last sentence on page 3; included the "Note" as part of the last paragraph First sentence below Figure 2-2; added "constrain the layout" Corrections in Chapter 3: Last sentence on page 4; added "too" Last sentence above Figure 3-3; added "mates" / "series" replaced by "size" / "at" replaced by "in" Correction in Chapter 6: 5th sentence; added "gaps and holes" Correction in Chapter 8: New heading
42131A	04/2013	Initial document release

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