
USB331x USB Transceiver Layout Guidelines

INTRODUCTION

The USB331x provides the physical layer interface (PHY) in systems using Hi-Speed USB. Proper design techniques must be used in the printed circuit board (PCB) layout to maintain the signal integrity required for 480 Mbps operation. The USB331x is available in both a 24-pin QFN and a 25-ball BGA, and layout guidelines for both packages are provided in this application note.

Audience

This document is written for a reader that is familiar with hardware design and the USB 2.0 specification. The goal of this application note is to provide information on sensitive areas of the PCB layout.

Overview

The following recommendations are for a four layer PWB layout with a Microchip part. Our recommendations are not the only way to layout our 24-pin QFN and 25-ball BGA. PWB design engineers will have his/her own preference, and the implementation will be dependent on complexity and density of layout, PCB real estate, number and types of devices in circuit and the environment that the final product will reside in. For example, the PWB described in this application note has components on both sides of the board. A four layer board could be realized with components on one side only.

References

The following documents should be referenced when using this application note:

- Microchip USB331x Data Sheets
- Universal Serial Bus Specification Revision 2.0

GENERAL DESIGN GUIDELINES

This chapter provides guidelines for the sensitive circuits associated with the system application of the USB331x.

Controlled Impedance for USB Traces

The USB 2.0 specification requires that the USB DP/DM traces maintain a nominal 90 Ohms differential impedance $\pm 15\%$ (see USB specification Rev 2.0, paragraph 7.1.1.3 for more details). In this design the traces are 7 mil wide with line spacing of 7 mils. These numbers are derived for 5 mil distance from ground reference plane. For different dielectric thickness, copper weight or board stack-up, trace width and spacing will need to be recalculated. A continuous ground plane is required directly beneath the DP/DM traces and extending at least 5 times the spacing width to either side of DP/DM lines.

Maintain symmetry between DP/DM lines in regards to shape and length.

Single ended impedance is not as critical as the differential impedance. A range of 42 to 78ohms is acceptable (equivalently, common mode impedance must be between 21 Ohms and 39 Ohms).

FIGURE 1: EXAMPLE OF ROUTING DP/DM FROM BGA PKG TO TYPE B CONNECTOR

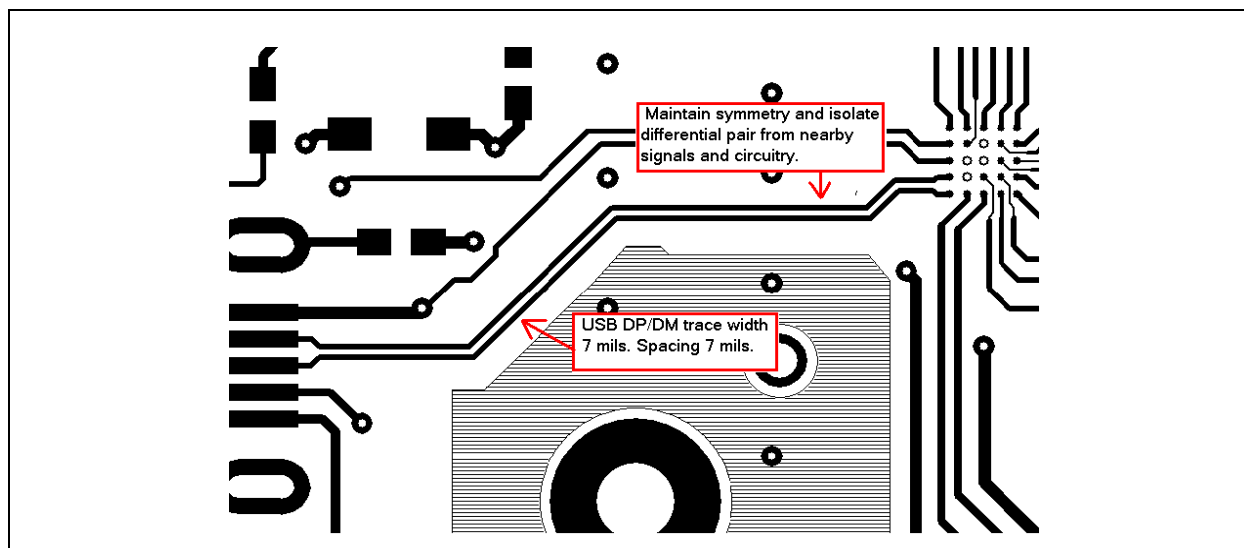


FIGURE 2: EXAMPLE OF ROUTING DP/DM FROM QFN PKG TO TYPE B CONNECTOR

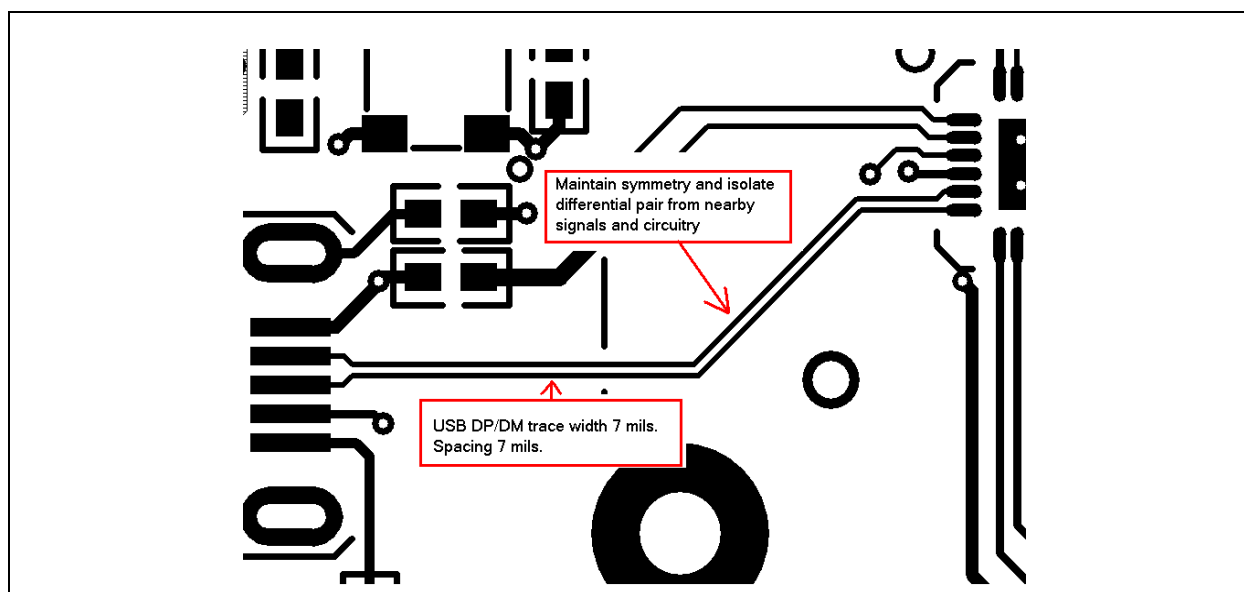


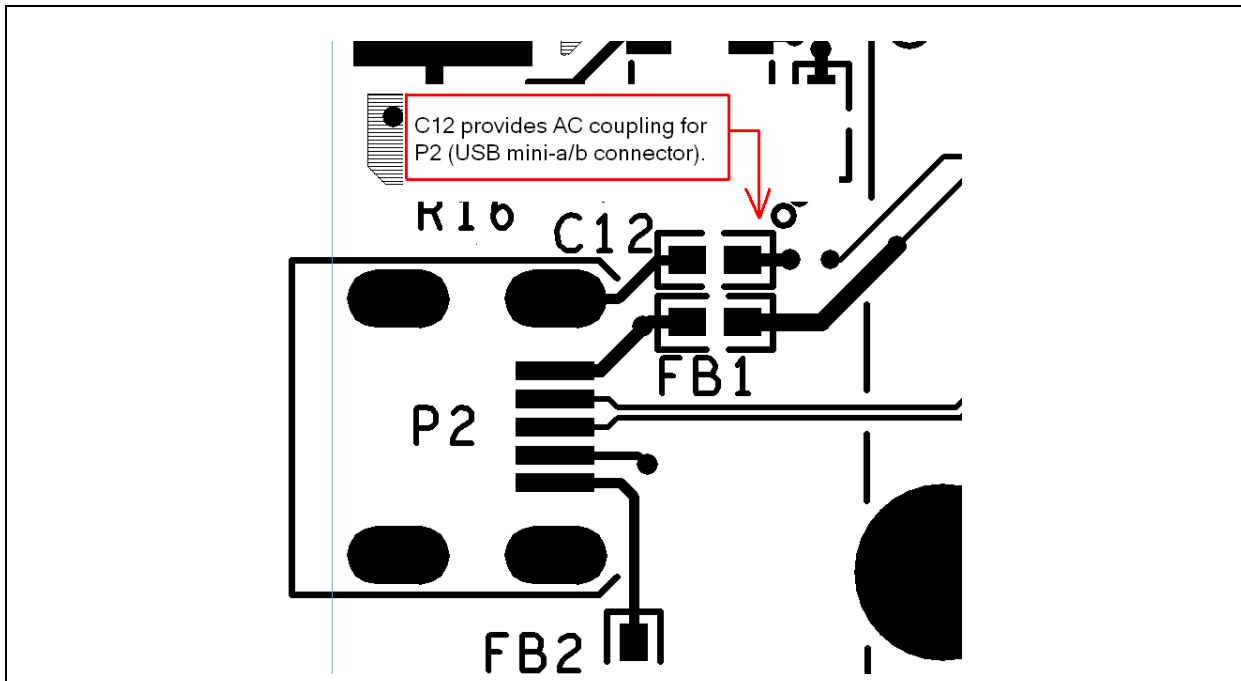
Figure 1 and Figure 2 show DP/DM traces with approximately equal trace length and symmetry. It is important to maintain a conductor width and spacing that provides differential and common mode impedances compliant with the USB specification. Use 45 degree turns to minimize impedance discontinuities.

Isolation of DP/DM Traces

The DP/DM traces must be isolated from nearby circuitry and signals. Maintain a distance of components to lines that is greater than or equal to 5 times the distance of the 7 mil spacing between the traces. Do not route differential pairs under components. Do not cross DP/DM lines with other PCB traces unless the traces are on the opposite side of the ground plane from DP/DM. Route DP/DM over solid GROUND plane with no ground plane splits under the traces.

Isolated Shielding on the USB Connector

FIGURE 3: CONNECTIONS TO SHIELD OF USB CONNECTOR



The USB331x fully supports USB On-the-Go (OTG). [Figure 3](#) shows the Mini-AB connector housing is DC isolated but AC coupled to the device ground. Industry convention is to ground only the host side of the cable shield. This is done to provide cable shielding while preventing possible ground currents from flowing in the USB cable if there happens to be a potential difference between the host and device grounds. If DC grounding is required replace C12 with a zero ohm resistor.

In OTG applications the shield may be DC grounded at both ends of the cable.

SPKR_L and SPKR_R/M

In USB audio mode, internal analog switches connect the DP pin to the SPKR_R/M pin and the DM pin to the SPKR_L pin. The system will then accommodate stereo/mono audio signaling over the USB cable. The internal analog switches can also be used to mux other USB traffic to the USB connector. Rules applied to DP/DM should also be applied to SPKR_L and SPKR_R/M traces. Refer to [Isolation of DP/DM Traces on page 2](#).

Because the SPKR_L and SPKR_R/M pins can be used carry audio signals to the user's audio components, the traces to these pins should follow layout guidelines to prevent noise from nearby circuitry and other signals. Noise induced onto these traces may cause undesirable glitches to reach.

FIGURE 4: EXAMPLE OF ROUTING SPKR TRACES FROM BGA PACKAGE

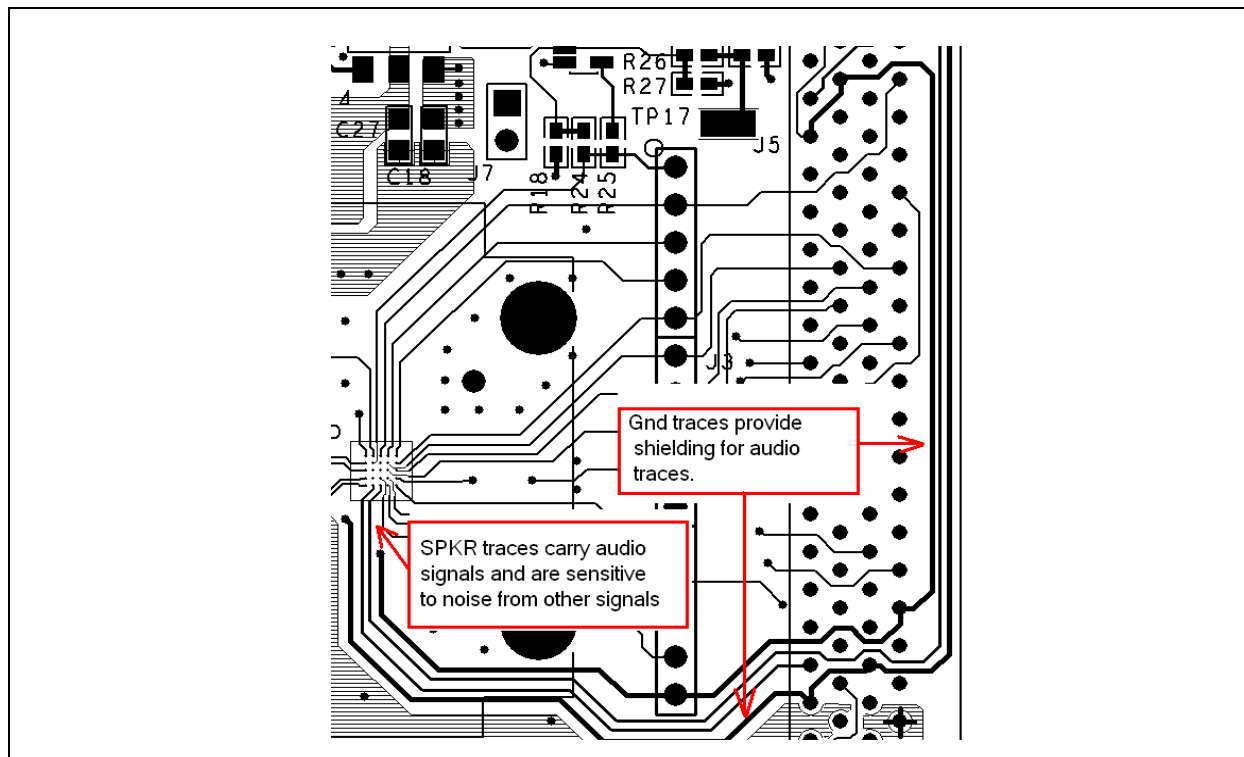
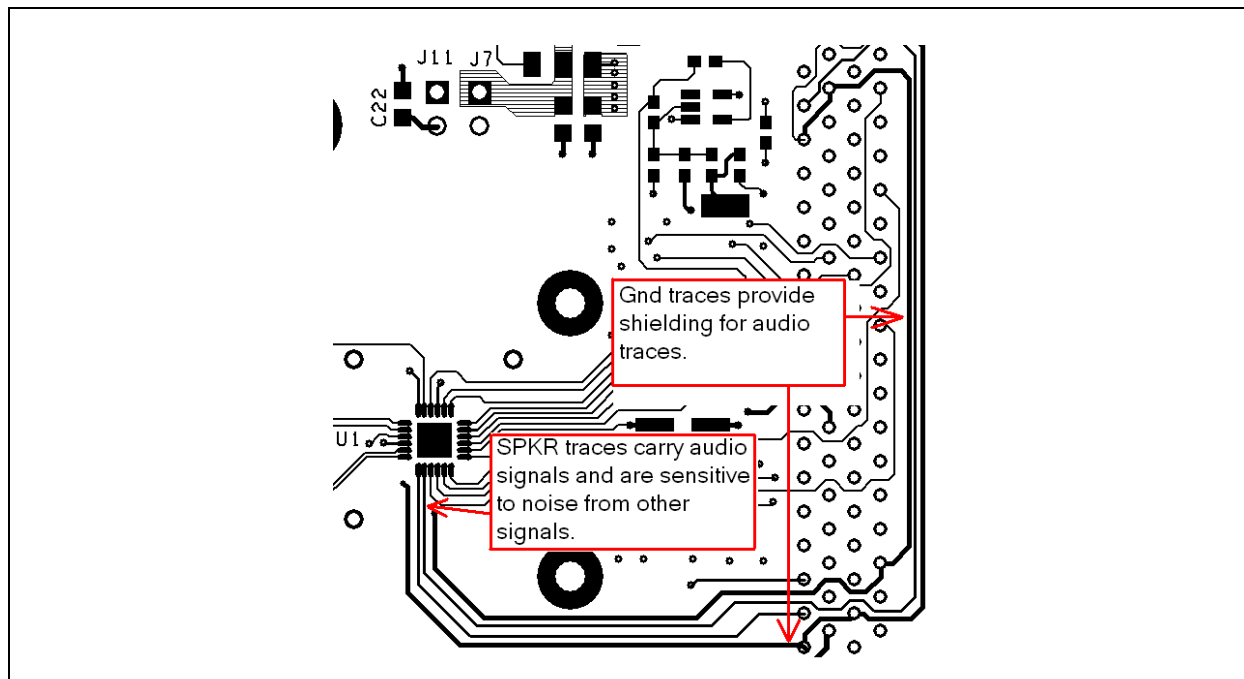


FIGURE 5: EXAMPLE OF ROUTING SPKR TRACES FROM QFN PACKAGE



RBIAS

The RBIAS resistor sets an internal current source reference. Thus, the RBIAS pin is a high impedance node and any noise induced on the RBIAS traces will directly impact internal current references and degrade eye-diagram quality. The RBIAS resistor should be placed close to the RBIAS pin and the ground return should be short and direct to VSS. Traces for the resistor should be very short and isolated from nearby traces if possible.

Power Supply Bypass Capacitors

Bypass capacitors should be placed close to respective supply pins of the USB331x for optimum power supply decoupling, and connected with short, wide traces. In [Figure 6](#) and [Figure 7](#), the top (dark) and bottom (red) circuit layers show bypass cap placement with respect to the USB331x's gnd pin. The USB331x evaluation board has bypassing directly under part, with return current paths tied to internal ground plane. Refer to data sheet for bypass cap values and ESR requirements.

FIGURE 6: C25 AND C23 ARE THE DECOUPLING FOR SUPPLY PINS FOR BGA PKG.

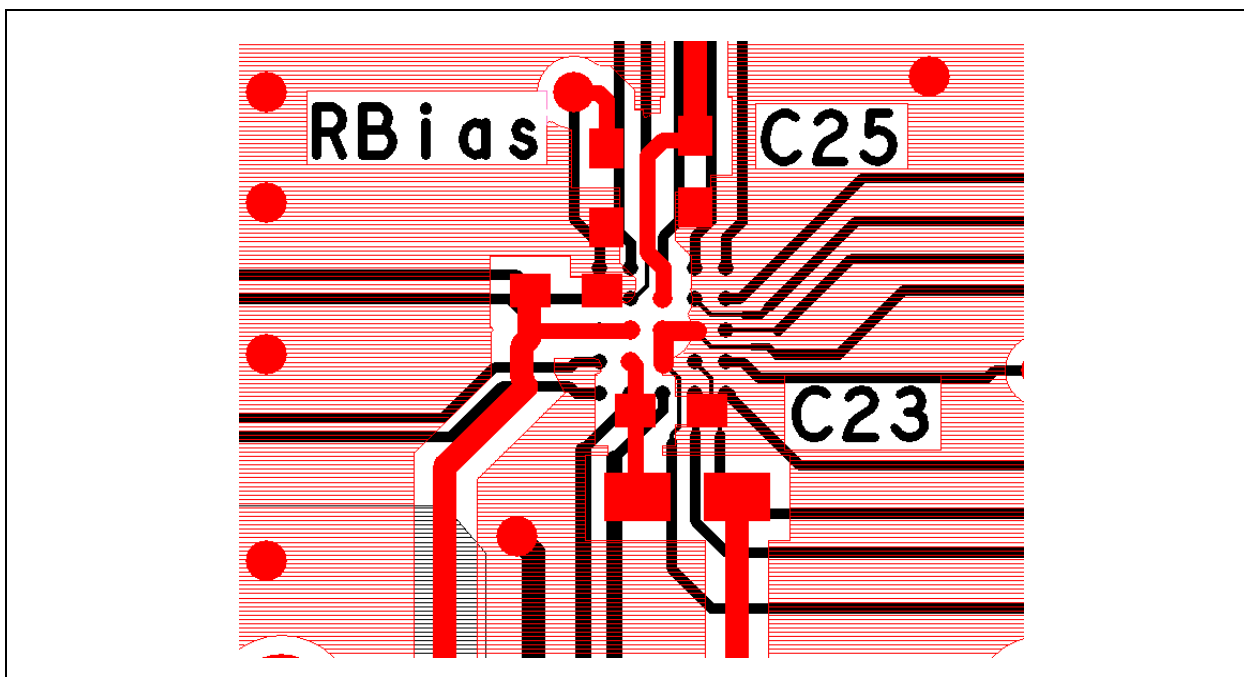
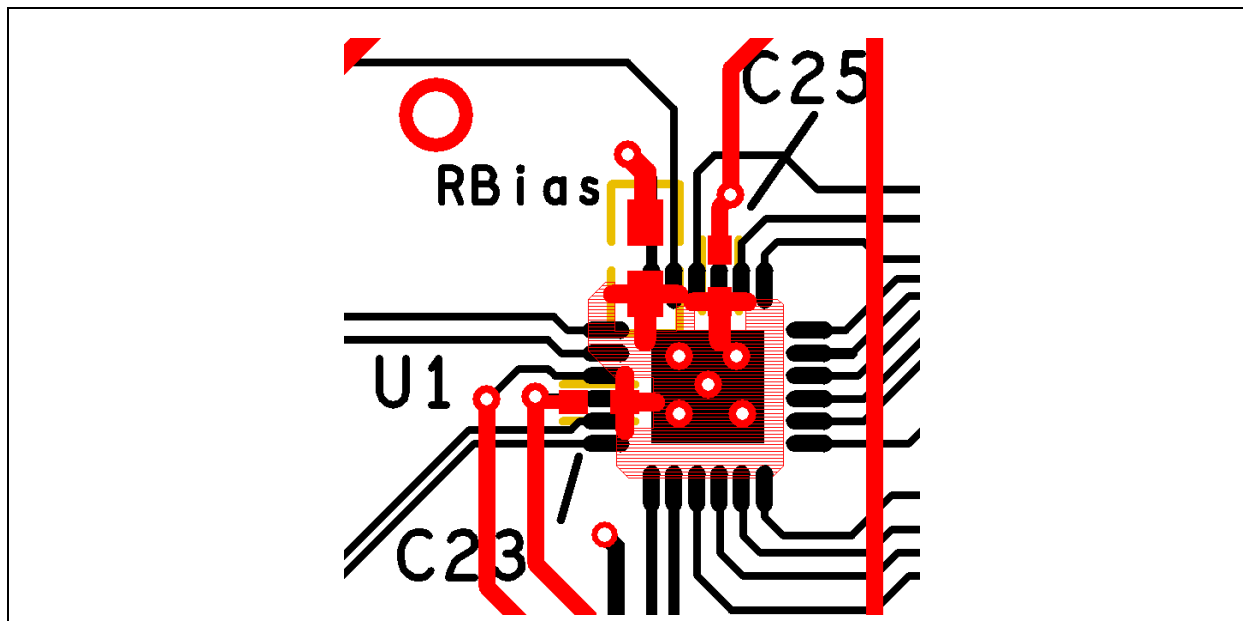


FIGURE 7: C25 AND C23 ARE THE DECOUPLING FOR SUPPLY PINS FOR QFN PKG.



VIAS in Ground Flag

The die pad (flag) in QFN package is 98 mils square. A 8 mil drilled via in a pattern of 2-1-2 has been used which resulted in excellent signal integrity performance. Ideally these vias would be plugged so that no solder will flow through which would result in less than ideal solder connection to flag.

Crystal Placement and Routing (USB3313 Only)

In addition to the general guidelines for the USB331x family of USB transceivers, the USB3313 requires some additional guidelines for the crystal placement and routing.

- The crystal should be placed as close as possible to the USB3313.
- The lengths of signals XO and XI should be kept as short as possible (<1", if possible).
- Capacitors on XI and XO should be placed as close as possible to the crystal. (For applications using a ceramic resonator, capacitors are not required.)

APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00002947A (02-06-19)	REV A replaces SMSC version Rev. 0.1 (11-26-12)	
Rev. 1.0 (11-26-12)	Document release	

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