PIC16F716

FLASH Memory Programming Specification

This document includes the programming specifications for the following devices:

- PIC16F716

1.0 PROGRAMMING THE PIC16F716

The PIC16F716 is programmed using a serial method. The Serial mode will allow the PIC16F716 to be programmed while in the user's system. This allows for increased design flexibility. This programming specification applies to PIC16F716 devices in all packages.

1.1 Hardware Requirements

The PIC16F716 requires one power supply for VDD (5.0V) and one for VPP (12V).

1.2 Program/Verify Mode

The Program/Verify mode for the PIC16F716 allows programming of user program memory, special locations used for ID, and the configuration word.

TABLE 1-1: PIN DESCRIPTIONS (DURING PROGRAMMING): PIC16F716

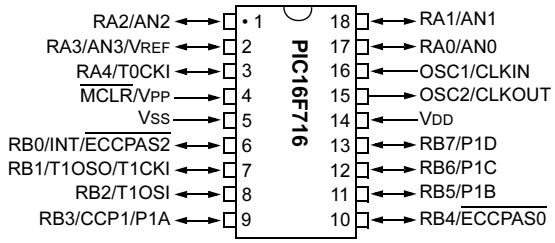
Pin Name	During Programming		
	Function	Pin Type	Pin Description
RB6	ICSPCLK	I	Clock input – Schmitt Trigger input
RB7	ICSPDAT	I/O	Data input/output – Schmitt Trigger input
$\overline{MCLR}$/VPP	Program/Verify mode	P(1)	Program Mode Select
VDD	VDD	P	Power Supply
VSS	VSS	P	Ground

Legend: I = Input, O = Output, P = Power

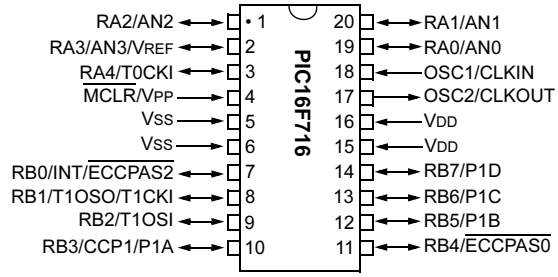
Note 1: In the PIC16F716, the programming high voltage is internally generated. To activate the Program/Verify mode, high voltage of IIHH current capability (see Table 5-1) needs to be applied to $\overline{MCLR}$ input.

FIGURE 1-1: PIN DIAGRAMS FOR PIC16F716

18-pin PDIP, SOIC, Windowed CERDIP



20-pin SSOP



2.0 PROGRAM MODE ENTRY

2.1 User Program Memory Map

The user memory space extends from 0x0000 to 0x1FFF. In Program/Verify mode, the program memory space extends from 0x0000 to 0x3FFF, with the first half (0x0000-0x1FFF) being user program memory and the second half (0x2000-0x3FFF) being configuration memory. In user program space, the PC will increment from x0000 to 0x1FFF then wrap back to 0x0000. In configuration memory space, the PC will increment from 0x2000 to 0x3FFF then wrap back to 0x2000 (not 0x0000). Once in configuration memory, the highest bit of the PC stays a '1', thus always pointing to the configuration memory. The only way to point to user program memory is to reset the part and re-enter Program/Verify mode as described in Section 2.3.

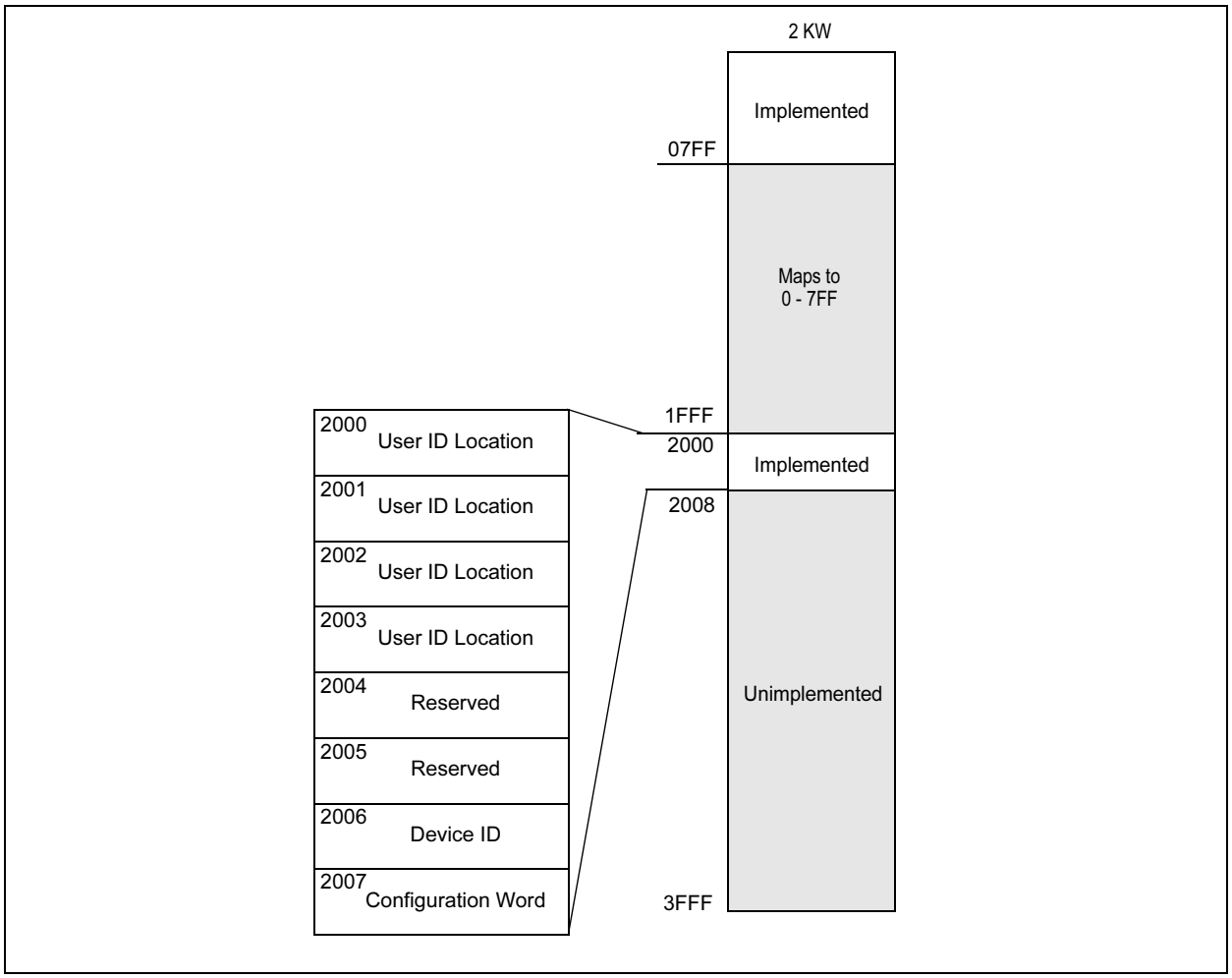
In the configuration memory space, 0x2000-0x2007 are physically implemented. However, only locations 0x2000 through 0x2003, and 0x2007 are available. Other locations are reserved.

2.2 User ID Locations

A user may store Identification Information (ID) in four User ID locations. The User ID locations are mapped in [0x2000: 0x2003]. It is recommended that the user use only the seven Least Significant bits (LSb) of each User ID location. The User ID locations read out normally, even after code protection is enabled. It is recommended that User ID location is written as "xx xxxx xbbb bbbb" where 'bbb bbbb' is User ID information.

The 14 bits may be programmed, but only the LSb's are displayed by MPLAB® IDE. xxxx's are "don't care" bits as they won't be read by MPLAB® IDE.

FIGURE 2-1: PROGRAM MEMORY MAPPING



2.3 Program/Verify Mode

The Program/Verify mode is entered by holding pins ICSPCLK and ICSPDAT low while raising VDD pin from VIL to VDD. Then raise VPP from VIL to VIHH. Once in this mode, the user program memory and configuration memory can be accessed and programmed in serial fashion. Clock and data are Schmitt Trigger inputs in this mode.

The sequence that enters the device into the Programming/Verify mode places all other logic into the RESET state (the MCLR pin was initially at VIL). This means that all I/O are in the RESET state (hi-impedance inputs).

The PIC16F716 program memory may be written in two ways. The fastest method writes four words at a time to the program memory array. However, one-word writes are also supported for backward compatibility.

2.3.1 FOUR-WORD PROGRAMMING

The normal sequence for writing the program array is to load four words to sequential addresses, then issue a begin programming command. The PC must be advanced following the first three loads, but not advanced following the last program load until after the programming cycle. The programming cycle is started and timed externally. Then, the PC is advanced after the programming cycle. The cycle repeats to program the array. After writing the array, the PC may be reset and the array may be read back to verify the write. It is not possible to verify immediately following the write because the PC can only increment, not decrement. See Figure 2-11.

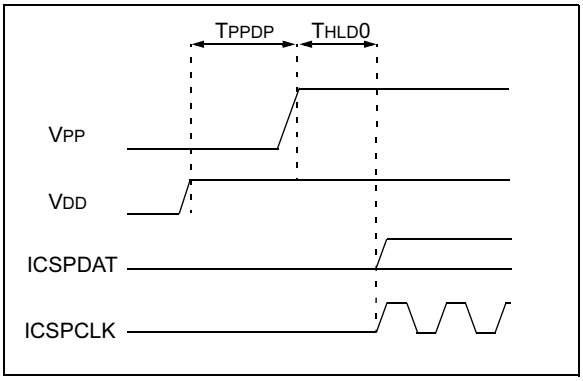
It is important that the PC is not advanced after the 4th word is loaded as the programming cycle writes the row selected by the PC <11:2>. If the PC is advanced, the data will be written to the next row.

2.3.2 ONE-WORD PROGRAMMING

The program memory may be written one word at a time to allow compatibility with some other PICmicro® FLASH devices. The one-word sequence loads a word, programs, verifies, and finally increments the PC. See Figure 2-10.

A device RESET will clear the PC and set the address to '0x0000'. The Increment Address command will increment the PC. The Load Configuration command will set the PC to 0x2000. The available commands are shown in Table 2-1.

FIGURE 2-2: ENTERING HIGH VOLTAGE PROGRAM/VERIFY MODE



2.3.3 SERIAL PROGRAM/VERIFY OPERATION

The ICSPCLK pin is used for clock input and the ICSPDAT pin is used for data input/output during serial operation. To input a command, the clock pin is cycled six times. Each command bit is latched on the falling edge of the clock with the LSb of the command being input first. The data must adhere to the setup (TSET1) and hold (THLD1) times with respect to the falling edge of the clock (see Table 5-1).

Commands that do not have data associated with them are required to wait a minimum of TDLY2 measured from the falling edge of the last command clock to the rising edge of the next command clock (see Table 5-1).

Commands that do have data associated with them (Read and Load) are also required to wait TDLY2 between the command and the data segment measured from the falling edge of the last command clock to the rising edge of the first data clock. The data segment, consisting of 16 clock cycles, can begin after this delay.

The first and last clock pulses during the data segment correspond to the START and STOP bits respectively. Input data is a don't care during the START and STOP cycles. The 14 clock pulses between the START and STOP cycles, clock the 14 bits of input/output data. Data is transferred LSb first.

During read commands, in which the data is output from the PIC16F716, the ICSPDAT pin transitions from the hi-impedance state to the low impedance output state at the rising edge of the second data clock (first clock edge after the START cycle). The ICSPDAT pin returns to the hi-impedance state at the rising edge of the 16th data clock (first edge of the STOP cycle). See Figure 2-5.

The commands that are available are described in Table 2-1.

TABLE 2-1: COMMAND MAPPING FOR PIC16F716

Command	Mapping (MSb … LSb)						Data
Load Configuration	x	x	0	0	0	0	0, data (14), 0
Load Data For Program Memory	x	x	0	0	1	0	0, data (14), 0
Read Data From Program Memory	x	x	0	1	0	0	0, data (14), 0
Increment Address	x	x	0	1	1	0	
Begin Programming	x	1	1	0	0	0	Externally Timed
End Programming	x	0	1	1	1	0	
Bulk Erase Program Memory	x	x	1	0	0	1	Internally Timed

2.3.3.1 LOAD CONFIGURATION

After receiving this command and the corresponding 14 bits of configuration data, the program counter (PC) will be set to 0x2000 and the input latch will contain the data (see Figure 2-3). Since 0x2000 is the first user ID location and 0x2007 is the configuration word address, the program counter must be incremented 7 times to access the configuration word latch. The following sequence is recommended when reprogramming the configuration word only:

- Send Load Configuration command with an unprogrammed data word (i.e., 0x3FFF).
- Send Increment Program Counter command seven times.
- Send Load Data For Program Memory command with the desired configuration word.
- Send Begin Programming command
- Wait TPROG then send End Programming command.
- Wait TDIS before the next action.

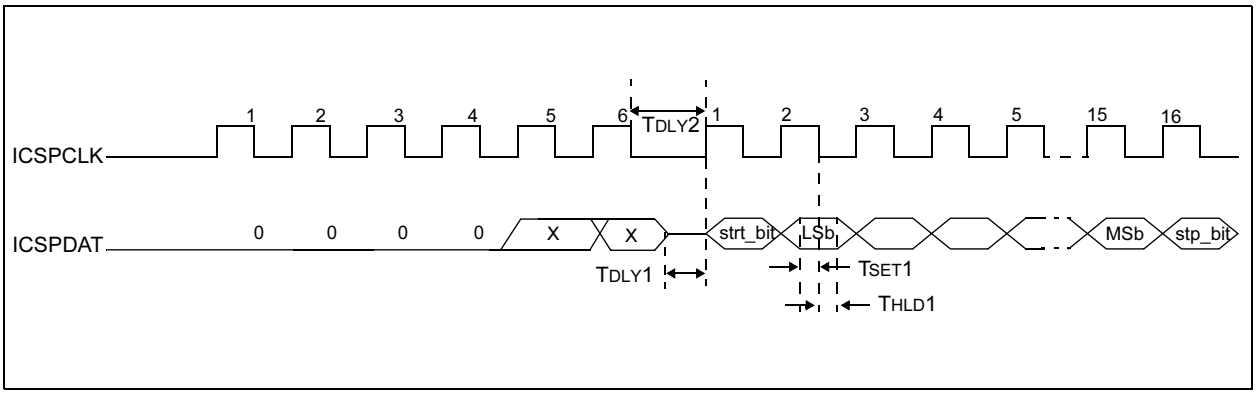
The following sequence may be used to program the 4 user ID locations and the configuration word:

- Send Load Configuration command with first word of user ID data
- Send Increment Program Counter command
- Send Load Data for Program Memory command with second word of user ID data
- Send Increment Program Counter command
- Send Load Data for Program Memory command with third word of user ID data
- Send Increment Program Counter command
- Send Load Data for Program Memory command with fourth word of user ID data
- Send Begin Programming command
- Wait TPROG then send End Programming command
- Wait TDIS then send Increment Address command 4 times
- Send Load Data for Program Memory commanders configuration word data
- Send Begin Programming command
- Wait TPROG then send End Programming command

Unlike program memory and user ID data which must start from the erased state before programming, the configuration word can be reprogrammed regardless of it's current state. The exception to this is the code protect bit ($\overline{CP}$) which can only be changed from '0' (protected) to '1' (unprotected) by issuing a Bulk Erase command.

After configuration memory is entered, the only way to get back to the user program memory is to exit the Program/Verify mode by taking $\overline{MCLR}$ low (VIL).

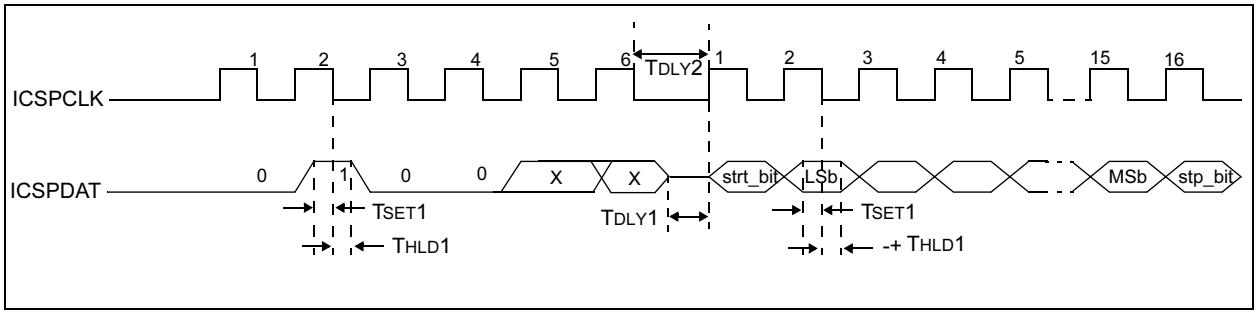
FIGURE 2-3: LOAD CONFIGURATION COMMAND



2.3.3.2 LOAD DATA FOR PROGRAM MEMORY

After receiving this command, the chip will load in a 14-bit “data word” when 16 cycles are applied, as shown in Figure 2-4.

FIGURE 2-4: LOAD DATA FOR PROGRAM MEMORY COMMAND

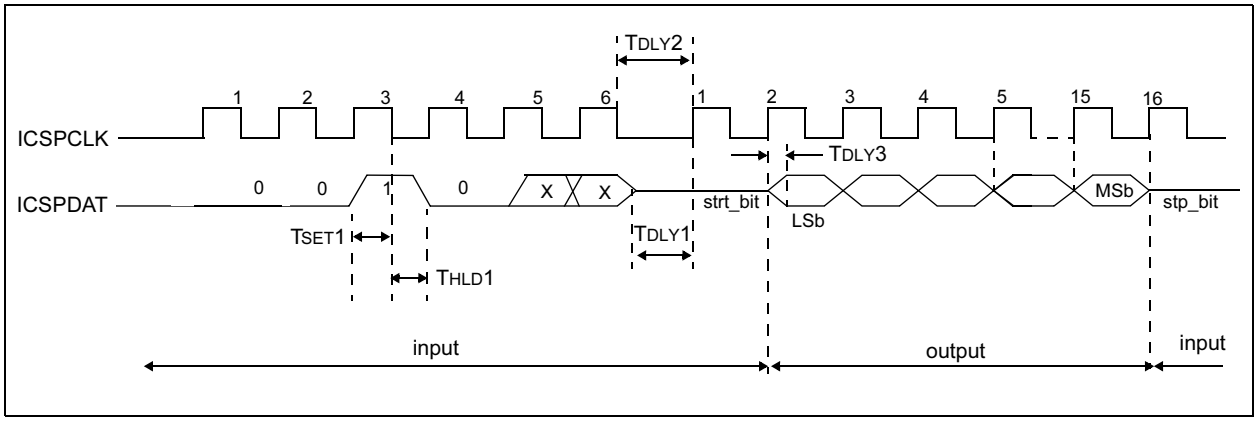


2.3.3.3 READ DATA FROM PROGRAM MEMORY

After receiving this command, the chip will transmit data bits out of the program memory (user or configuration) currently addressed, starting with the second rising edge of the clock input. The data pin will go into Output mode on the second rising clock edge, and it will revert to Input mode (hi-impedance) after the 16th rising edge.

If the program memory is code protected ($\overline{CP}$ = 0), the data is read as zeros.

FIGURE 2-5: READ DATA FROM PROGRAM MEMORY COMMAND

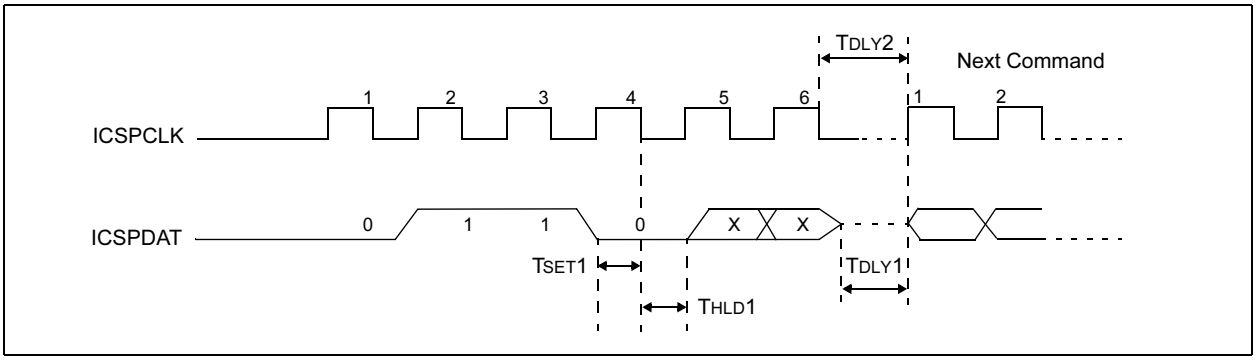


2.3.3.4 INCREMENT ADDRESS

The PC is incremented when this command is received. A timing diagram of this command is shown in Figure 2-6.

It is not possible to decrement the address counter. To reset this counter, the user must exit and re-enter Program/Verify mode.

FIGURE 2-6: INCREMENT ADDRESS COMMAND

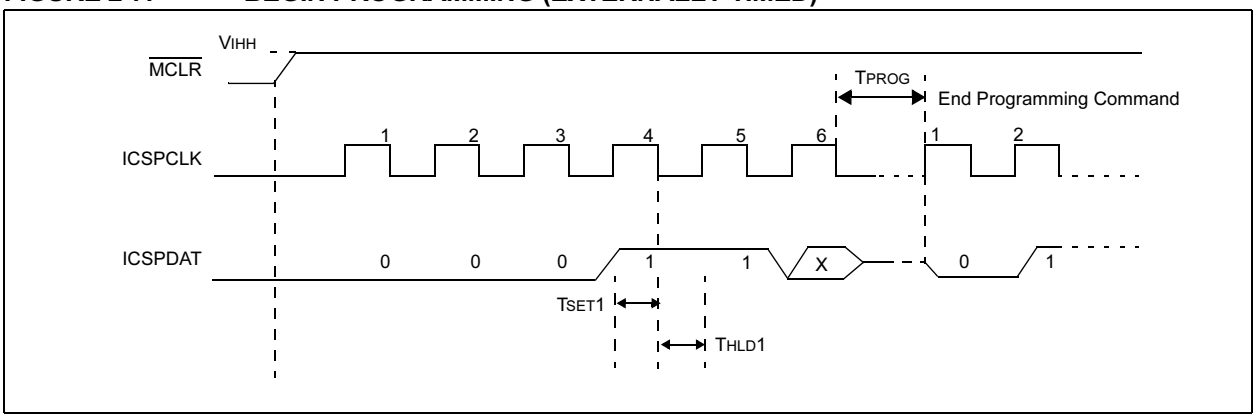


2.3.3.5 BEGIN PROGRAMMING (Externally Timed)

A Load command must be given before every Begin Programming command**.** Programming will begin immediately after the Begin Programming command is received and decoded. Programming requires (TPROG) time and is terminated using an End Programming command. This command programs the current location(s), no erase is performed.

When programming program memory, the word addressed is not erased before programming.

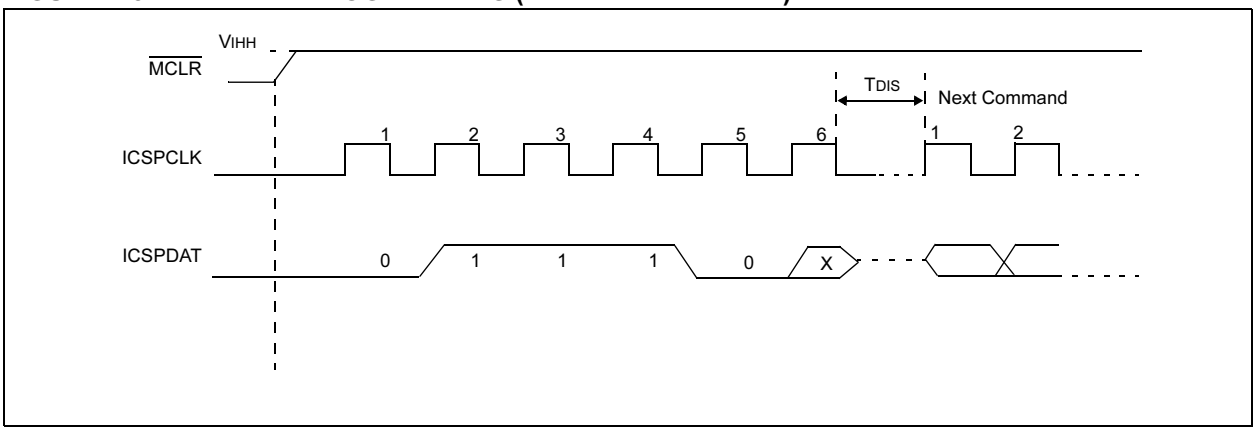
FIGURE 2-7: BEGIN PROGRAMMING (EXTERNALLY TIMED)



2.3.3.6 END PROGRAMMING

The End Programming command terminates the program process by removing the high programming voltage from the memory cells and resetting the data input latches to all '1's (erased state). A delay of TDIS (see Table 5-1) is required before the next command to allow the high programming voltage to discharge (see Figure 2-8.

FIGURE 2-8: END PROGRAMMING (EXTERNALLY TIMED)



2.3.3.7 BULK ERASE PROGRAM MEMORY

After this command is performed the entire program memory and configuration word is erased.

To perform a bulk erase of the program memory, user ID's and configuration word, the following sequence must be performed.

1. Perform a Load Configuration command.
2. Perform a Bulk Erase Program Memory command.
3. Wait TERA to complete bulk erase.

If the PC is pointing to the configuration program memory (0x2000 - 0x2007), then the program memory, configuration word, and user ID locations will all be erased. If the PC is in user memory space (0x0000 - 0x1FFF) only program memory and the configuration word will be erased.

FIGURE 2-9: BULK ERASE PROGRAM MEMORY COMMAND

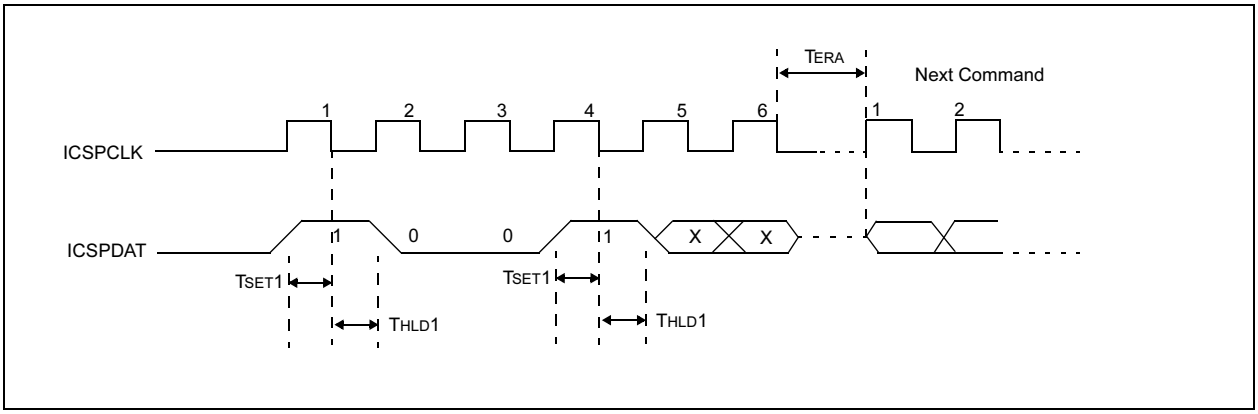


FIGURE 2-10: ONE-WORD PROGRAM FLOW CHART - PIC16F716 PROGRAM MEMORY

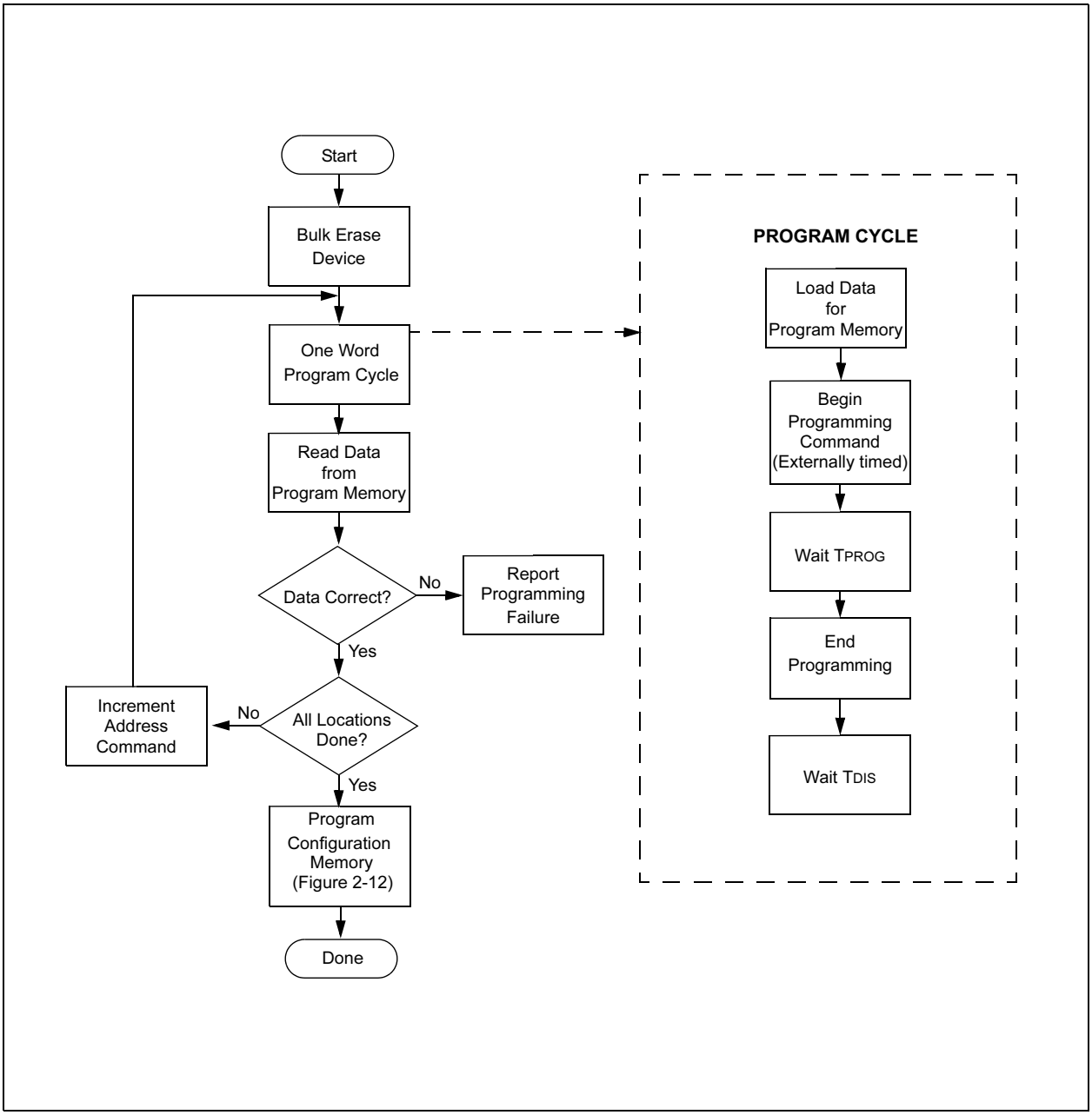


FIGURE 2-11: FOUR-WORD PROGRAM FLOW CHART - PIC16F716 PROGRAM MEMORY

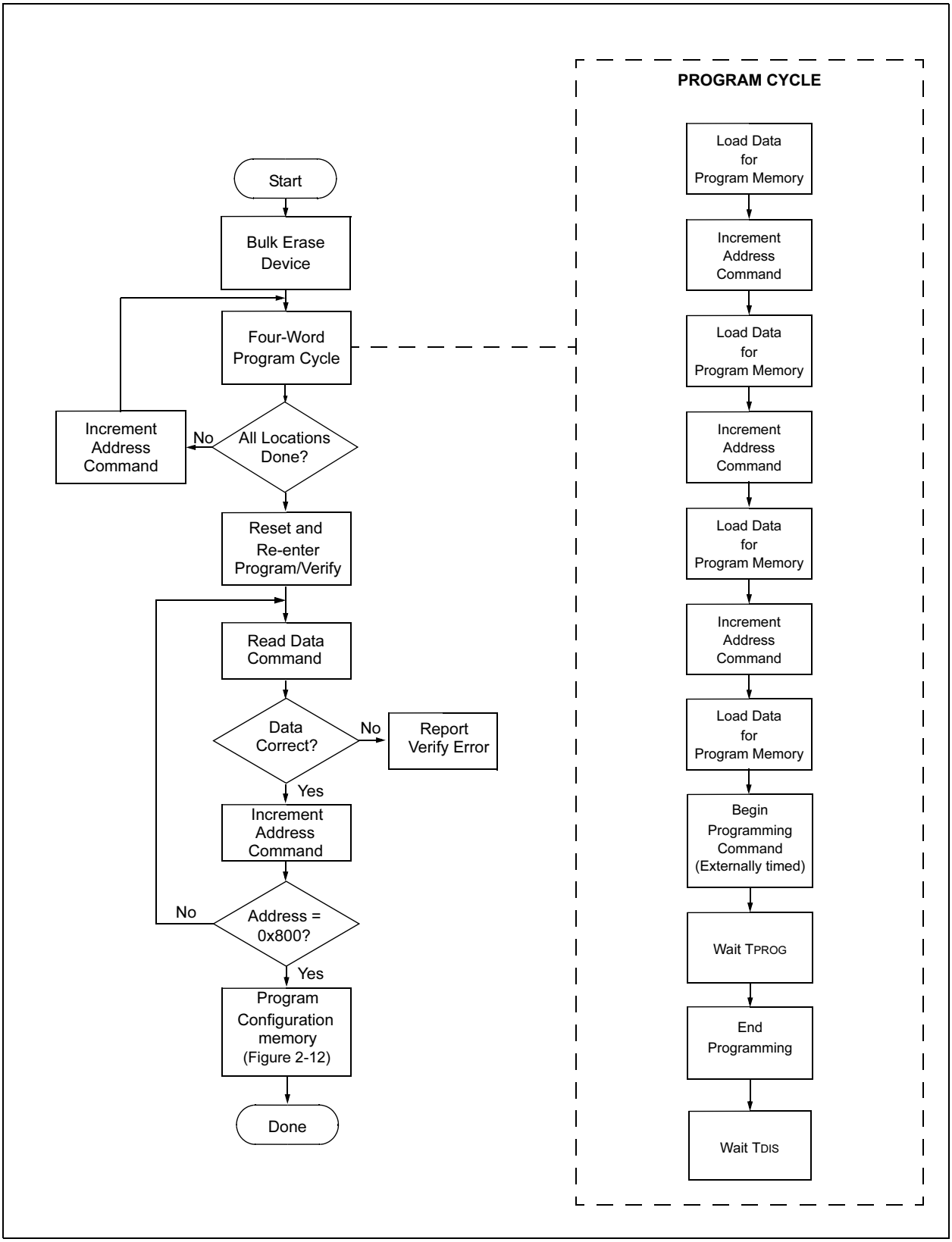


FIGURE 2-12: PROGRAM FLOW CHART - PIC16F716 CONFIGURATION MEMORY

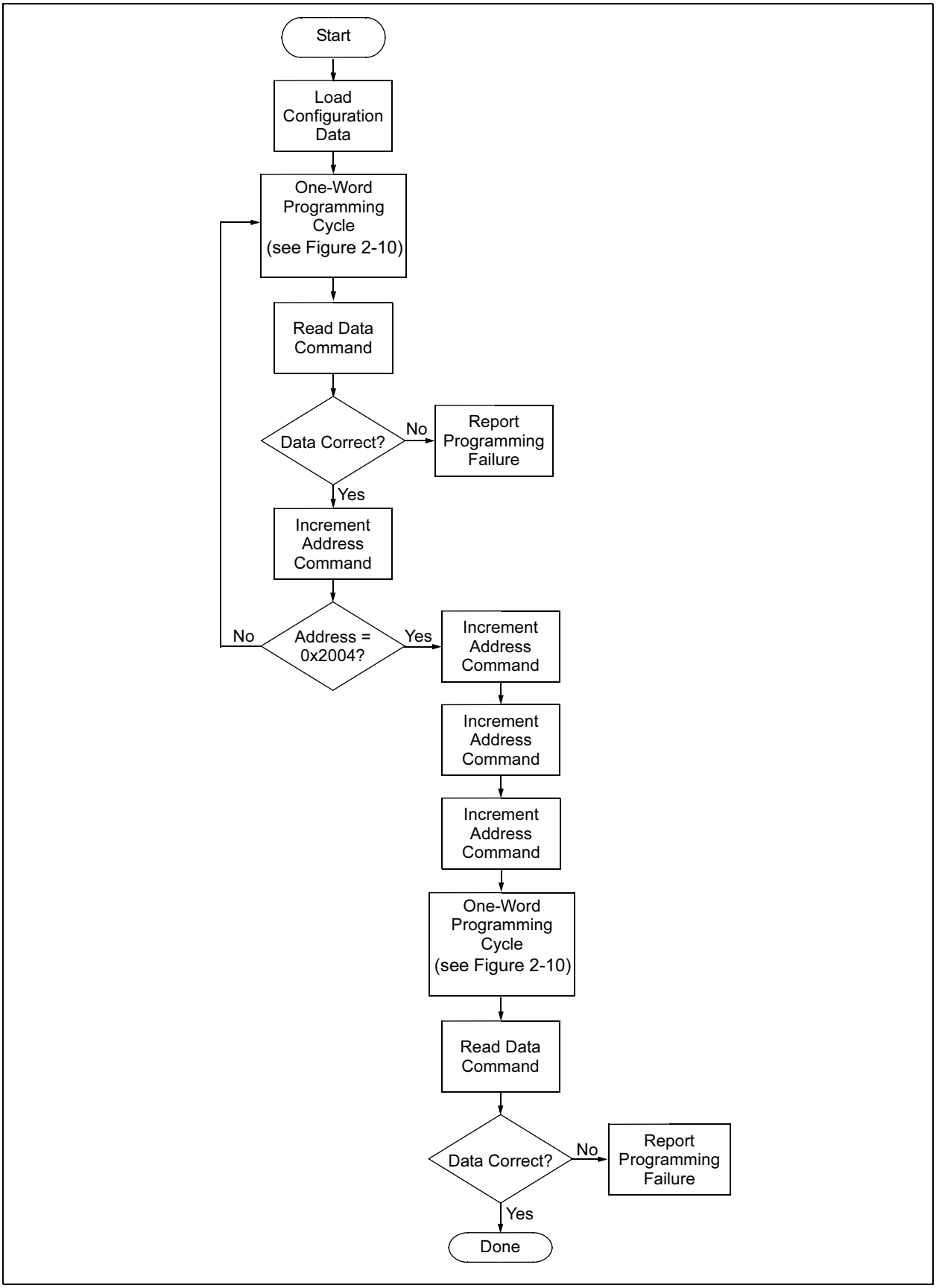


FIGURE 2-13: PROGRAM FLOW CHART - ERASE PROGRAM MEMORY, CONFIGURATION WORD & USER ID

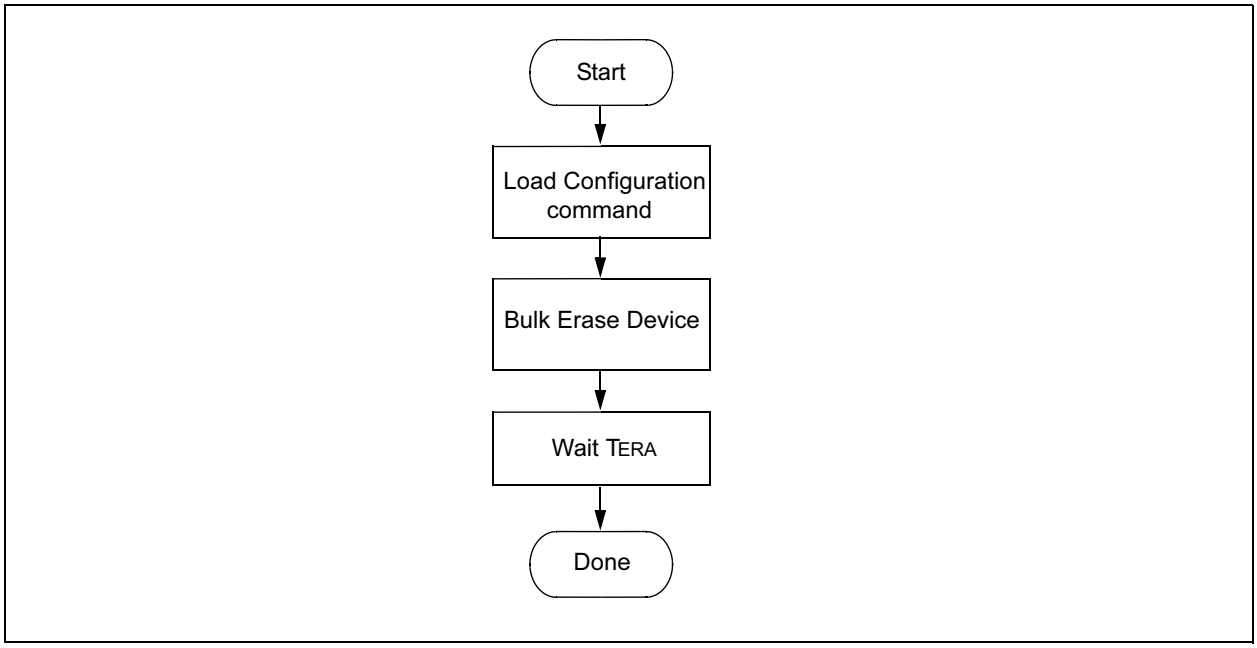
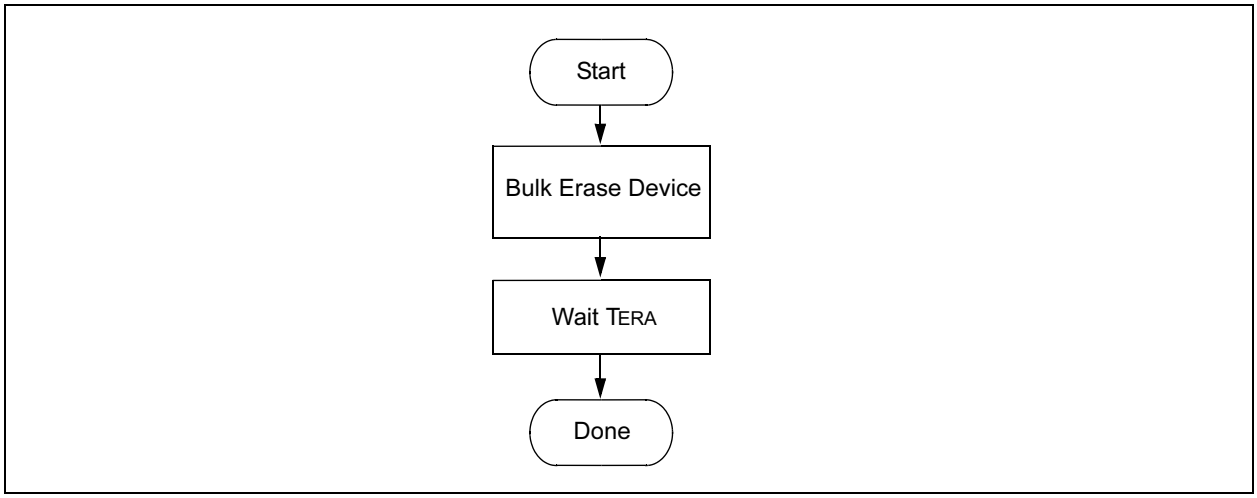


FIGURE 2-14: PROGRAM FLOW CHART - ERASE PROGRAM MEMORY & CONFIGURATION WORD



3.0 CONFIGURATION WORD

The PIC16F716 has several configuration bits. These bits can be programmed (reads '0'), or left unchanged (reads '1'), to select various device configurations.

REGISTER 3-1: CONFIGURATION WORD

R/P-1	U-1	U-1	U-1	U-1	U-1	R/P-1	R/P-1	U-1	U-1	R/P-1	R/P-1	R/P-1	R/P-1
$\overline{CP}$	—	—	—	—	—	BORV	BOREN	—	—	$\overline{PWRTE}$	WDTE	FOSC1	FOSC0
bit 13													bit 0

bit 13 **$\overline{CP}$**: Flash Program Memory Code Protection bit(2)
1 = Code protection off
0 = All program memory code protected

bit 12-8 **Unimplemented**: Read as '1'

bit 7 **BORV**: Brown-out Reset Voltage bit
1 = V_{BOR} set to 4.0V
0 = V_{BOR} set to 2.5V

bit 6 **BOREN**: Brown-out Reset Enable bit (1)
1 = BOR Reset enabled
0 = BOR Reset disabled

bit 5-4 **Unimplemented**: Read as '1'

bit 3 **$\overline{PWRTE}$**: Power-up Timer Enable bit(1)
1 = PWRT disabled
0 = PWRT enabled

bit 2 **WDTE**: Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0 **FOSC1:FOSC0**: Oscillator Selection bits
11 = RC oscillator
10 = HS oscillator: High speed crystal/resonator on OSC2/CLKOUT and OSC1/CLKIN
01 = XT oscillator: Crystal/resonator on OSC2/CLKOUT and OSC1/CLKIN
00 = LP oscillator: Low power crystal on OSC2/CLKOUT and OSC1/CLKIN

Note 1: Enabling Brown-out Reset does not automatically enable the Power-up Timer ($\overline{PWRTE}$).
2: $\overline{CP}$ can only be programmed to '0'. It must be set to '1' via bulk erase.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '1'	P = Programmable
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

3.1 Device ID Word

The device ID word for the PIC16F716 is located at 2006h.

TABLE 3-1: DEVICE ID VALUES

Device	Device ID Values	
	Dev	Rev
PIC16F716	01 0001 010	x xxxx

4.0 CODE PROTECTION

For PIC16F716 devices, once code protection is enabled, all program memory locations read all 0's. The ID locations and the configuration word read out in an unprotected fashion. Further programming is disabled for the entire program memory. It is possible to program the ID locations and the configuration word.

4.1 Disabling Code Protection

It is recommended that the following procedure be performed before any other programming is attempted. It is also possible to turn code protection off ($\overline{CP}$ = 1) using this procedure. However, ***all data within the program memory will be erased when this procedure is executed, and thus, the security of the code is not compromised.***

To disable code protect:

a) Execute Load Configuration (`000000`).

b) Execute Bulk Erase Program Memory (`001001`).

c) Wait TERA.

4.2 Embedding Configuration Word and ID Information in the HEX File

To allow portability of code, the programmer is required to read the configuration word and ID locations from the HEX file when loading the HEX file. If configuration word information was not present in the HEX file, then a simple warning message may be issued. Similarly, while saving a HEX file, configuration word and ID information must be included. An option to not include this information may be provided.

Microchip Technology Incorporated feels strongly that this feature is important for the benefit of the end customer.

4.3 Checksum Computation

4.3.1 CHECKSUM

Checksum is calculated by reading the contents of the PIC16F716 memory locations and adding up the opcodes up to the maximum user addressable location, (e.g., 0x7FF for the PIC16F716). Any carry bits exceeding 16 bits are neglected. Finally, the configuration word (appropriately masked) is added to the checksum. Checksum computation for each member of the PIC16F716 devices is shown in Table 4-1.

The checksum is calculated by summing the following:

- The contents of all program memory locations
- The configuration word, appropriately masked
- Masked ID locations (when applicable)

The Least Significant 16 bits of this sum is the checksum.

The following table describes how to calculate the checksum for each device. Note that the checksum calculation differs depending on the code protect setting. The configuration word and ID locations can always be read regardless of the code protect setting.

TABLE 4-1: CHECKSUM COMPUTATIONS

Device	Code Protect	Checksum*	Blank Value	0x25E6 at 0 and Max Address
PIC16F716	OFF	SUM[0x0000:0x7FF] + CFGW & 0x20CF	18CF	E49D
	ON	CFGW & 0x20CF + SUM_ID	199E(1)	E56C(1)

Legend: CFGW = Configuration Word
SUM[a:b] = [Sum of locations a to b inclusive]
SUM_ID = ID locations masked by 0xF then made into a 16-bit value with ID0 as the Most Significant nibble.
For example, ID0 = 0x1, ID1 = 0x2, ID3 = 0x3, ID4 = 0x4, then SUM_ID = 0x1234
*Checksum = [Sum of all the individual expressions] MODULO [0xFFFF]
+ = Addition
& = Bitwise AND

Note 1: Checksum shown assumes that SUM_ID contains the unprotected checksum.

5.0 PROGRAM/VERIFY MODE ELECTRICAL CHARACTERISTICS

TABLE 5-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE

AC/DC Characteristics		Standard Operating Conditions (unless otherwise stated) Operating Temperature 10°C ≤ TA ≤ 40°C Operating Voltage 4.5V ≤ VDD ≤ 5.5V				
Sym	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Conditions/Comments**
General						
VDD	VDD level for read/write operations, program memory	TBD	—	5.5	V	PIC16F716
	VDD level for bulk erase/write operations, program memory	4.5	—	5.5	V	
VIHH	High voltage on $\overline{\text{MCLR}}$ for Program/Verify mode entry	11	—	13.5	V	
IIHH	$\overline{\text{MCLR}}$ pin current during Program/ Verify mode			TBD	mA	
TVHHR	$\overline{\text{MCLR}}$ rise time (VSS to VIHH) for Program/Verify mode entry	—	—	1.0	μs	
TPPDP	Hold time after VPP↑	5	—	—	μs	
VIH1	(ICSPCLK, ICSPDAT) input high level	0.8 VDD	—	—	V	
VIL1	(ICSPCLK, ICSPDAT) input low level	—	—	0.2 VDD	V	
TSET0	ICSPCLK, ICSPDAT setup time before $\overline{\text{MCLR}}$↑ (Program/Verify mode selection pattern setup time)	100	—	—	ns	
THLD0	ICSPCLK, ICSPDAT hold time after $\overline{\text{MCLR}}$↑ (Program/Verify mode selection pattern setup time)	5	—	—	μs	
Serial Program/Verify						
TSET1	Data in setup time before clock↓	100	—	—	ns	
THLD1	Data in hold time after clock↓	100	—	—	ns	
TDLY1	Data input not driven to next clock input (delay required between command/data or command/ command)	1.0	—	—	μs	
TDLY2	Delay between clock↓ to clock↑ of next command or data	1.0	—	—	μs	
TDLY3	Clock↑ to data out valid (during Read Data)		—	80(1)	ns	
TERA	Erase cycle time	—	5	6(1)	ms	
TPROG	Programming cycle time (externally timed)	—	1	2(1)	ms	
TDIS	Time delay to next command (HV discharge time)	100	—	—	μs	

Note 1: Amount of time needed to ensure proper programming over voltage, temperature and device variations.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

DNV Certification, Inc. USA — ANSI-RAB QMS ACCREDITED — DNV MSC The Netherlands Accredited by the RvA — DNV — ISO 9001 / QS-9000 REGISTERED FIRM

Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999 and Mountain View, California in March 2002. The Company's quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, non-volatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001 certified.

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200 Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: http://www.microchip.com

Atlanta
3780 Mansell Road, Suite 130
Alpharetta, GA 30022
Tel: 770-640-0034 Fax: 770-640-0307

Boston
2 Lan Drive, Suite 120
Westford, MA 01886
Tel: 978-692-3848 Fax: 978-692-3821

Chicago
333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071 Fax: 630-285-0075

Dallas
4570 Westgrove Drive, Suite 160
Addison, TX 75001
Tel: 972-818-7423 Fax: 972-818-2924

Detroit
Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250 Fax: 248-538-2260

Kokomo
2767 S. Albright Road
Kokomo, IN 46902
Tel: 765-864-8360 Fax: 765-864-8387

Los Angeles
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888 Fax: 949-263-1338

Phoenix
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7966 Fax: 480-792-4338

San Jose
Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto
6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

Australia
Microchip Technology Australia Pty Ltd
Marketing Support Division
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

China - Beijing
Microchip Technology Consulting (Shanghai) Co., Ltd., Beijing Liaison Office
Unit 915
Bei Hai Wan Tai Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Chengdu
Microchip Technology Consulting (Shanghai) Co., Ltd., Chengdu Liaison Office
Rm. 2401-2402, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-86766200 Fax: 86-28-86766599

China - Fuzhou
Microchip Technology Consulting (Shanghai) Co., Ltd., Fuzhou Liaison Office
Unit 28F, World Trade Plaza
No. 71 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7503506 Fax: 86-591-7503521

China - Hong Kong SAR
Microchip Technology Hongkong Ltd.
Unit 901-6, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

China - Shanghai
Microchip Technology Consulting (Shanghai) Co., Ltd.
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

China - Shenzhen
Microchip Technology Consulting (Shanghai) Co., Ltd., Shenzhen Liaison Office
Rm. 1812, 18/F, Building A, United Plaza
No. 5022 Binhe Road, Futian District
Shenzhen 518033, China
Tel: 86-755-82901380 Fax: 86-755-8295-1393

China - Qingdao
Rm. B505A, Fullhope Plaza,
No. 12 Hong Kong Central Rd.
Qingdao 266071, China
Tel: 86-532-5027355 Fax: 86-532-5027205

India
Microchip Technology Inc.
India Liaison Office
Marketing Support Division
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaugnessey Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan
Microchip Technology Japan K.K.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471- 6166 Fax: 81-45-471-6122

Korea
Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Singapore
Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-6334-8870 Fax: 65-6334-8850

Taiwan
Microchip Technology (Barbados) Inc.,
Taiwan Branch
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Austria
Microchip Technology Austria GmbH
Durisolstrasse 2
A-4600 Wels
Austria
Tel: 43-7242-2244-399
Fax: 43-7242-2244-393

Denmark
Microchip Technology Nordic ApS
Regus Business Centre
Lautrup hoj 1-3
Ballerup DK-2750 Denmark
Tel: 45-4420-9895 Fax: 45-4420-9910

France
Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - ler Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany
Microchip Technology GmbH
Steinheilstrasse 10
D-85737 Ismaning, Germany
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy
Microchip Technology SRL
Via Quasimodo, 12
20025 Legnano (MI)
Milan, Italy
Tel: 39-0331-742611 Fax: 39-0331-466781

United Kingdom
Microchip Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44-118-921-5869 Fax: 44-118-921-5820

05/30/03

