PIC16C55X

EPROM Memory Programming Specification

This document includes the programming specifications for the following devices:

- PIC16C554
- PIC16C557
- PIC16C558

1.0 PROGRAMMING THE PIC16C55X

The PIC16C55X can be programmed using a serial method. In Serial mode the PIC16C55X can be programmed while in the user's system. This allows for increased design flexibility.

1.1 Hardware Requirements

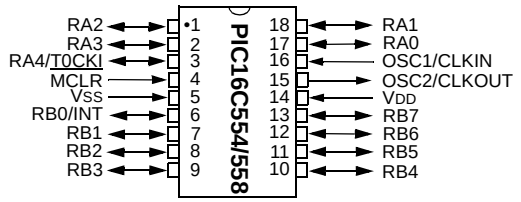
The PIC16C55X requires two programmable power supplies, one for V_{DD} (2.0V to 6.5V recommended) and one for V_{PP} (12V to 14V). Both supplies should have a minimum resolution of 0.25V.

1.2 Programming Mode

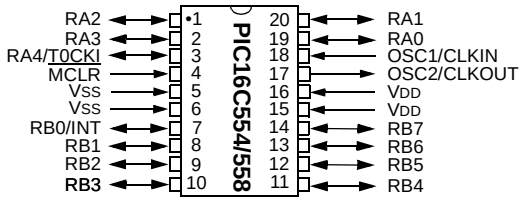
The Programming mode for the PIC16C55X allows programming of user program memory, special locations used for ID, and the configuration word for the PIC16C55X.

Pin Diagrams

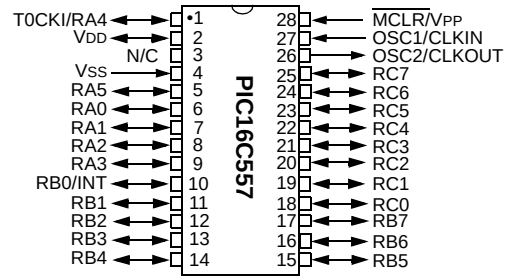
PDIP, SOIC, Windowed CERDIP



SSOP



PDIP, SOIC, Windowed CERDIP



SSOP

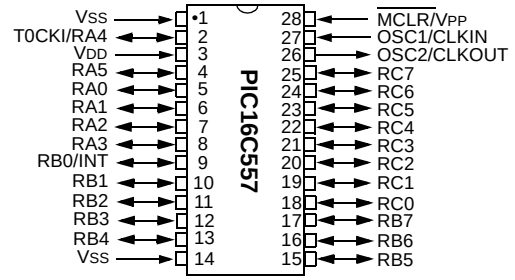


TABLE 1-1: PIN DESCRIPTIONS (DURING PROGRAMMING): PIC16C554/557/558

Pin Name	During Programming		
	Pin Name	Pin Type	Pin Description
RB6	CLOCK	I	Clock input
RB7	DATA	I/O	Data input/output
$\overline{MCLR}/V_{PP}$	V_{PP}	P	Programming Power
V_{DD}	V_{DD}	P	Power Supply
V_{SS}	V_{SS}	P	Ground

Legend: I = Input, O = Output, P = Power

2.0 PROGRAM MODE ENTRY

2.1 User Program Memory Map

The user memory space extends from 0x0000 to 0x1FFF (8K). Table 2-1 shows actual implementation of program memory in the PIC16C55X family.

TABLE 2-1: Implementation of Program Memory in the PIC16C55X

Device	Program Memory Size	Access to Program Memory
PIC16C554	0x000 - 0x1FF (0.5K)	PC<8:0>
PIC16C557	0x000 - 0x7FF (2K)	PC<10:0>
PIC16C558	0x000 - 0x7FF (2K)	PC<10:0>

When the PC reaches the last location of the implemented program memory, it will wrap around and address a location within the physically implemented memory (see Figure 2-1).

In Programming mode the program memory space extends from 0x0000 to 0x3FFF, with the first half (0x0000-0x1FFF) being user program memory and the second half (0x2000-0x3FFF) being configuration memory. The PC will increment from 0x0000 to 0x1FFF and wrap to 0x0000 or 0x2000 to 0x3FFF and wrap around to 0x2000 (not to 0x0000). Once in configuration memory, the highest bit of the PC stays a '1', thus always pointing to the configuration memory. The only way to point to user program memory is to reset the part and re-enter Program/Verify mode, as described in Section 2.2.

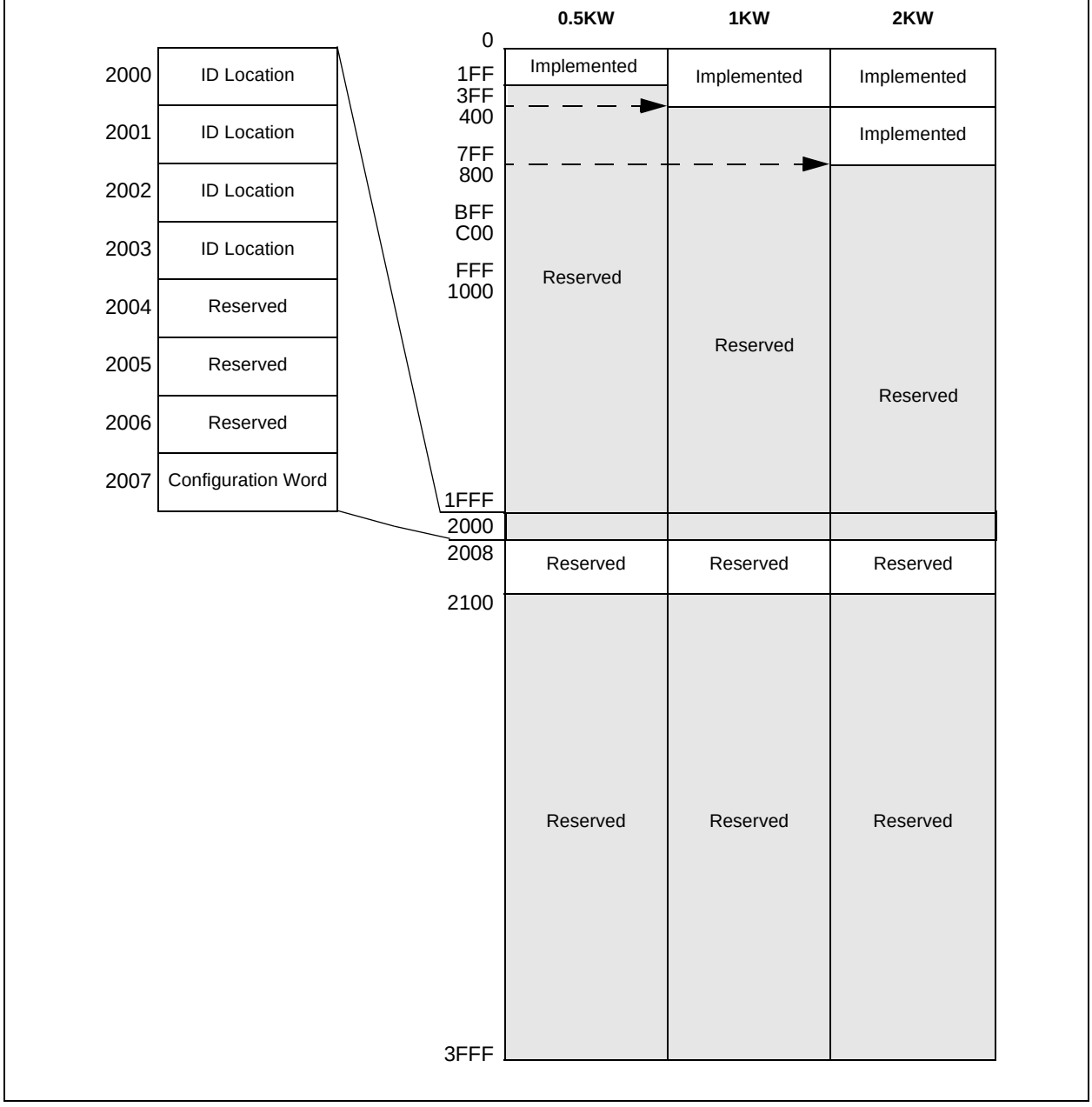
In the configuration memory space, 0x2000-0x20FF are utilized. When in a configuration memory, as in the user memory, the 0x2000-0x20FF segment is repeatedly accessed as the PC exceeds 0x20FF (see Figure 2-1).

A user may store identification information (User ID) in four ID locations. The User ID locations are mapped in [0x2000: 0x2003]. These locations read out normally even after code protection is enabled.

Note 1: All other locations in PICmicro® MCU configuration memory are reserved and should not be programmed.

2: Only the low order 4 bits of the User ID locations may be included in the device checksum. See Section 4.3 for checksum calculation details.

FIGURE 2-1: PROGRAM MEMORY MAPPING



2.2 Program/Verify Mode

The Program/Verify mode is entered by holding pins RB6 and RB7 low while raising $\overline{MCLR}$ pin from V_{IL} to V_{IHH} (high voltage). Once in this mode the user program memory and the configuration memory can be accessed and programmed in a serial fashion. The mode of operation is serial, and the memory that is accessed is the user program and configuration memory. RB6 is a Schmitt Trigger input in this mode.

The sequence that enters the device into the Programming/Verify mode places all other logic into the RESET state (the $\overline{MCLR}$ pin was initially at V_{IL}). This means that all I/O are in the RESET state (High impedance inputs).

Note:	The $\overline{MCLR}$ pin should be raised as quickly as possible from V_{IL} to V_{IHH}. This is to ensure that the device does not have the PC incremented while in valid operation range.

2.2.1 PROGRAM/VERIFY OPERATION

The RB6 pin is used as a clock input pin and the RB7 pin is used for entering command bits and data input/output during serial operation. To input a command, the clock pin (RB6) is cycled six times. Each command bit is latched on the falling edge of the clock with the Least Significant bit (LSb) of the command being input first. The data on pin RB7 is required to have a minimum setup and hold time (see AC/DC specs) with respect to the falling edge of the clock. Commands that have data associated with them (Read and Load) are specified to have a minimum delay of 1 µs between the command and the data. After this delay the clock pin is cycled 16 times with the first cycle being a START bit and the last cycle being a STOP bit. Data is also input and output LSb first. Therefore, during a read operation the LSb will be transmitted onto pin RB7 on the rising edge of the second cycle, and during a load operation the LSb will be latched on the falling edge of the second cycle. A minimum 1 µs delay is also specified between consecutive commands.

The commands that are available are listed in Table 2-2.

2.2.1.1 Load Configuration

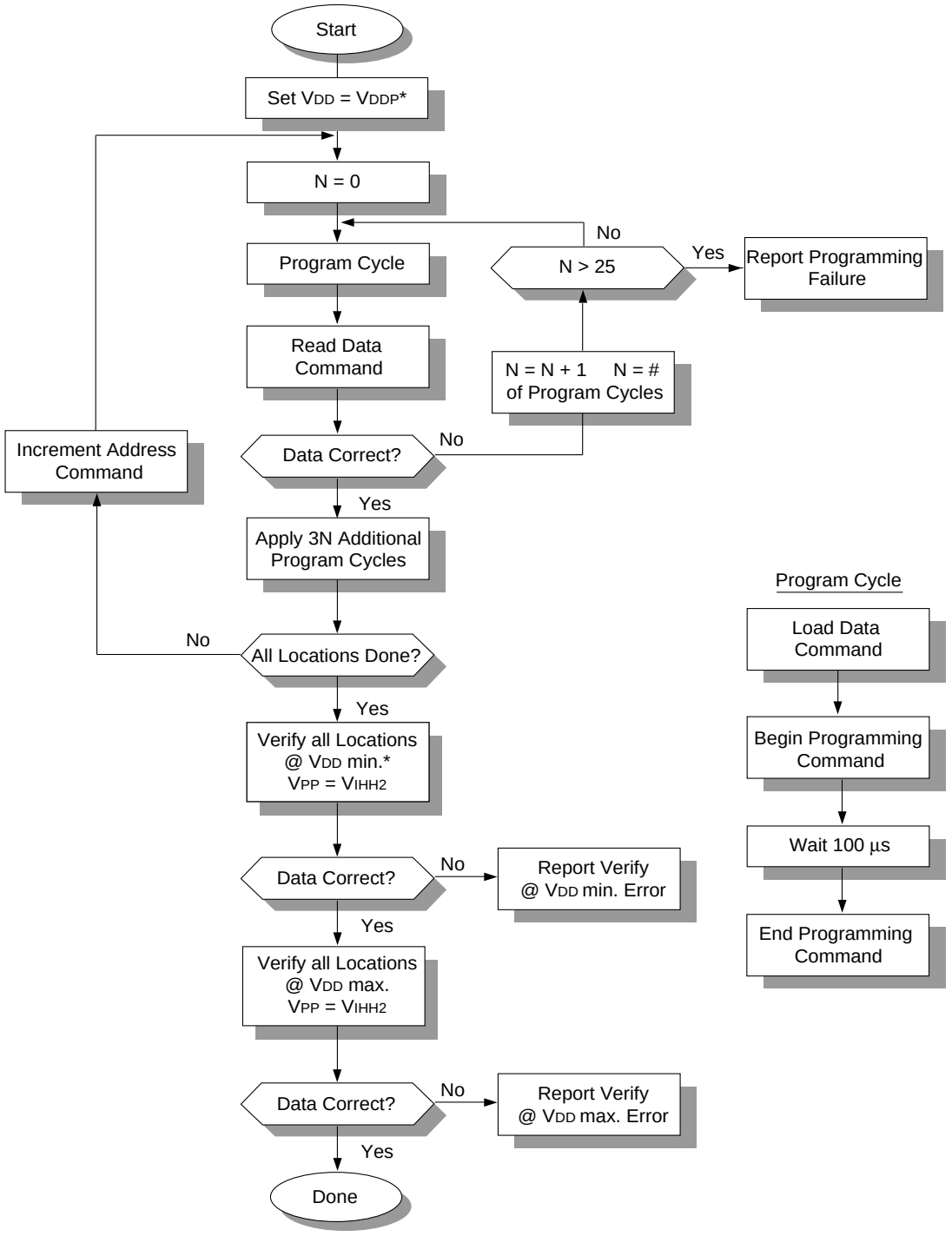
After receiving this command, the program counter (PC) will be set to 0x2000. By then applying 16 cycles to the clock pin, the chip will load 14-bits a “data word” as described above, to be programmed into the configuration memory. A description of the memory mapping schemes for normal operation and Configuration mode operation is shown in Figure 2-1. After the configuration memory is entered, the only way to get back to the user program memory is to exit the Program/Verify Test mode by taking $\overline{MCLR}$ low (V_{IL}).

TABLE 2-2: COMMAND MAPPING

Command	Mapping (MSB ... LSB)						Data
Load Configuration	0	0	0	0	0	0	0, data(14), 0
Load Data	0	0	0	0	1	0	0, data(14), 0
Read Data	0	0	0	1	0	0	0, data(14), 0
Increment Address	0	0	0	1	1	0	
Begin Programming	0	0	1	0	0	0	
End Programming	0	0	1	1	1	0	

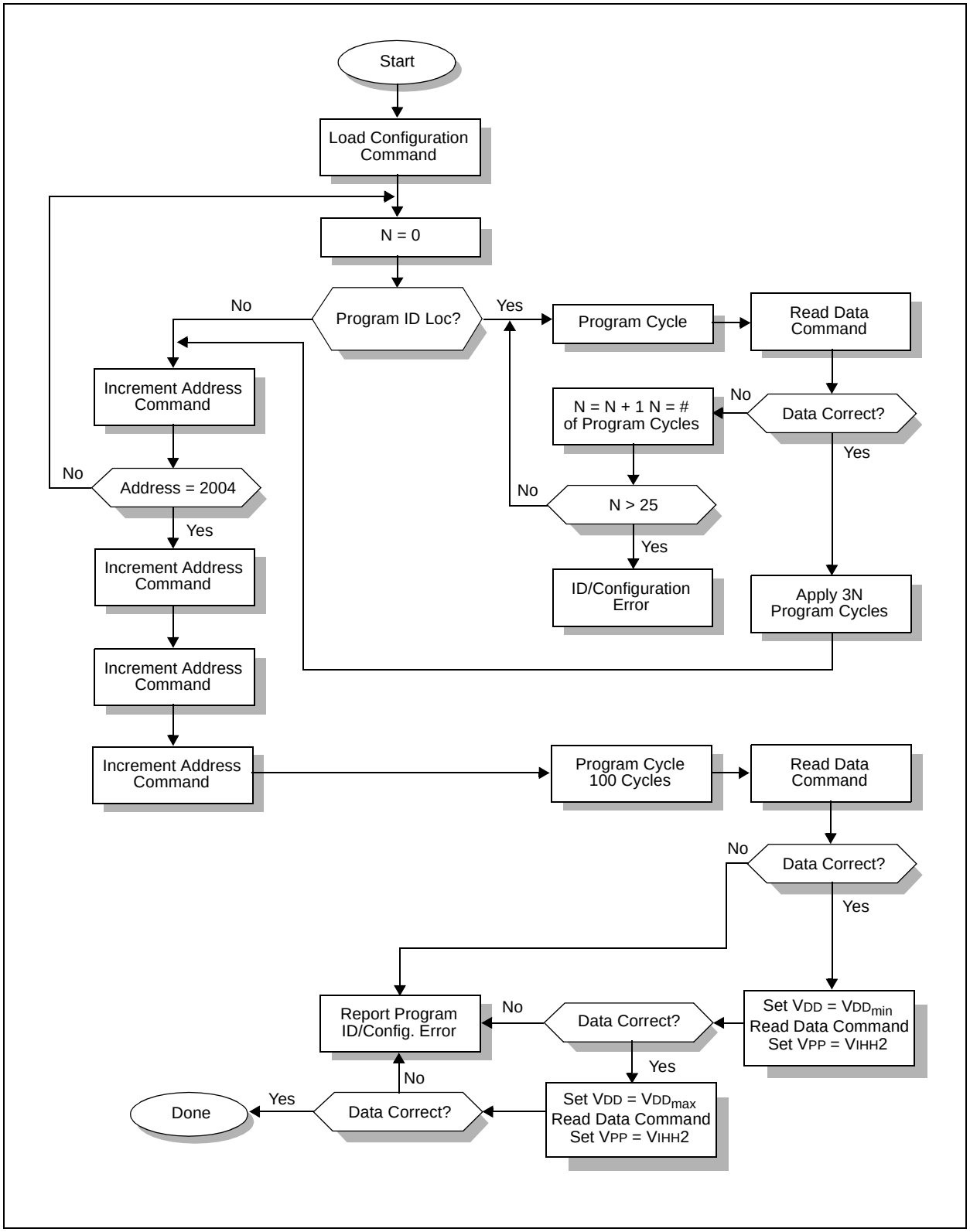
Note: The CPU clock must be disabled during in-circuit programming.

FIGURE 2-2: PROGRAM FLOW CHART - PIC16C55X PROGRAM MEMORY



* V_{DDP} = V_{DD} range for programming (typically 4.75V - 5.25V).
$V_{DD_{min}}$ = Minimum V_{DD} for device operation.
$V_{DD_{max}}$ = Maximum V_{DD} for device operation.

FIGURE 2-3: PROGRAM FLOW CHART - PIC16C55X CONFIGURATION WORD & ID LOCATIONS



2.2.1.2 Load Data

After receiving this command, the chip will load in a 14-bit “data word” when 16 cycles are applied, as described previously. A timing diagram for the Load Data command is shown in Figure 5-1.

2.2.1.3 Read Data

After receiving this command, the chip will transmit data bits out of the memory currently accessed starting with the second rising edge of the clock input. The RB7 pin will go into Output mode on the second rising clock edge, and it will revert back to Input mode (hi-impedance) after the 16th rising edge. A timing diagram of this command is shown in Figure 5-2.

2.2.1.4 Increment Address

The PC is incremented when this command is received. A timing diagram of this command is shown in Figure 5-3.

2.2.1.5 Begin Programming

A Load command (load configuration or load data) must be given before every Begin Programming command. Programming of the appropriate memory (test program memory or user program memory) will begin after this command is received and decoded. Programming should be performed with a series of 100 µs programming pulses. A programming pulse is defined as the time between the Begin Programming command and the End Programming command.

2.2.1.6 End Programming

After receiving this command, the chip stops programming the memory (configuration program memory or user program memory) that it was programming at the time.

2.3 Programming Algorithm Requires Variable V_{DD}

The PIC16C55X uses an intelligent algorithm. The algorithm calls for program verification at $V_{DD_{min}}$ as well as $V_{DD_{max}}$. Verification at $V_{DD_{min}}$ ensures good “erase margin”. Verification at $V_{DD_{max}}$ ensures good “program margin”.

The actual programming must be done with V_{DD} in the V_{DDP} range (4.75 - 5.25V).

V_{DDP} = V_{CC} range required during programming.

V_{DD} min. = minimum operating V_{DD} spec for the part.

V_{DD} max. = maximum operating V_{DD} spec for the part.

Programmers must verify the PIC16C55X at its specified $V_{DD_{max}}$ and $V_{DD_{min}}$ levels. Since Microchip may introduce future versions of the PIC16C55X with a broader V_{DD} range, it is best that these levels are user selectable (defaults are ok).

Note:	Any programmer not meeting these requirements may only be classified as “prototype” or “development” programmer but not a “production” quality programmer.

3.0 CONFIGURATION WORD

The PIC16C55X family members have several configuration bits. These bits can be programmed (reads '0') or left unprogrammed (reads '1') to select various device configurations. Figure 3-1 provides an overview of configuration bits.

FIGURE 3-1: CONFIGURATION WORD BIT MAP

PIC16C554/557/558

CP1	CP0	CP1	CP0	CP1	CP0	–	0	CP1	CP0	PWRTE	WDTE	FOSC1	FOSC0
bit 13													bit 0

bit 7 Reserved for future use

bit 6 Set to 0

bit 4,5, 8-13 CP1:CP0, Code Protect

Device	CP1	CP0	Code Protection
PIC16C554	0	0	All memory protected
	0	1	Do not use
	1	0	Do not use
	1	1	Code protection off
PIC16C557 PIC16C558	0	0	All memory protected
	0	1	Upper 3/4 memory protected
	1	0	Upper 1/2 memory protected
	1	1	Code protection off

bit 3 **$\overline{\text{PWRTE}}$**, Power-up Timer Enable Bit

1 = Power-up timer disabled
0 = Power-up timer enabled

bit 2 **WDTE**, WDT Enable Bit

1 = WDT enabled
0 = WDT disabled

bit 1-0 **FOSC<1:0>**, Oscillator Selection Bits

11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

4.0 CODE PROTECTION

The program code written into the EPROM can be protected by writing to the CP0 & CP1 bits of the configuration word.

4.1 Programming Locations 0x0000 to 0x03F after Code Protection

For PIC16C55X devices, once code protection is enabled, all protected segments read '0's (or “garbage values”) and are prevented from further programming. All unprotected segments, including ID locations and configuration word, read normally. These locations can be programmed.

4.2 Embedding Configuration Word and ID Information in the HEX File

Note: To allow portability of code, the programmer is required to read the configuration word and ID locations from the HEX file when loading the HEX file. If configuration word information was not present in the HEX file then a simple warning message may be issued. Similarly, while saving a HEX file, configuration word and user ID information must be included. An option to not include this information may be provided. Microchip Technology Inc. feels strongly that this feature is important for the benefit of the end customer.

TABLE 4-1: Configuration Word

PIC16C554

To code protect:

- Protect all memory `0000001000XXXX`
- No code protection `1111111011XXXX`

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0x2007)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Protected memory segment	Read All ‘0’s, Write Disabled	Read Unscrambled, Write Enabled
ID Locations (0x2000 : 0x2003)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled

PIC16C556

To code protect:

- Protect all memory `0000001000XXXX`
- Protect upper 1/2 memory `0101011001XXXX`
- No code protection `1111111011XXXX`

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0x2007)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Protected memory segment	Read All ‘0’s, Write Disabled	Read Unscrambled, Write Enabled
ID Locations (0x2000 : 0x2003)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled

PIC16C557/558

To code protect:

- Protect all memory `0000001000XXXX`
- Protect upper 3/4 memory `0101011001XXXX`
- Protect upper 1/2 memory `1010101010XXXX`
- No code protection `1111111011XXXX`

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0x2007)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Protected memory segment	Read All ‘0’s, Write Disabled	Read Unscrambled, Write Enabled
ID Locations (0x2000 : 0x2003)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled

4.3 Checksum

4.3.1 CHECKSUM CALCULATIONS

The checksum is calculated by reading the contents of the PIC16C55X memory locations and adding up the opcodes up to the maximum user addressable location, (e.g., 0x1FF for the PIC16C74). Any carry bits exceeding 16 bits are neglected. Finally, the configuration word (appropriately masked) is added to the checksum. Checksum computation for each member of the PIC16C55X devices is shown in Table 4-2.

The checksum is calculated by summing the following:

- The contents of all program memory locations
- The configuration word, appropriately masked
- Masked ID locations (when applicable)

The Least Significant 16 bits of this sum is the checksum.

The following table describes how to calculate the checksum for each device. Note that the checksum calculation differs depending on the code protect setting. Since the program memory locations read out differently depending on the code protect setting, the table describes how to manipulate the actual program memory values to simulate the values that would be read from a protected device. When calculating a checksum by reading a device, the entire program memory can simply be read and summed. The configuration word and ID locations can always be read.

Note:	Some older devices have an additional value added in the checksum. This is to maintain compatibility with older device programmer checksums.

TABLE 4-2: CHECKSUM COMPUTATION

Device	Code Protect	Checksum*	Blank Value	0x25E6 at 0 and max address
PIC16C554	OFF ALL	SUM[0x000:0x1FF] + CFGW & 0x3F3F SUM_ID + CFGW & 0x3F3F	3D3F 3D4E	090D 091C
PIC16C557 PIC16C558	OFF 1/2 3/4 ALL	SUM[0x000:0x7FF] + CFGW & 0x3F3F SUM[0x000:0x3FF] + CFGW & 0x3F3F + SUM_ID SUM[0x000:0x1FF] + CFGW & 0x3F3F + SUM_ID CFGW & 0x3F3F + SUM_ID	373F 5D6E 4A5E 374E	030D 0F23 FC13 031C

Legend: CFGW = Configuration Word
SUM[a:b] = [Sum of locations a through b inclusive]
SUM_ID = ID locations masked by 0xF then made into a 16-bit value with ID0 as the Most Significant nibble. For example,
ID0 = 0x12, ID1 = 0x37, ID2 = 0x4, ID3 = 0x26, then SUM_ID = 0x2746.
*Checksum = [Sum of all the individual expressions] **MODULO** [0xFFFF]
+ = Addition
& = Bitwise AND

5.0 PROGRAM/VERIFY MODE ELECTRICAL CHARACTERISTICS

TABLE 5-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY TEST MODE

Standard Operating Conditions **Operating Temperature: +10° C ≤ TA ≤ +40° C, unless otherwise stated, (25° C is recommended)** **Operating Voltage: 4.5 V ≤ VDD ≤ 5.5 V, unless otherwise stated.**							
Parameter No.	**Sym.**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
General							
PD1	VDDP	Supply voltage during programming	4.75	5.0	5.25	V	
PD2	IDDP	Supply current (from VDD) during programming	-	-	20	mA	
PD3	VDDV	Supply voltage during verify	VDDmin	-	VDDmax	V	**Note 1**
PD4	VIHH1	Voltage on $\overline{MCLR}$/VPP during programming	12.75	-	13.25	V	**Note 2**
PD5	VIHH2	Voltage on $\overline{MCLR}$/VPP during verify	VDD + 4.0	-	13.5	-	
PD6	IPP	Programming supply current (from VPP)	-	-	50	mA	
PD9	VIH1	(RB6, RB7) input high level	0.8 VDD	-	-	V	Schmitt Trigger input
PD8	VIL1	(RB6, RB7) input low level	0.2 VDD	-	-	V	Schmitt Trigger input
Serial Program Verify							
P1	TR	$\overline{MCLR}$/VPP rise time (VSS to VHH) for Test mode entry	-	-	8.0	µs	
P2	TF	$\overline{MCLR}$ Fall time	-	-	8.0	µs	
P3	Tset1	Data in setup time before clock ↓	100	-	-	ns	
P4	Thld1	Data in hold time after clock ↓	100	-	-	ns	
P5	Tdly1	Data input not driven to next clock input (delay required between command/data or command/command)	1.0	-	-	µs	
P6	Tdly2	Delay between clock ↓ to clock ↑ of next command or data	1.0	-	-	µs	
P7	Tdly3	Clock ↑ to date out valid (during read data)	200	-	-	ns	
P8	Thld0	Hold time after $\overline{MCLR}$ ↑	2	-	-	µs	
-	Tpw	Programming Pulse Width	10	100	1000	µs	

Note 1: Program must be verified at the minimum and maximum VDD limits for the part.

2: VIHH must be greater than VDD + 4.5V to stay in Programming/Verify mode.

FIGURE 5-1: LOAD DATA COMMAND (PROGRAM/VERIFY)

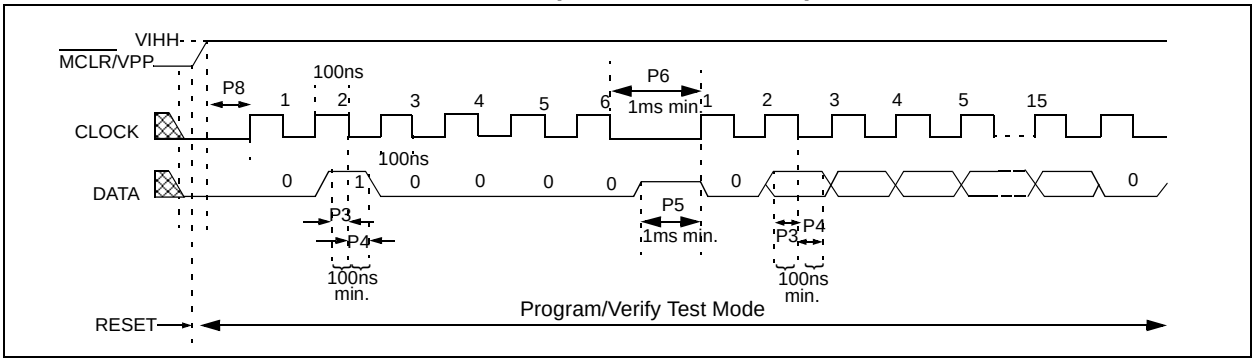


FIGURE 5-2: READ DATA COMMAND (PROGRAM/VERIFY)

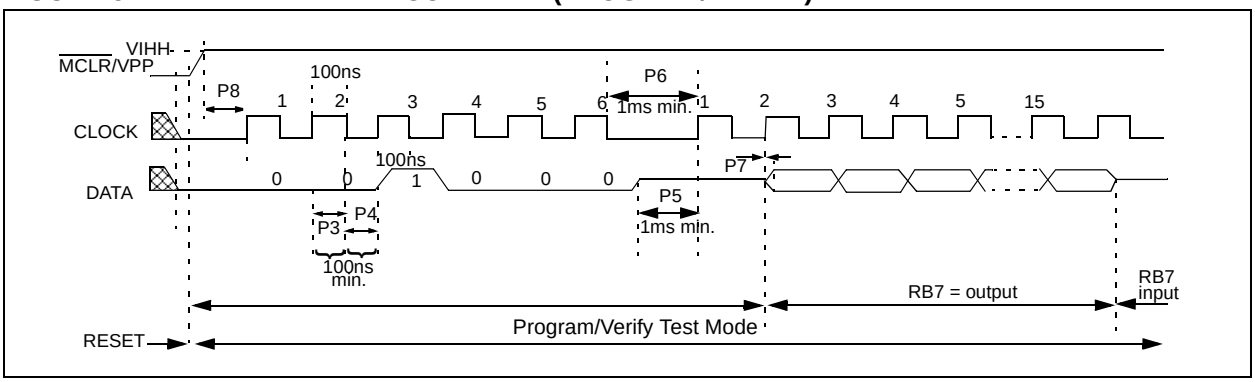
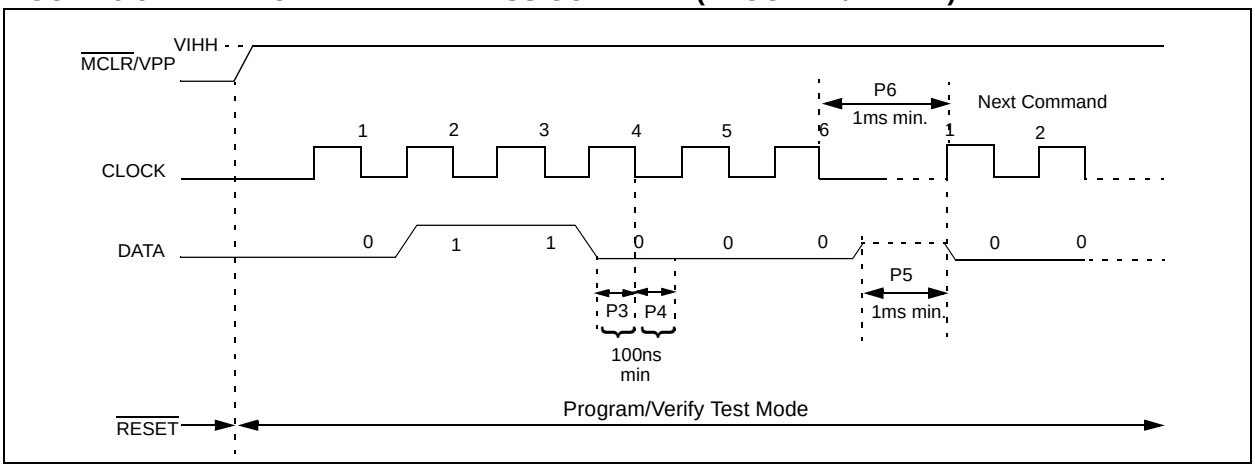


FIGURE 5-3: INCREMENT ADDRESS COMMAND (PROGRAM/VERIFY)



NOTES:

Note the following details of the code protection feature on PICmicro® MCUs.

- The PICmicro family meets the specifications contained in the Microchip Data Sheet.
- Microchip believes that its family of PICmicro microcontrollers is one of the most secure products of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the PICmicro microcontroller in a manner outside the operating specifications contained in the data sheet. The person doing so may be engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable”.
- Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our product.

If you have any further questions about this matter, please contact the local sales office nearest to you.

DNV Certification, Inc. USA — ANSI-RAB QMS ACCREDITED — DNV MSC The Netherlands Accredited by the RvA — DNV — ISO 9001 / QS-9000 REGISTERED FIRM

Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999 and Mountain View, California in March 2002. The Company’s quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, non-volatile memory and analog products. In addition, Microchip’s quality system for the design and manufacture of development systems is ISO 9001 certified.

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200 Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: http://www.microchip.com

Rocky Mountain
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7966 Fax: 480-792-4338

Atlanta
500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770-640-0034 Fax: 770-640-0307

Boston
2 Lan Drive, Suite 120
Westford, MA 01886
Tel: 978-692-3848 Fax: 978-692-3821

Chicago
333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071 Fax: 630-285-0075

Dallas
4570 Westgrove Drive, Suite 160
Addison, TX 75001
Tel: 972-818-7423 Fax: 972-818-2924

Detroit
Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250 Fax: 248-538-2260

Kokomo
2767 S. Albright Road
Kokomo, Indiana 46902
Tel: 765-864-8360 Fax: 765-864-8387

Los Angeles
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888 Fax: 949-263-1338

New York
150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 631-273-5305 Fax: 631-273-5335

San Jose
Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto
6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

Australia
Microchip Technology Australia Pty Ltd
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

China - Beijing
Microchip Technology Consulting (Shanghai) Co., Ltd., Beijing Liaison Office
Unit 915
Bei Hai Wan Tai Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Chengdu
Microchip Technology Consulting (Shanghai) Co., Ltd., Chengdu Liaison Office
Rm. 2401, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-86766200 Fax: 86-28-86766599

China - Fuzhou
Microchip Technology Consulting (Shanghai) Co., Ltd., Fuzhou Liaison Office
Unit 28F, World Trade Plaza
No. 71 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7503506 Fax: 86-591-7503521

China - Shanghai
Microchip Technology Consulting (Shanghai) Co., Ltd.
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

China - Shenzhen
Microchip Technology Consulting (Shanghai) Co., Ltd., Shenzhen Liaison Office
Rm. 1315, 13/F, Shenzhen Kerry Centre,
Renminnan Lu
Shenzhen 518001, China
Tel: 86-755-82350361 Fax: 86-755-82366086

China - Hong Kong SAR
Microchip Technology Hongkong Ltd.
Unit 901-6, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

India
Microchip Technology Inc.
India Liaison Office
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaugnessey Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan
Microchip Technology Japan K.K.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471- 6166 Fax: 81-45-471-6122

Korea
Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Singapore
Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-6334-8870 Fax: 65-6334-8850

Taiwan
Microchip Technology (Barbados) Inc.,
Taiwan Branch
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Austria
Microchip Technology Austria GmbH
Durisolstrasse 2
A-4600 Wels
Austria
Tel: 43-7242-2244-399
Fax: 43-7242-2244-393

Denmark
Microchip Technology Nordic ApS
Regus Business Centre
Lautrup hoj 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France
Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - ler Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany
Microchip Technology GmbH
Steinheilstrasse 10
D-85737 Ismaning, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Italy
Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

United Kingdom
Microchip Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44 118 921 5869 Fax: 44-118 921-5820

08/01/02