AFE Calibration on SAM V/E/S7x Microcontrollers

APPLICATION NOTE

Introduction

The Atmel® | SMART SAM V/E/S7x series are high-performance, power-efficient embedded MCUs based on the ARM® Cortex®-M7 processor.

Analog-to-digital converters translate analog measurements, characteristic of most phenomena in the real world, to digital format, used in information processing, computing, data transmission, and control systems.

The purpose of this application note is to propose a method of offset and gain calibration using digital processing including the average and the calibration registers.

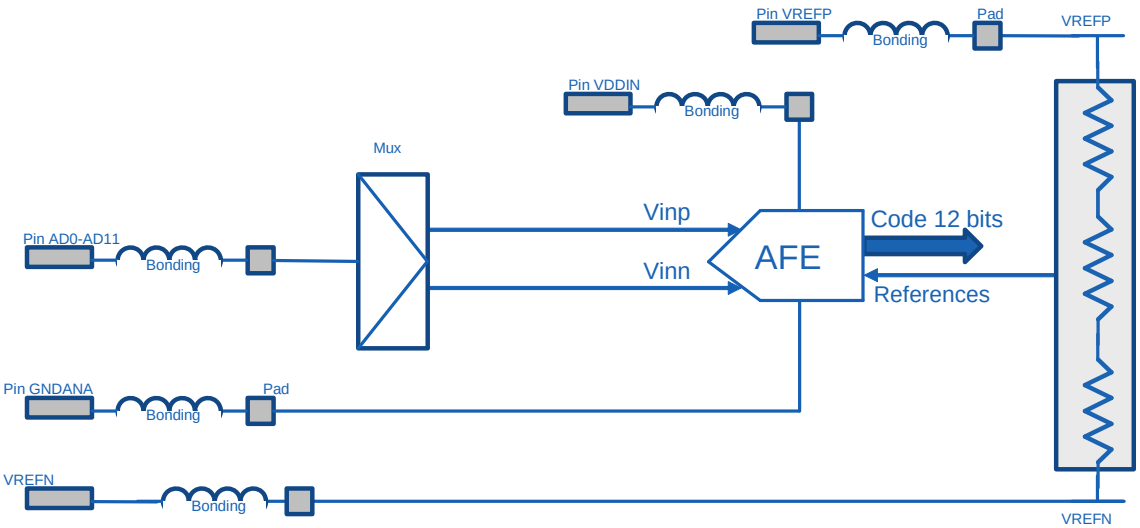
An efficient way to generate the analog levels used in the calibration is also proposed.

Reference Documents

Type	Title	Atmel Lit. No.
Datasheet	SAM V71 Datasheet	44003
Datasheet	SAM V70 Datasheet	11297
Datasheet	SAM E70 Datasheet	11296
Datasheet	SAM S70 Datasheet	11242

1. Block Diagram

Figure 1-1. AFE Block Diagram (BGA144 Package)



The AFE implements a cyclic ADC architecture. After an input sampling, the ADC processes the voltage in 12 steps, using 23 AFE clock cycles. As illustrated in the above figure, the AFE is built as a differential AFE. This capability provides a good common mode noise rejection which is essential in a microcontroller working at high clock frequency. Without this differential design, the ADC aliases the noise of the microcontroller digital activity and drastically reduces performance.

From the natural Differential mode of the ADC, a Single-ended mode is implemented. This mode uses all the positive inputs ADx,y for the signal V_{INP} and V_{DAC} as the reference connected to the ADC negative input V_{INN}.

Figure 1-2. Functional Diagram of Sample in Single-Ended Mode

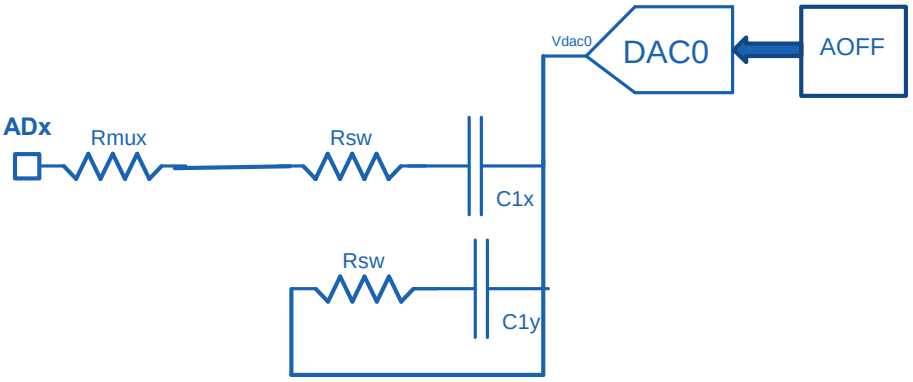


Figure 1-3. Functional Diagram of Sample in Differential Mode

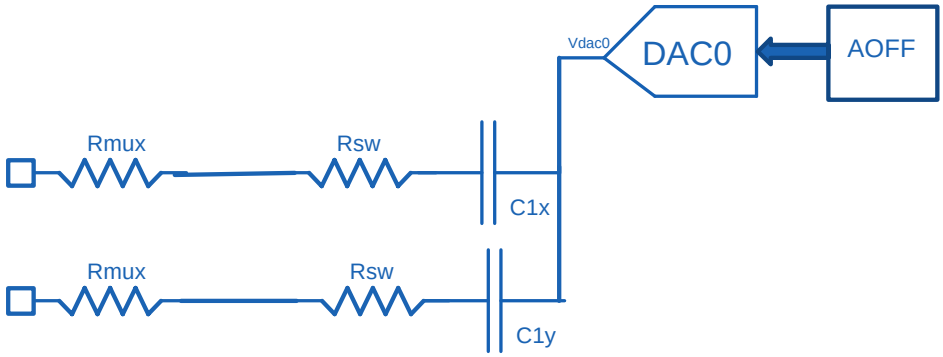
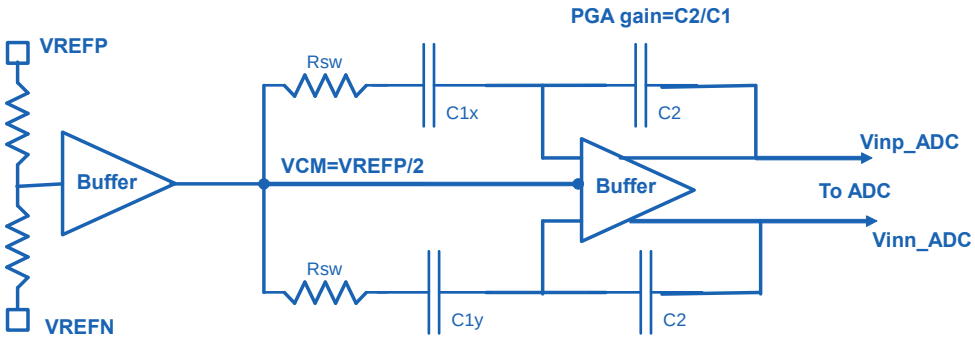


Figure 1-4. Functional Diagram of Hold in Single-Ended and Differential Modes

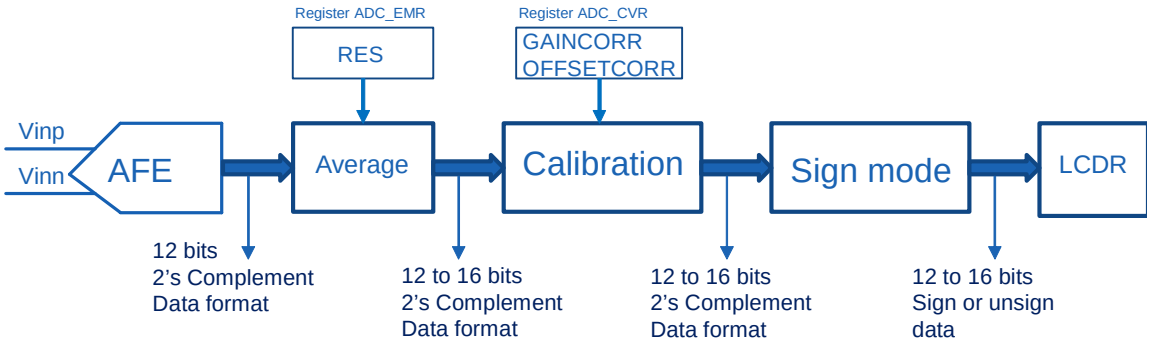


Built in this way, the Single-ended mode maintains the good noise rejection feature of Differential mode. The noise immunity is also reinforced with the dedicated power supply rails VDDANA-GNDANA and the dedicated pin for references VREFP-VREFN.

2. AFE Processing

The AFE is followed by some digital processing (an average, an offset and gain correction, and a sign format output) before going into the AFE Last Converted Data register (AFEC_LCDR) and AFE Channel Data register (AFEC_CDR).

Figure 2-1. AFE Digital Processing



The data out of the ADC is in 12-bit 2's Complement format. All the processing until the Sign mode block is based on a signed operation. The Sign mode block adds 2047 to the DATA to obtain not-signed output.

The appropriate value of the AFEC_COCR.AOFF field is 512 (the reset value is zero). Different values are possible for each channel. In a sequencer with more than one selected channel, AOFF is read and updated after the first channel in numeric order. If only one channel is selected, AOFF is read during startup time once and cannot be updated. A new value of AOFF can be updated to the condition to restart the AFEC or to run two conversions; the second one will have the correct AOFF.

AFEC_ACR.IBCTL should be 10.

With AFEC_MR.TRANSFER=2 and AFEC_MR.TRACKTIM=0, the conversion time is 23 cycles of the ADC clock. The available tracking time is always 15 cycles of the ADC clock. Increasing the tracking time can be done only by reducing the ADC clock frequency.

IMPORTANT	It is recommended to run the ADCLOCK at a lower frequency, i.e. avoid 40 MHz. 10 MHz or 20 MHz reduces the risk of altering the output code with noise.
IMPORTANT	IO pull-up resistance is not automatically disabled when a channel is selected, so this operation needs to be performed previously in the PIO Controller.
IMPORTANT	There is no interrupt for a sequence of conversion; there is an interrupt for each channel individually.

2.1 ADC Averaging

The averaging block filters the ADC 12-bit DATA in order to suppress noise. Not all kinds of noise can be reduced by this technique. The highest efficiency is achieved with white noise, such as thermal noise and quantization noise.

The OSR represents the numbers of averaged samples. The final code is the result of the computation:

$$\text{Averaged Code} = \frac{1}{\sqrt{\text{OSR}}} \sum_{k=1}^{\text{OSR}} \text{Sample}(k)$$

The code gets one additional bit of resolution for 4 averaged samples.

This result is not true when the noise is not white. This often occurs when parasitic noise is generated by a digital activity or by a clock noise in ground or supply. The gain of resolution can be reduced down to 0.8 each 4 averaged samples. An actual measurement in 12-bit mode gives a resolution of 10.2 bits effective, which is mainly due to digital activity noise and may change from one application to another.

An actual achievement would be as follows:

OSR	Extra Bits	Resolution
4	0.8	11
16	1.6	11.8
64	2.4	12.6
256	3.2	13.4

When an average is used, the code is multiplied by the dynamic enhancement factor M:

OSR	M	Code Max
4	2	8191
16	4	16383
64	8	32767
256	16	65535

with

$$R = 12 + \frac{\log_2(\text{OSR})}{2}$$

where R is the resolution of the ADC with averaging (OSR).

2.2 ADC Automatic Error Correction

This ADC is built as a differential ADC, so offset error is measured at the midpoint ADVREFP/2, even in Single-ended mode. As a consequence, all modes have the same definition of offset and gain error and the same corrective method.

2.2.1 Gain and Offset Error

For a given offset of E_O(LSB) with 12-bit resolution, this offset value is M × E_O LSB when the OSR is used.

For a given gain error E_G(%), this gain error remains unchanged whatever the OSR. The AFE introduces an offset error and then multiplies it by the gain. But we consider the final mathematic equation as y=ax+b form.

The actual code $C_A=(1+E_G/100)\times(C_i+Offset)=(1+E_G/100)\times C_i+E_O$

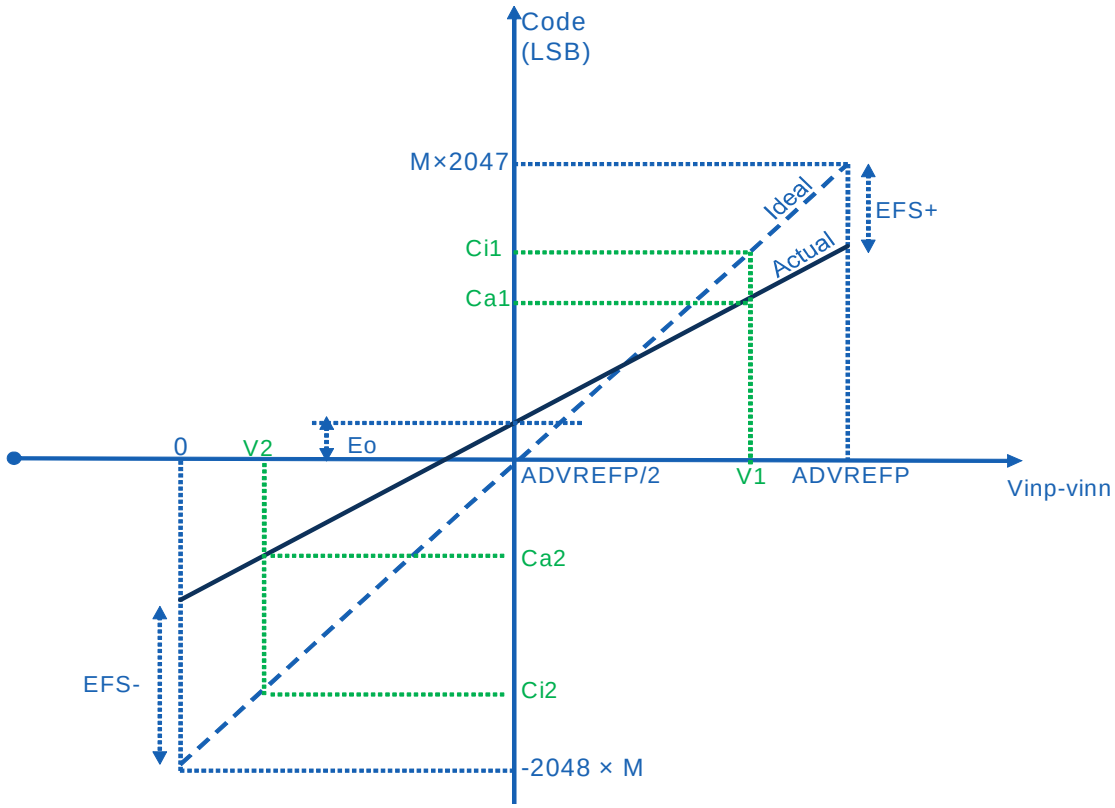
With $E_O=(1+E_G/100)\times Offset$

E_G is the gain error, $E_G(\%)=100\times E_{FS} / (M\times 4096)$

With full-scale gain error $E_{FS} = (E_{FS+}) - (E_{FS-})$

C_i is the ideal code.

Figure 2-2. Gain and Offset Error



In Single-ended mode, V_{INP}= input signal, V_{INN}= V_{DAC}.

In Differential mode, V_{INP}= positive input signal, V_{INN}= negative input signal.

This automatic error correction feature can be very useful for a user to remove offset and gain error coming from an applicative system, and not only the errors internal to the ADC.

2.2.2 Hardware Correction

The fields OFFSETCORR and GAINCORR in the AFE Correction Values register (AFEC_CVR) need to be filled with corrective data. This data is computed from two measurement points in signed format. The correction is the same for all functional modes.

By choosing two input voltages, V1 and V2, giving the actual measured points, C_A1 and C_A2, this data contains offset error and gain error added on the corresponding ideal points, C_i1 and C_i2. Use signed output code to get the data in the correct format. The use of an averaged value is advised to reduce noise disturbance on the calibration values.

The gain error is computed $E_G = 100\times(((C_A2-C_A1))/((C_i2-C_i1))-1)$

The offset error is computed $E_O = C_A2-(1+E_G/100)\times C_i2)$

If the code is measured in a nonsigned format, then the computation must be reverted to a signed format like:

$E_O= (C_A2-2047)-(1+E_G/100)\times(C_i2-2047)$

With the field OFFSETCORR = $-E_O$

and the field GAINCORR= rounding of $2^{15} \times (C_i2-C_i1)/(C_A2-C_A1)$

The automatic correction is calculated as:

Corrected code = (Code+OFFSETCORR) × GAINCORR/2^{15}

To obtain a correct calibration, it is essential to have an external stable and accurate voltage to measure, such as a bandgap voltage.

This voltage is provided externally to the AFE. If VREFP accuracy is not ensured (for example ±3%), the calibration also corrects this error. This supposes that VREFP is stable over time, temperature and power consumption.

Once a calibration is performed for Single-ended mode, it stays valid for Differential mode.

2.2.3 Software Correction

The hardware correction can be replaced by a software correction. When using the same equation of E_O evaluation and correction as the hardware correction, it is important to pay attention to the Offset and Gain order of correction: In this case Offset is corrected first and the Gain after, not the opposite.

3. Creating Two Calibration Points V1 and V2 without External Voltage

The AFE features a 10-bit DAC in feedback with all inputs. A calibration method consists of taking advantage of this DAC to create the V1 and V2 voltages used to compute the offset and gain error. However, this method does not correct the inner variations of the VREFP due to the fact that V1 and V2 depend on VREFP.

The main error comes from PGA0 or PGA1. An input of PGA0 must be grounded (or any input with a possible zero volt measurement). This is also valid for calibration of PGA1.The 10-bit DAC AFEC_COCR.AOFF field will be programmed with two values, AOFF1 and AOFF2.

V1=GND-VAOFF1

V2=GND-VAOFF2

Computation Example:

We select AOFF1=100 and AOFF2=400.

Assuming VDDIN=3.3V=VREFP (for the example):

V1=VREFP × AOFF1/1024=0.322266V

V2=VREFP × AOFF2/1024=1.289063V

Table 3-1. Computation Example with an OSR=256, Resolution R=16 bits

Step	Parameter	Value	Unit	Equations
ideal	C_i1	-6400	LSB	2^R × (0-V1) / VREFP
ideal	C_i2	-25600	LSB	2^R × (0-V2) / VREFP
actual	C_A1	-6434	LSB	Measured signed format
actual	C_A2	-25826	LSB	Measured signed format
Extraction of Gain and Offset:				
Error	Gain	1.01	–	Gain=(C_A2-C_A1) / (C_i2-C_i1)
Error	Offset	30	–	Offset=C_A2-C_i2 × Gain
From this point, the correction can be applied:				
Register	OFFSETCORR	-30	LSB	OFFSETCORR=-Offset
Register	GAINCORR	32443	LSB	GAINCORR=FLOOR(2^{15}/Gain,1)
Verification				
corrected	C1	-6400	LSB	C1=FLOOR((C_A1+OFFSETCORR) × GAINCORR/2^{15},1)
corrected	C2	-25600	LSB	C2=FLOOR((C_A2+OFFSETCORR) × GAINCORR/2^{15},1)

Note: 1. Converted data must be in signed format.

This method works for all values of VREFP. If VREFP varies ±3%, the calibration data is not affected and the AFEC is compensated for its own error of gain and offset. The DAC INL, gain and offset error introduces an error on the calibration. If the final accuracy is not sufficient, then an external voltage V1 and V2 are required.

Unfortunately, the absolute accuracy (including the VREFP variation) is not corrected. To improve it, it is necessary to compensate the VREFP variations.

The advantage to this method is that it can be used in-application and compensates for temperature variation of offset and gain error if the calibration is repeated periodically.

Revision History

Table 3-2. Revision History

Date	Change
29-Aug-16	First issue.

Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**