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## Doze, Idle and PMD Features of 8-Bit PIC<sup>®</sup> Microcontrollers

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### INTRODUCTION

The demand for portable and battery-operated equipment increases as they are gaining more popularity in the market. With microcontrollers providing most of the control in such applications, they are also responsible for the highest system power consumption. Thus, managing the current draw of the MCU is essential to prolong battery life, increase system reliability, and improve the overall system performance.

This technical brief gives emphasis to three features of the 8-bit PIC<sup>®</sup> microcontrollers affecting the dynamic power consumption: Idle mode, Doze mode, and Peripheral Module Disable (PMD). This document covers the functionalities, operation and implementation of these modes. A few examples are also presented to highlight the advantages of these modes, especially on applications in which the MCU needs to run most of the time and cannot implement static power modes such as Sleep and Deep Sleep.

### XLP TECHNOLOGY

Microchip's line of PIC microcontrollers implementing the XLP Technology features numerous choices of power modes which can be tailored on-the-fly, allowing the circuit to consume the least possible amount of current at different times.

The nanoWatt Technology (predecessor to XLP Technology) devices first introduced the Idle mode. With the aim of reducing more current consumption, XLP devices introduced more features which include both Doze and PMD. 8-bit PIC MCUs such as the PIC16(L)F183XX, PIC16(L)F188XX and PIC18(L)FK40 product families are only a few of the XLP devices featuring all the three modes. For a complete list of microcontrollers implementing the XLP Technology, visit [www.microchip.com/xlp](http://www.microchip.com/xlp).

### STATIC vs. DYNAMIC POWER

Power consumption in microcontrollers is actually categorized into two components: static power and dynamic power. This section provides a brief description of the two components; however, more emphasis will be given to dynamic power since it is most affected by the Idle, Doze, and PMD low-power features.

#### Static Power

The static power is the power consumed when the system clock is disabled and the code is not running. It is composed mainly of transistor leakage, the power used by supply voltage supervisors (e.g., BOR circuit) and the clocking of monitoring circuits (e.g., Watchdog Timer). Microchip's XLP devices feature the lowest static power consumption in the industry today, through its Sleep and Deep Sleep modes.

#### Dynamic Power

The dynamic power is the power consumed by the device when the system clock is active. It is mainly caused by the switching of CMOS logic during normal operation of the device. The primary factors affecting dynamic power include the supply voltage, switching frequency and the charging and discharging of load capacitance. Equation 1 shows the relationship between these factors.

#### EQUATION 1: DYNAMIC POWER CONSUMPTION OF A CMOS DEVICE FOR A SINGLE CLOCK CYCLE

$$P = V^2 \cdot f \cdot C$$

Equation 1 shows that voltage (V) has the most significant effect on the dynamic power (P) consumption. Hence, the designer must select MCUs that can operate at lower voltages. However, this will require trade-offs between system power and cost if external interfaces have a defined minimum voltage requirement. An additional voltage regulator will not just increase the system cost but may also contribute to a much higher power loss than the dynamic power consumption when operating at a higher voltage.

Frequency ( $f$ ) is the most variable factor among the three. However, reducing the clock frequency will have a negative impact on the MCU performance because it will also reduce the number of instructions that the CPU can execute at a given amount of time. But, there are instances that the CPU operation is neither critical nor necessary at all. The PIC microcontroller Doze feature allows the CPU frequency to slow down while the peripherals run at the configured clock frequency. The ratio of the CPU clock to the peripheral clock is configured through software. When CPU operation is not needed, putting the device in Idle mode can completely disable the CPU clock. For a detailed discussion on the two modes, refer to [Section “Doze Mode”](#) and [Section “Idle Mode”](#).

Clock gating contributes to power reduction by shutting off the clock on unused domains/modules, which in turn eliminate the transistor switching losses. PIC microcontrollers allow the user to control not just the device system clock but also the clock on each module through Peripheral Module Disable (PMD) registers (see [Section “Peripheral Module Disable”](#)).

## PIC® MCU POWER MODES

PIC microcontrollers, especially devices implementing the XLP Technology, allow the user to choose the most appropriate mode to optimize the power consumption of the device in different applications. These modes are summarized in [Table 1](#).

**TABLE 1: DIFFERENT POWER MODES/FEATURES IN 8-BIT PIC MCUs**

Mode/Feature	CPU Clock (CLK <sub>CPU</sub> )	Peripheral Clock (CLK <sub>PER</sub> )	Power Consumption
Deep Sleep	Off	Off	Static
Sleep	Off	Off	Static
Idle	Off	On	Dynamic
Doze	On (CLK <sub>PER</sub> /n)	On	Dynamic
Run	On	On	Dynamic
Peripheral Module Disable (PMD)	On or Off	Selectively-Disabled	Dynamic

As shown in [Table 1](#), Sleep and Deep Sleep affect the static power consumption of the device because the system clock is completely disabled in these modes. Moreover, the peripheral clocks are still active during Doze and Idle which means that the device consumes dynamic power. PMD is actually not a Low-Power mode but it is a feature that can further reduce dynamic power on top of Doze and Idle.

Aside from the modes/features listed above, the user can also manipulate the MCU clock through on-the-fly clock switching and Two-Speed Start-up features.

The next sections will cover the three dynamic power-saving features in more detail.

## DOZE MODE

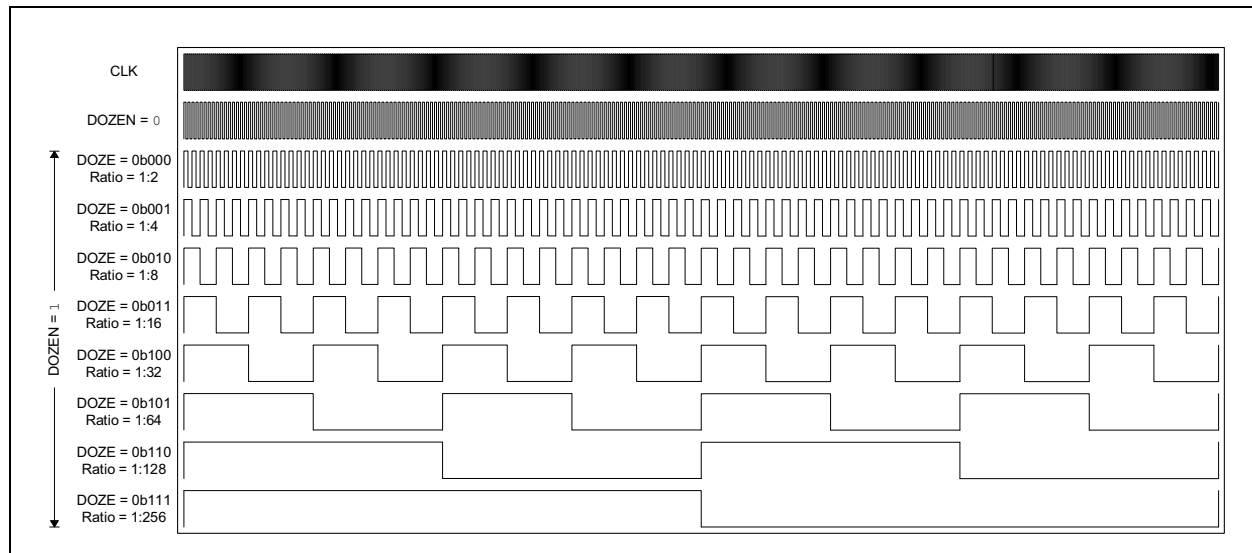
As discussed in [Section “Static vs. Dynamic Power”](#), frequency is one of the main factors affecting the dynamic power consumption. Doze mode allows the user to manage both the CPU and peripheral clock switching frequencies. During this mode, the CPU operation and program memory access are reduced without affecting peripheral operation. This mode is useful in applications requiring the peripheral(s) to run in full speed while performing non-critical CPU operations.

Doze mode is enabled by setting the DOZEN bit to '1' in which the CPU executes instruction cycles according to the DOZE setting. The CPU clock is slowed down with a specific ratio to the peripheral clock which is selected through the DOZE<2:0> bits of the CPUDOZE register.

## Ratio of Instruction to Peripheral Clock Cycles

The simplest method of visualizing Doze mode is by toggling a digital output pin continuously between high and low using different DOZE settings. The timing diagram for this sample application is depicted in [Figure 1](#), using PIC16F18345. As shown in this figure, clearing the DOZEN bit allows the CPU to run at the same clock rate with the peripheral clock. On the contrary, setting this bit to '1' allows the CPU to execute only one instruction out of every  $N$  peripheral clock cycles, as defined by the DOZE<2:0> bits.

**FIGURE 1: TIMING DIAGRAM FOR DIFFERENT DOZE SETTINGS**



Consider the timing diagram of DOZE<2:0> = 010 or 1:8 CPU to peripheral clock ratio in [Figure 1](#). Toggling the I/O pin high and low consumes two instruction cycles and occurs every 16 peripheral clock cycles, which is equal to a 2:16 or simply 1:8.

## Doze Mode and Interrupts

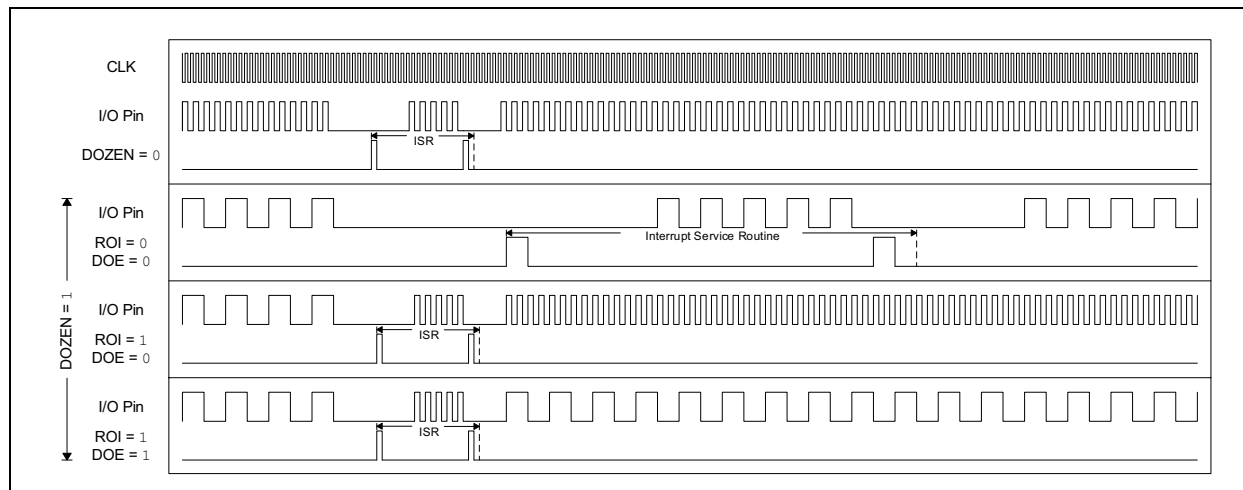
The effects of an interrupt during Doze are determined by the Recover-on-Interrupt (ROI) and Doze-on-Exit (DOE) bits of the CPUDOZE Register.

If an interrupt occurs and the ROI bit is clear at the time of the interrupt, the Interrupt Service Routine (ISR) continues to execute at the rate selected by DOZE<2:0>. However, if the ROI bit is set to '1' when an interrupt occurs, the DOZEN bit is cleared and the CPU executes at full speed during ISR.

The DOE bit determines the CPU execution speed after exit from an ISR. If DOE is cleared, the DOZEN bit does not change and the CPU will continue to execute at a rate equal to its execution speed during ISR. On the other hand, setting DOE to '1' will also set the DOZEN bit to '1' upon exit and the CPU will execute at a slower rate determined by the DOZE<2:0> ratio.

Figure 2 illustrates a sample timing diagram for different ROI and DOE bits setting. This example shows an I/O pin toggled continuously and its behavior before, during, and after an ISR.

**FIGURE 2: SAMPLE TIMING DIAGRAM FOR DIFFERENT ROI AND DOE SETTINGS**



## Effects of Doze on Supply Current

**FIGURE 3: SUPPLY CURRENT vs. DOZE RATIO**

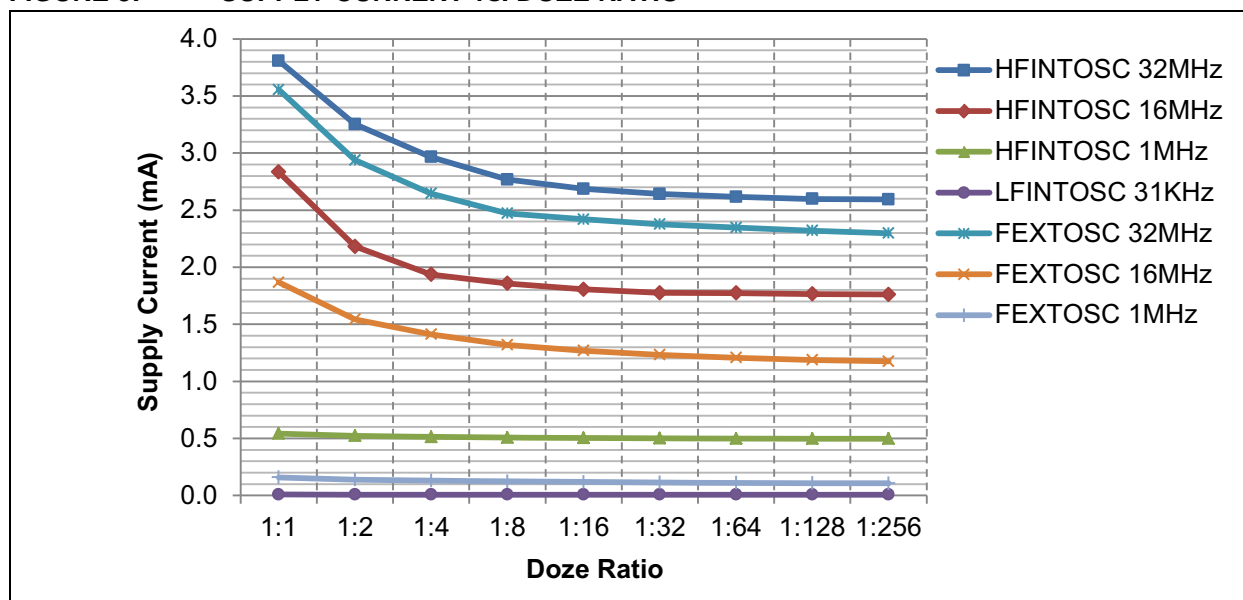


Figure 3 shows the relationship of different DOZE ratios and the supply current using different clock sources at different frequencies. This example uses the PIC16F18345 with a supply voltage of 5V and all unused I/O pins set as inputs and pulled up to V<sub>DD</sub>, to allow only leakage current to pass through (refer to the device data sheet for the test conditions). It can be noticed from the figure that higher DOZE ratios result to lower power consumption. The figure also shows the significance of Doze, especially at higher frequencies where effects are more noticeable.

## IDLE MODE

Idle mode is another dynamic power-saving feature in PIC microcontrollers. It can simply be considered as Doze with a ratio of 1:Infinity in which the CPU clock is completely shut off while the peripherals run at full speed.

This mode can be used to save power from wasteful executions of the CPU such as waiting for interrupts. While there are peripherals that can operate in Sleep mode, it is still not advisable for applications that need peripherals to operate in High Speed because internal RC oscillators typically run at lower frequencies.

### Enabling Idle Mode

PIC16 and PIC18 devices can enter IDLE mode using the `SLEEP` instruction after the IDLE Enable bit is set (`IDLEN=1`). Executing `SLEEP` with `IDLEN=0` will put the device to Sleep mode instead. The location of this bit, however, depends on the device used. For older devices wherein DOZE is unsupported, IDLEN is located in the Oscillator Control Register (`OSCCON<7>`). For new devices wherein DOZE is supported, the bit is located in the DOZE and IDLE Register (`CPUDOZE<7>`).

After issuing `SLEEP` (with IDLE enabled), the peripherals will continue to run with the configured system clock but the CPU will be completely disconnected from the clock source and will stop executing instructions.

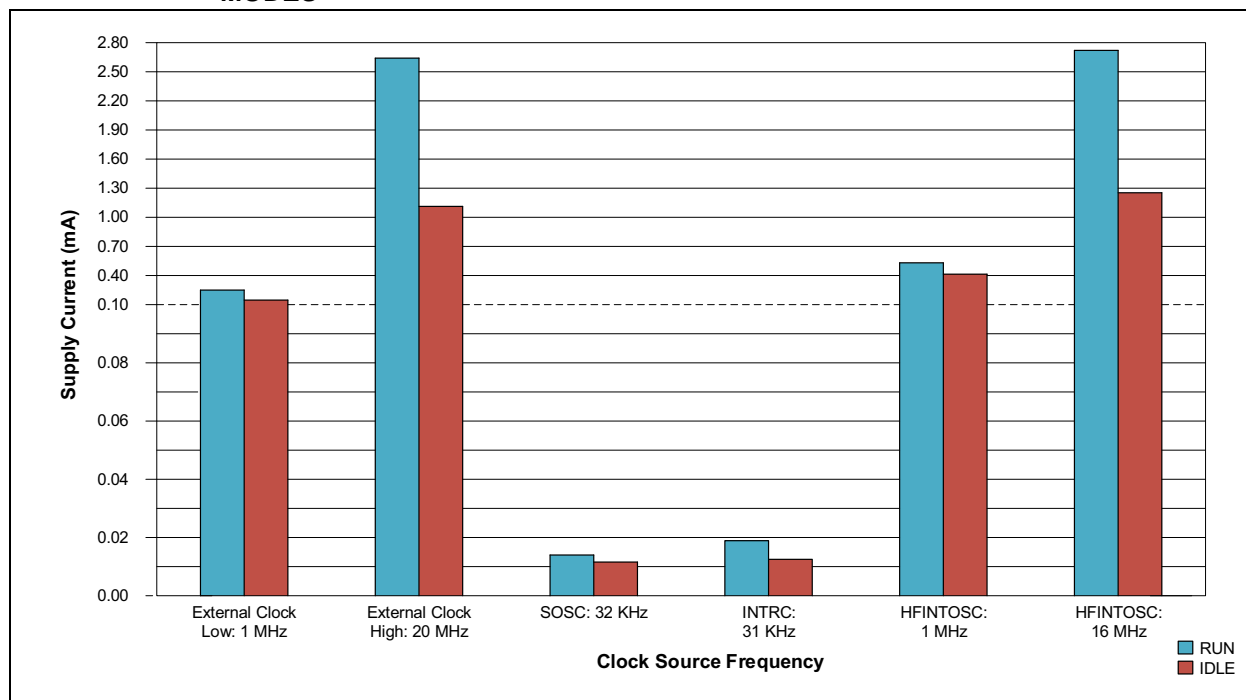
### Exiting Idle Mode

The only way to exit from Idle mode is through wake-up events such as Interrupt, WDT Time-out, or Reset. Devices wake-up on individual interrupts, regardless of the Global Interrupt Enable (GIE) bit setting. The GIE bit determines whether the program will direct the PIC device to the interrupt vector when an interrupt flag bit is set. After a wake-up event, the CPU returns to full operation.

### Effect of Idle Mode on Supply Current

Figure 4 shows the effects of Idle mode on the PIC18F25K50 supply current using different clock sources at different frequencies. The device is supplied with 5V  $V_{DD}$  and all unused I/O pins are configured as outputs pulled down to  $V_{SS}$ , preventing the pins from consuming any additional current (refer to the device data sheet for the test conditions).

**FIGURE 4: RELATIONSHIP OF SUPPLY CURRENT AND FREQUENCY IN RUN AND IDLE MODES**



As shown in Figure 4, there is a significant reduction in supply current during Idle mode compared to Run mode. The differences are more evident when using high-frequency clock sources. It also shows that the device current draw depends upon the clock source. Internal oscillators are enabled when required,

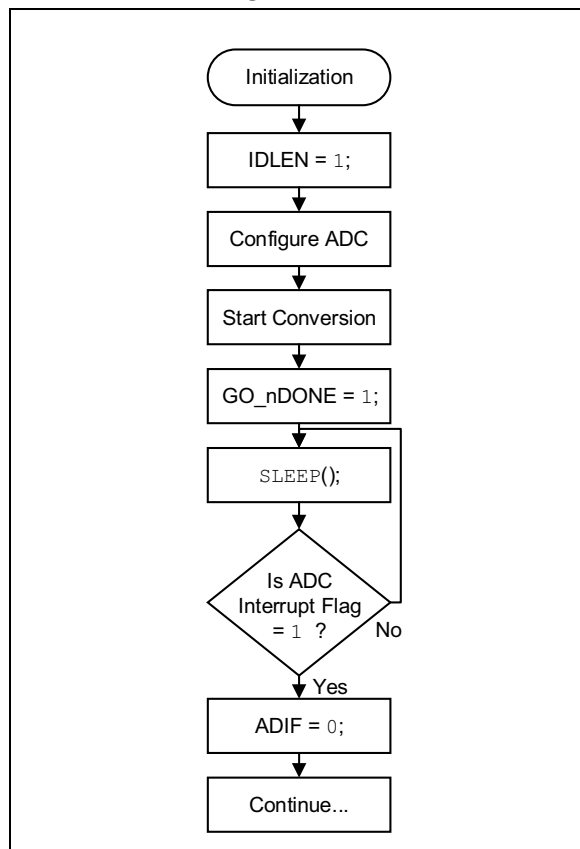
resulting in slightly higher device current consumption when compared with using an external source of the same frequency.

## Sample Application: Idle Mode during High-Speed ADC Conversion

PIC microcontrollers can perform ADC conversion independently from the CPU. To conserve power, the CPU can enter Sleep or Idle mode. Putting the device to Sleep allows the device to consume the lowest possible current. This method, however, imposes limits on the conversion speed. The ADC module can only run in Sleep mode when using the dedicated FRC or ADCRC oscillators as the conversion clock. These clock sources usually run at lower frequencies and are not advisable to use for high-speed conversion. Instead of Sleep, entering Idle mode can eliminate this conversion speed limitation. When the device is in Idle mode, the ADC can still utilize the FOSC system clock which can considerably speed up the ADC conversion time while consuming a reduced amount of current.

There are basically two methods of determining if an ADC conversion is completed: by polling the GO/DONE bit of ADCON0 or through an ADC interrupt. [Figure 5](#) illustrates a flowchart on how to implement Idle mode during ADC conversion using ADC interrupt.

**FIGURE 5: ADC CONVERSION IMPLEMENTING THE IDLE MODE**



A sample code for this application is shown in [Example 1](#).

## EXAMPLE 1: SAMPLE CODE FOR ADC CONVERSION IMPLEMENTING THE IDLE MODE

```

//Enable Idle Mode
OSCCONbits.IDLEN = 1;
/*Insert codes to initialize the
ADC Interrupt*/
/*Insert codes to initialize and
start the ADC conversion*/
ADCON0bits.GO_nDONE = 1;
//Enter Idle Mode
SLEEP();
/*wait for ADC interrupt event then
clear the interrupt flag after
conversion*/
PIR1bits.ADIF = 0;
//continue to main program
  
```

Because ADC interrupt is enabled, the device can wait until the interrupt flag sets after a conversion process is completed. The flag bit is then cleared through software for the next ADC conversion. This method saves more current than continuously polling the bit while waiting for the conversion to finish (see [Figure 6](#)).

[Figure 6](#) shows that putting the device in Idle can significantly reduce current consumption. But, this is still not the lowest possible current that the device can achieve during ADC conversion. Using PMD can further reduce this current. The succeeding sections will discuss the details about this feature.

## PERIPHERAL MODULE DISABLE

The Peripheral Module Disable (PMD) feature of XLP devices provides power reduction in addition to the other dynamic power-saving modes such as Doze and Idle. PMD eliminates wasteful clocking of unused peripherals.

The PMD bits are generically named “xxxMD” and are located in the PMDx Registers. For example, TMR0MD is the PMD bit for Timer TMR0. Setting the PMD bit completely shuts down the peripheral, effectively powering down all circuits and removing all clock sources. When implemented with either the Idle or Doze mode, the device can operate at the lowest possible power.

Some common modules that PMD can disable are timers, comparators, ADC/DAC modules, communication modules, and memory read/writes. Refer to the specific device data sheet for all the PMD supported modules.

### Disabling a Module Using PMD

A specific module can be disabled by setting its respective PMD bit to ‘1’. When disabled, the module’s clock is shut off and its registers are also unusable. The user will be unable to write any data, and all reads will only return “00h”. Dedicated I/O pins either by default or by PPS will be used for the next priority module.

### Enabling a Module Using PMD

Clearing a set PMD bit will re-enable a module in its Reset state. SFR data will reflect the POR Reset values. The module fully activates after at least one instruction cycle; only then the user can modify the SFRs.

### PMD Bits vs. Module’s Enable Bits

Aside from using PMD, clearing a module’s enable bit, usually in the form of “xxxEN”, from its respective control register also halts the peripheral’s operation. Since a module is initialized with “xxxEN=0” by default, this option applies to previously running peripherals which are no longer required. But unlike PMD, users can still read or write its registers and the module continues to receive clock signals. Thus, unused peripherals still draw a minimal amount of current which PMD can completely eliminate. ‘xxxEN’ should be set if the user requires that specific peripheral to run in the later parts of the program.

## Sample PMD Implementation

The ADC conversion code in [Example 1](#) uses Idle mode to reduce power consumption. In this section, PMD is implemented to further minimize the current consumption during ADC conversion by disabling unused peripherals.

Since the sample code only uses the ADC module, the user can disable all the other modules at the beginning of the program by setting their respective PMD bits. The program will run exactly the same but with much lower power consumption. The sample code for this application using PIC18F25K50 is shown in [Example 2](#)

### EXAMPLE 2: PMD REGISTERS SETTING FOR EXAMPLE 1

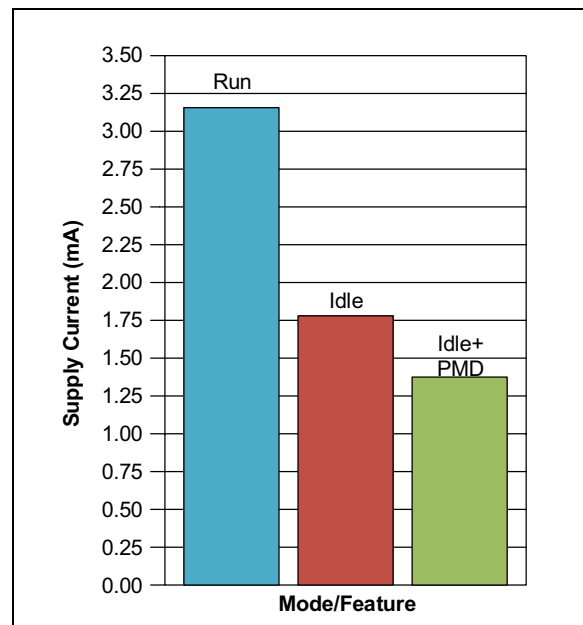
```
/*Set ALL PMD control bits*/
PMD0 = 0xFF;
PMD1 = 0xFF;

/*Clear ADCMD in PMD1<2> to enable
the ADC Module*/
PMD1bits.ADCMD=0;

/*Continue to the Initialization
codes and the main program*/
```

The power consumption for the ADC conversion implementing Idle and PMD on PIC18F25K50 are summarized in [Figure 6](#).

**FIGURE 6: COMPARISON OF SUPPLY CURRENT FOR THE ADC CONVERSION EXAMPLE**



This example utilizes PIC18F25K50 running with an internal 16 MHz clock source and 5V VDD. With the device running in Idle mode, there is a nearly 44% decrease in the supply current. Implementing PMD provides an additional reduction of 13%, resulting to an almost 57% total power savings.

## CONCLUSION

Choosing the appropriate power mode for a specific application is a crucial task for a designer. PIC microcontrollers, especially devices implementing the XLP Technology, provide three useful dynamic power-saving features that can be employed in applications wherein static power-saving modes cannot suffice.

When properly implemented, Doze, Idle and PMD features can reduce the power consumption to the lowest possible, making them most suitable for applications such as serial communications, audio/video conversion, sensor devices, digital communications, and instrumentation.

## ADDITIONAL REFERENCES

- *AN1267 nanoWatt and nanoWatt XLP™ Technologies: An Introduction to Microchip's Low-Power Devices* (DS01267)
- *AN1416 Low-Power Design Guide* (DS01416)
- *Microchip Compiled Tips 'N Tricks Guide* (DS01146)



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