APPLICATION NOTE

The Stand-alone Low Drop Voltage Regulator ATA663203 and the Low Drop Voltage Regulator of the ATA663254

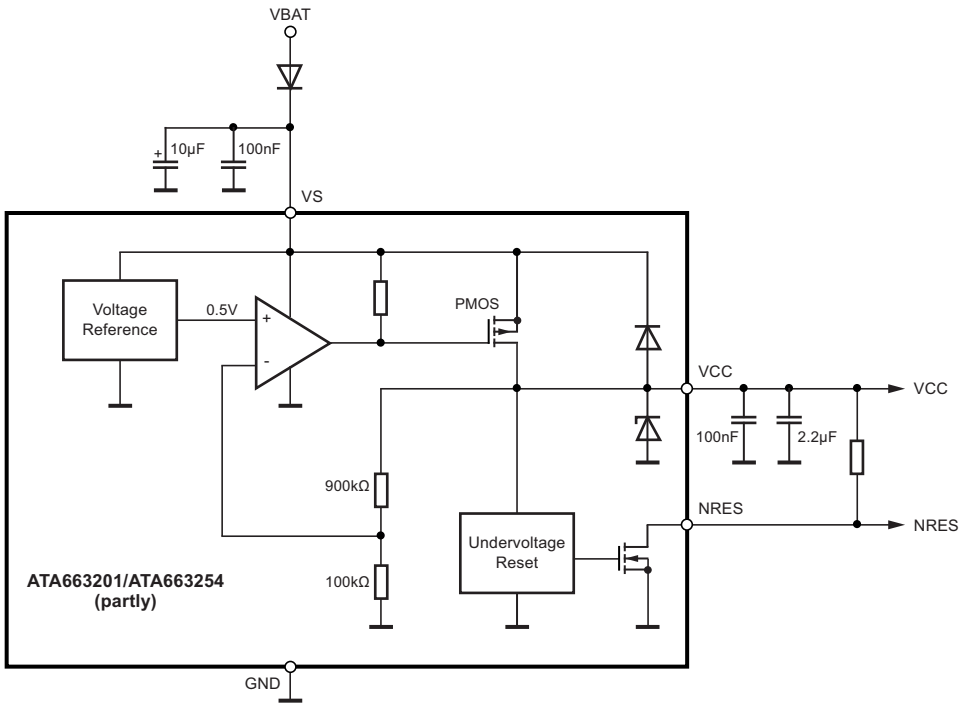
ATAN0091

Introduction

The voltage regulator IC Atmel® ATA663203 and the voltage regulator inside the Atmel ATA663254 LIN-SBC is a low drop regulator (LDO) with a PMOSFET as pass transistor, designed for harsh automotive environments.

The 5V regulator delivers up to 85mA with an voltage accuracy of ±2%. As blocking capacitor a low cost multi layer ceramic capacitor with 0Ω ESR can be used. The SBC current consumption in silent mode (regulator active) is 47µA for 5.5V < V_S < 14V (regulator mode) and outstanding 130µA for linear mode (2V < V_S < 5.5V). The block diagram is shown in Figure 1.

Figure 1. The Voltage Regulator in Principle



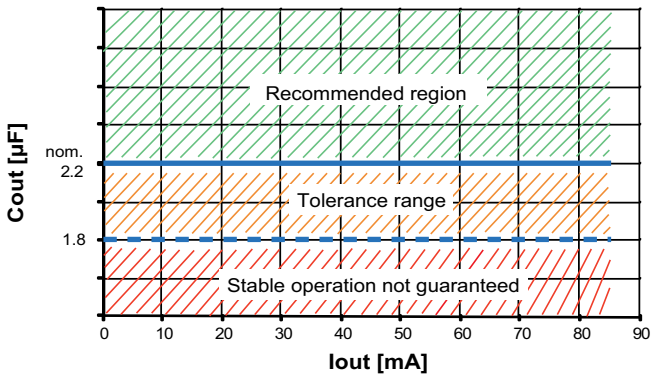
1. Description

An external capacitor is required at the VCC output for compensation and to smooth disturbances from the connected microcontroller or other connected loads. We strongly recommend using a MLC (multi-layer ceramic) capacitor with a minimum capacitance of 1.8µF because due to the very low ESR value of this capacitor the ripple at the output voltage VCC is also very low. We also recommend a second ceramic capacitor with 100nF.

Depending on the application, these capacitor values can be modified by the customer.

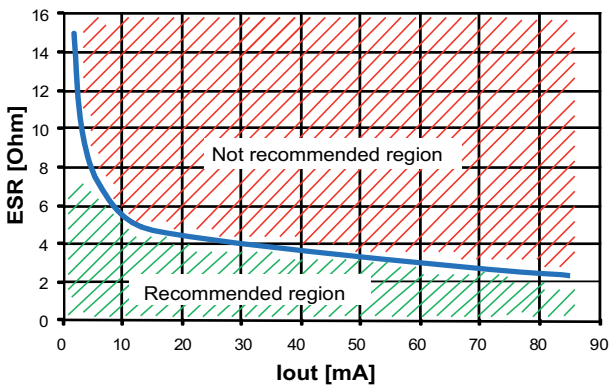
The following typical characteristics and curves have each been measured respectively simulated. The relation between the output current and the required capacitor value is shown in Figure 1-1.

Figure 1-1. Relation between the Output Current and the Required Minimum Capacitor Value (MLC)



The ESR value of the capacitor at the VCC output also affects regulator stability. It is also possible to use a tantalum capacitor at the VCC output, but due to its higher ESR value the VCC voltage ripple also increases. The relation between the ESR value and load current is shown in Figure 1-2.

Figure 1-2. ESR versus Iout



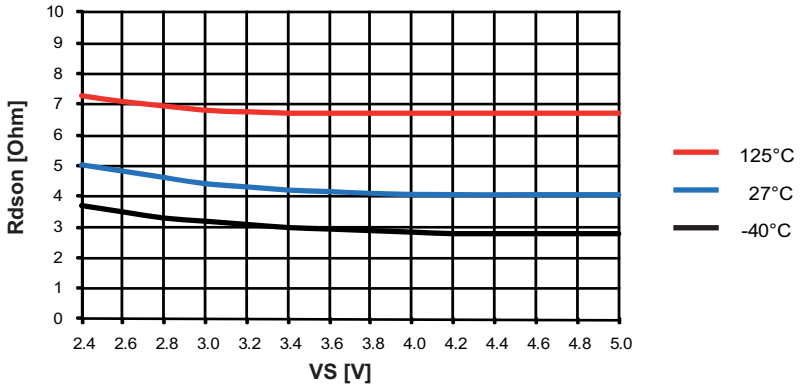
The regulator of the LIN SBC is active in silent, fail-safe, and normal mode. In sleep mode the PMOSFET is switched off and the internal voltage divider (typ. 1MΩ) together with the external load pulls the VCC line down to GND.

If the supply voltage V_S drops under the nominal value of VCC, the PMOS transistor is switched on completely, this means the output voltage VCC is VS – VD (voltage drop).

The voltage drop VD = Iout × RDSON.

The difference between VS and VCC in this situation depends on the RDSON. The characteristic of this parameter is shown in Figure 1-3 on page 3.

Figure 1-3. RDSON of the PMOS Pass Transistor



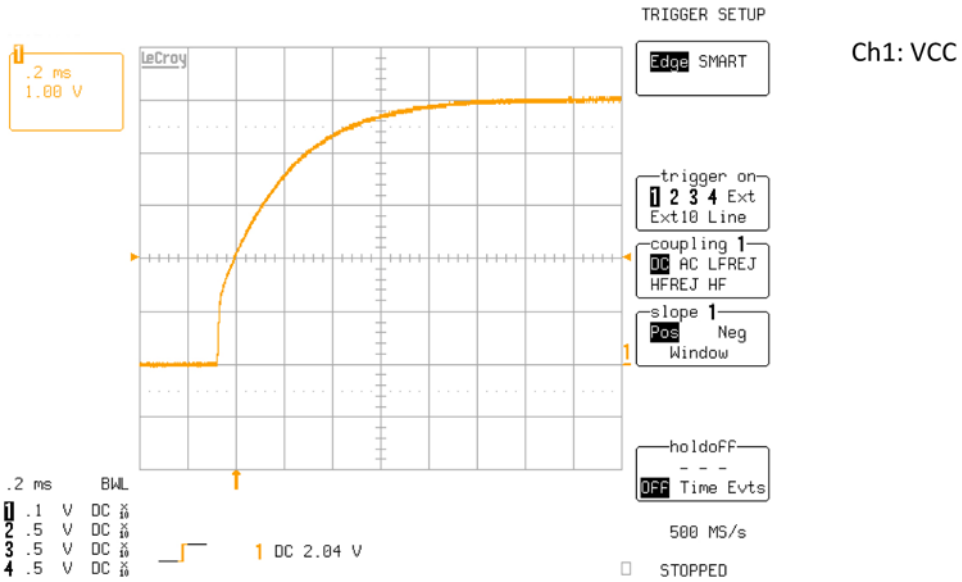
The current consumption of the LIN SBC in silent and fail-safe mode is always below **170µA** even if the supply voltage V_S is lower than the nominal output voltage VCC.

Behavior during supply voltage ramp-up and ramp-down is described in more detail in the corresponding datasheet.

2. Ramp-up Behavior

When the Atmel® ATA663254 wakes up from sleep mode, the VCC voltage ramps up as follows (see Figure 2-1).

Figure 2-1. Ramp-up of VCC at Wake-Up from Sleep Mode, Cout = 2.2µF, no External Load Current



The figure shows that VCC ramps up without any overshot.

3. Load Current Change - Step Response

Figure 3-1 and Figure 3-2 show the step response for a 50mA load change with various blocking capacitors.

Figure 3-1. Transient Response at Cout = 2.2µF Ceramic, 100nF Ceramic Parallel

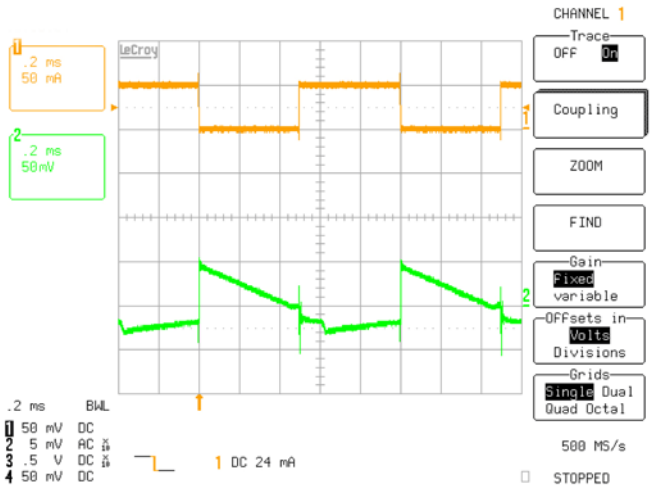
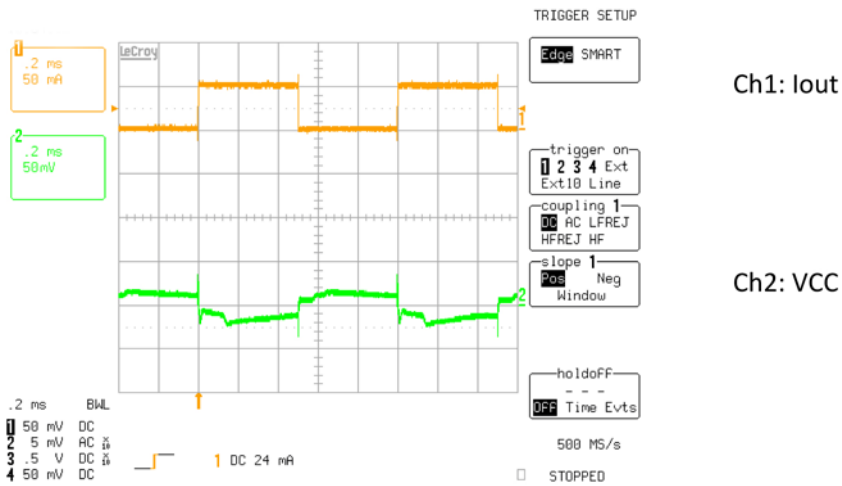


Figure 3-2. Transient Response at Cout = 22µF Ceramic, 100nF Ceramic Parallel



Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**