AVR096: Migrating from ATmega128 to AT90CAN128

8-bit AVR® Microcontroller

Application Note

This application note is a guide to help current ATmega128 users convert existing designs to AT90CAN128. The information given will also help users migrating from any ATmega microcontroller to AT90CAN128. Additionally, the electrical characteristics of the AT90CAN128 are different than those of ATmega128. Check the datasheets of both of these products for detailed information.

Features

The main features of the ATmega128 have been carried over to the AT90CAN128.

- **Advance RISC Architecture**
- **128 KB Flash & 4 KB E^2PROM with Software Security**
- **4 KB internal RAM & 64 KB external RAM**
- **Watchdog Timer, 8-bit Timer & 8-bit Real Time Timer & Two 16-bit Timers**
- **8-channel 10-bit SAR ADC & Analog Comparator**
- **Dual USART, SPI & TWI**
- **8 External Interrupts**
- **POR/PFD & Sleep Modes**
- **Operating Voltage from 2.7V up to 5.5V**
- **16 MHz Maximum Frequency (5V range)**

The more important evolution is the full-CAN (Controller Area Network) peripheral implementation in the AT90CAN128.

Other features have been added such as three General Purpose Registers (one of them is bit-accessible) and two Digital Input Disable Registers for analog I/Os.

To be compatible with the new generation of 8-bit AVR microcontrollers (i.e. ATmega169), the register mapping had been re-modelled. This new distribution restructures the addressing to improve its coherence and thus to privilege readability.

The AT90CAN128 also has some improvements on Timers, Analog to Digital Converter and Clocks.

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Pin Configuration

The AT90CAN128 is functionally pin compatible with ATmega128. Certain pins have been upgraded with regard to their associated alternate functions, the change of the timers/counters index and the voluntary removal ATmega103 compatibility.

Figure 1. Pin Configuration

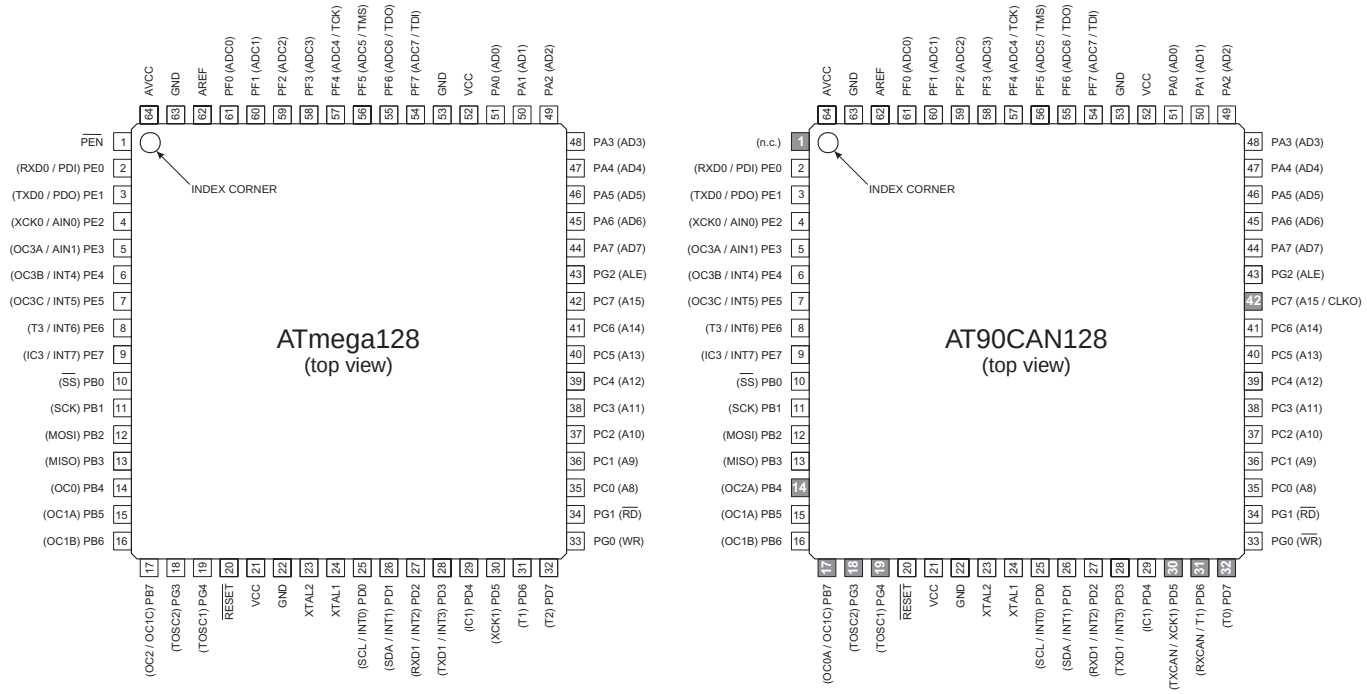

Table 1. Changed Pins

Pin	ATmega128	AT90CAN128	Comments for AT90CAN128
1	$\overline{\text{PEN}}$	(n.c.) Not connected	Removal ATmega103 compatibility mode.
14	PB4 (OC0)	PB4 (OC2A)	The asynchronous-Real Time Timer/Counter index becomes 2 instead of 0.
17	PB7 (OC2/OC1C)	PB7 (OC0A/OC1C)	The synchronous 8-bit Timer/Counter index becomes 0 instead of 2.
18	PG3 (TOSC2)	PG3 (TOSC2)	No pin name changes, the TOSC crystal is always connected to the Asynchronous-Real Time Timer/Counter but the index of this timer/counter becomes 2 instead of 0.
19	PG4 (TOSC1)	PG4 (TOSC1)	
30	PD5 (XCK1)	PD5 (XCK1/TXCAN)	Addition of CAN I/O's as alternate functions. These alternate functions are enabled once the CAN peripheral is switched "ON".
31	PD6 (T1)	PD6 (T1/RXCAN)	
32	PD7 (T2)	PD7 (T0)	The synchronous 8-bit Timer index becomes 0 instead of 2.
42	PC7 (A15)	PC7 (A15/CLKO)	Addition of Clock output (CLKO) as alternate function. This alternate function is enabled/disabled by CKOUT fuse of the Fuse Low Byte.

AVR CORE

System Clock

Sources

Four sources for system clock are available in AT90CAN128:

- On-chip oscillator for external crystal or ceramic resonator
- On-chip oscillator for external low-frequency crystal
- Calibrated internal RC oscillator
- External clock

Unlike ATmega128, no external RC network can be connected to XTAL1 pin.

Amplifier Mode

XTAL1 and XTAL2 are input and output, respectively, from an inverting amplifier of the on-chip oscillators.

On ATmega128, the CKOPT fuse selects between two oscillator amplifier modes. If CKOPT is programmed, the oscillator output oscillates with a full rail-to-rail swing on the output. If CKOPT is unprogrammed, the oscillator has a smaller output swing.

This mode is not present on ATmega128CAN11.

Prescaler

The Clock Prescaler Register - CLKPR of ATmega128CAN11, replaces the XTAL Divide Control Register - XDIV. The clock division factor (CLKPS[3..0] field of CLKPR) is now a 2^n number from 1 up to 256.

Table 1. Clock Prescaler Select

ATmega128		AT90CAN128	
XDIV[6..0]	**Frequency**	**CLKPS[3..0]**	**Frequency**
d	$f_{CLK} = f_{Source\ Clock} / (129-d)$	0x0	$f_{CLK} = f_{Source\ Clock}$
		0x1	$f_{CLK} = f_{Source\ Clock} / 2$
		0x2	$f_{CLK} = f_{Source\ Clock} / 4$
		0x3	$f_{CLK} = f_{Source\ Clock} / 8$
		0x4	$f_{CLK} = f_{Source\ Clock} / 16$
		0x5	$f_{CLK} = f_{Source\ Clock} / 32$
		0x6	$f_{CLK} = f_{Source\ Clock} / 64$
		0x7	$f_{CLK} = f_{Source\ Clock} / 128$
		0x8	$f_{CLK} = f_{Source\ Clock} / 256$
		0x9 to 0xF	Reserved

CLKDIV8 Fuse

A new fuse (CKDIV8 - bit 7 of Fuse Low Byte) determines the initial value of the clock prescaler in AT90CAN128. If CKDIV8 is unprogrammed, the prescaler is initialized with “0x0”. Programmed, the prescaler is initialized with “0x3”, giving a division factor of “8” at start-up.

Table 2. Clock Prescaler Initialization

ATmega128		AT90CAN128		
XDIV[6..0]	**Frequency**	**CKDIV8**	**CLKPS[3..0]**	**Frequency**
0x00	$f_{CLK} = f_{Source\ Clock} / 129$	1	0x0	$f_{CLK} = f_{Source\ Clock}$
		0	0x3	$f_{CLK} = f_{Source\ Clock} / 8$

Oscillator Calibration

During reset, hardware loads the calibration byte into the OSCCAL Register and thereby automatically calibrates the internal RC Oscillator. OSCCAL Register is accessible by software. In ATmega128, 8 bits of OSCCAL Register are used, in AT90CAN128, only the 7 low significant bits are used.

Sleep Modes

The Extended Standby sleep mode of ATmega128 disappears in the sleep mode list of AT90CAN128.

The active clock domains and wake-up sources in the different sleep modes does not change.

Table 3. Sleep Modes

	ATmega128	AT90CAN128
Sleep Mode Select SM[2..0]		
0	Idle	*Idem*
1	ADC Noise Reduction	*Idem*
2	Power-down	*Idem*
3	Power-save	*Idem*
4	*"reserved"*	*Idem*
5	*"reserved"*	*Idem*
6	Standby	*Idem*
7	Extended Standby	*"reserved"*

Reset Logic

The AT90CAN128 reset logic differs from the ATmega128 one by the Brown-Out Detection (BOD). This is due to a new set of fuse bits (See "Fuse Bits" on page 7.).

Table 4. Brown-Out Detection

ATmega128		AT90CAN128	
Detected level Typ. V_{BOT}	**Setting**	**Detected level Typ. V_{BOT}**	**Setting**
Disable	BODEN(1)="1"	Disable	BODLEVEL[2..0](3)="111"
4.0 V	BODEN(1)="0" BODLEVEL(2)="0"	4.1 V (4)	BODLEVEL[2..0](3)="110"
		4.0 V (4)	BODLEVEL[2..0](3)="101"
		3.9 V (4)	BODLEVEL[2..0](3)="100"
		3.8 V (4)	BODLEVEL[2..0](3)="011"
2.7 V	BODEN(1)="0" BODLEVEL(2)="1"	2.7 V (4)	BODLEVEL[2..0](3)="010"
		2.6 V (4)	BODLEVEL[2..0](3)="001"
		2.5 V (4)	BODLEVEL[2..0](3)="000"

Notes: 1. BODEN: Fuse Bit 6 - Fuse Low Byte of ATmega128.
2. BODLEVEL: Fuse Bit 7 - Fuse Low Byte of ATmega128.
3. BODLEVEL[2..0]: Fuse Bits 3, 2 & 1 - Extended Fuse Byte of AT90CAN128.
4. Theorical values, refer to AT90CAN128 data sheet.

Interrupt Table

There are two additional interrupts in AT90CAN128, the CAN interrupts. All the Timer/Counter1 interrupts have been clustered (c.f. TIMER1 COMPC interrupt). The interrupts are compatible up to the 14th vector.

Table 5. Interrupt Table

Vector No.	Program Address(2)	ATmega128	AT90CAN128
		Interrupt Source	**Interrupt Source**
1	0x0000(1)	External Reset pin, POR, BOR, WD Reset & JTAG AVR Reset	*Idem*
2	0x0002	External Interrupt Request 0	*Idem*
3	0x0004	External Interrupt Request 1	*Idem*
4	0x0006	External Interrupt Request 2	*Idem*
5	0x0008	External Interrupt Request 3	*Idem*
6	0x000A	External Interrupt Request 4	*Idem*
7	0x000C	External Interrupt Request 5	*Idem*
8	0x000E	External Interrupt Request 6	*Idem*
9	0x0010	External Interrupt Request 7	*Idem*
10	0x0012	T/C2 Compare Match	*Idem*
11	0x0014	T/C2 Timer Overflow	*Idem*
12	0x0016	T/C1 Capture Event	*Idem*
13	0x0018	T/C1 Compare Match A	*Idem*

Table 5. Interrupt Table (Continued)

Vector No.	Program Address(2)	ATmega128	AT90CAN128
		Interrupt Source	**Interrupt Source**
14	0x001A	T/C1 Compare Match B	*Idem*
15	0x001C	T/C1 Timer Overflow	T/C1 Compare Match C
16	0x001E	T/C0 Compare Match	T/C1 Timer Overflow
17	0x0020	T/C0 Timer Overflow	T/C0 Compare Match
18	0x0022	SPI Transfer Complete	T/C0 Timer Overflow
19	0x0024	USART0, Rx Complete	CAN Transfer Complete or Error
20	0x0026	USART0 Data Register Empty	CAN Timer Overrun
21	0x0028	USART0, Tx Complete	SPI Transfer Complete
22	0x002A	ADC Conversion Complete	USART0, Rx Complete
23	0x002C	EEPROM Ready	USART0 Data Register Empty
24	0x002E	Analog Comparator	USART0, Tx Complete
25	0x0030	T/C1 Compare Match C	Analog Comparator
26	0x0032	T/C3 Capture Event	ADC Conversion Complete
27	0x0034	T/C3 Compare Match A	EEPROM Ready
28	0x0036	T/C3 Compare Match B	T/C3 Capture Event
29	0x0038	T/C3 Compare Match C	T/C3 Compare Match A
30	0x003A	T/C3 Timer Overflow	T/C3 Compare Match B
31	0x003C	USART1, Rx Complete	T/C3 Compare Match C
32	0x003E	USART1 Data Register Empty	T/C3 Timer Overflow
33	0x0040	USART1, Tx Complete	USART1, Rx Complete
34	0x0042	TWI Interface	USART1 Data Register Empty
35	0x0044	Store Program Memory Ready	USART1, Tx Complete
36	0x0046	/	TWI Interface
37	0x0048	/	Store Program Memory Ready

Notes: 1. When the BOOTRST Fuse is programmed, the device will jump to the Boot Loader address at reset.
2. When the IVSEL bit in MCUCR is set, Interrupt Vectors will be moved to the start of the Boot Flash Section. The address of each Interrupt Vector will then be the address in this table added to the start address of the Boot Flash Section.

ATmega103 Compatibility

The ATmega103 compatibility mode of ATmega128 does not exist in AT90CAN128. For further information, please refer to “ATmega103 and ATmega128 Compatibility” section of ATmega128 datasheet.

Memory

Fuse Bits

Extended Fuse Byte

All the valid bits of Extended Fuse Byte of AT90CAN128 are different from those of ATmega128.

Table 6. Extended Fuse Byte

Bit	ATmega128		AT90CAN128	
	Name	Description	Name	Description
7	-	-	-	-
6	-	-	-	-
5	-	-	-	-
4	-	-	-	-
3	-	-	BODLEVEL2	Brown-out detector trigger level
2	-	-	BODLEVEL1	
1	M103C	ATmega103 compatibility mode	BODLEVEL0	
0	WDTON	Watchdog Timer always “on”	TA0SEL	(Reserved for factory tests)

Fuse High Byte

Only the bit number 4 of Fuse High Byte of AT90CAN128 is different from the one in ATmega128.

Table 7. Fuse High Byte

Bit	ATmega128		AT90CAN128	
	Name	Description	Name	Description
7	OCDEN	Enable OCD	*Idem*	*Idem*
6	JTAGEN	Enable JTAG	*Idem*	*Idem*
5	SPIEN	Enable serial program and data downloading	*Idem*	*Idem*
4	CKOPT	Oscillator option	WDTON	Watchdog Timer always “on”
3	EESAVE	E^2PROM is preserved through the chip erase	*Idem*	*Idem*
2	BOOTSZ1	Select boot size	*Idem*	*Idem*
1	BOOTSZ0		*Idem*	
0	BOOTRST	Select reset vector	*Idem*	*Idem*

Fuse Low Byte

Bits number 7 and 6 of Fuse Low Byte of AT90CAN128 are different from those of ATmega128.

Table 8. Fuse Low Byte

Bit	ATmega128		AT90CAN128	
	Name	Description	Name	Description
7	BODLEVEL	Brown-out detector trigger level	CKDIV8	Divide clock by 8 at start-up
6	BODEN	Brown-out detector enable	CKOUT	Clock output enable
5	SUT1	Select start-up time	*Idem*	*Idem*
4	SUT0		*Idem*	
3	CLKSEL3	Select clock source	*Idem*	*Idem*
2	CLKSEL2		*Idem*	
1	CLKSEL1		*Idem*	
0	CLKSEL0		*Idem*	

Signature Bytes

Because AT90CAN128 and ATmega128 mainly differ by their I/O modules, only the third byte changes.

Table 9. Signature Bytes

Byte	Description	ATmega128	AT90CAN128
		Value	Value
0	Manufacturer	0x1E (ATMEL)	*Idem*
1	Flash Memory Size	0x97 (128 KB)	*Idem*
2	Device	0x02	0x81

JTAG Identification Register

For the same reason as signature bytes, only the part number field changes (revision field not included).

Table 10. JTAG Identification Register

Field	ATmega128		AT90CAN128	
	Field Value	Register Value	Field Value	Register Value
Device Revision	0x0[1]	0x0970201F	0x0[1]	0x0978101F
Part Number	0x9702		0x9781	
Manufacturer ID (+ lsb=0)	0x01E		*Idem*	
lsb	0x1		*Idem*	

Notes: 1. Refer to data sheets for the last revision field value.

I/O Modules

External Memory Interface

In AT90CAN128, CLKO (Clock output) has been added as alternate function of PC7 (Port C - Bit 7). Another alternate function of PC7 is A15 (external memory interface address 15). Because CLKO is enabled/disabled by CKOUT fuse, it has priority over any external memory interface setting.

If CLKO is enabled, the minimum setting of XMM field in External Memory Control Register B - XMCRB - must be “001” to be in agreement with the PC7 configuration.

Synchronous 8-bit Timer/Counter

Index/Name

The Timer/Counter2 of ATmega128 becomes Timer/Counter0 in AT90CAN128. The features of the Timer/Counter are maintained. The I/O pin locations remain unchanged (See “Pin Configuration” on page 2).

Asynchronous 8-bit Timer/Counter

Index/Name

The Timer/Counter0 of ATmega128 becomes Timer/Counter2 in AT90CAN128. The features of the Timer/Counter are maintained, especially the asynchronous mode. The I/O pin locations remain unchanged (See “Pin Configuration” on page 2.).

Asynchronous Clock

An external clock source can be applied to PG4 (TOSC1) pin for asynchronous operation on Timer/Counter2 of AT90CAN128. In this configuration, PG3 (TOSC2) is available as standard I/O.

Table 11. Asynchronous Timer Sources

ATmega128		AT90CAN128		
Source	**Setting**	**Source**	**Setting**	
CLK_{IO}	Default at start-up	CLK_{IO}	Default at start-up	
	AS0[1]=“0”		AS2[2]=“0”	EXCLK[3]=“0”
TOSC oscillator for external watch crystal	AS0[1]=“1”	TOSC oscillator for ext. watch crystal	AS2[2]=“1”	EXCLK[3]=“0”
		External clock on TOSC1 pin	AS2[2]=“1”	EXCLK[3]=“1”

Notes: 1. AS0: Bit 3 - Timer/Counter0 ASSR (ATmega128).
2. AS2: Bit 3 - Timer/Counter2 ASSR (AT90CAN128).
3. EXCLK: Bit 4 - Timer/Counter2 ASSR (AT90CAN128).

Synchronous Timer/Counter Prescaler

The prescaler reset of the synchronous timers/counters of ATmega128 is named PRS321 due to the index of the three timers/counters driven by this prescaler.

On AT90CAN128, automatically its name becomes PRS310.

Asynchronous Timer/Counter Prescaler

The prescaler reset of the asynchronous timers/counter of ATmega128 is named PRS0 due to the index of the timer/counter driven by this prescaler.

On AT90CAN128, automatically its name becomes PRS2.

ADC

A new feature has been added in ADC of AT90CAN128: the auto triggering.

A conversion can be triggered automatically by various sources. Auto Triggering is enabled by setting the ADC Auto Trigger Enable bit, ADATE in ADCSRA. The trigger source is selected by setting the ADC Trigger Select bits, ADTS in ADCSRB. When a positive edge occurs on the selected trigger signal, the ADC prescaler is reset and a conversion is started.

Table 12. ADC Conversions

ATmega128		AT90CAN128	
Mode	**Setting**	**Mode**	**Setting**
Single conversion start	ADCS(1)="1" ADFR(2)="0"	*Single conversion* start	ADCS(1)="1" ADATE(3)="0"
Free running mode start	ADCS(1)="1" ADFR(2)="1"	Starting with trigger source: *Free running mode*	ADCS(1)="1" ADATE(3)="1" ADST[2..0](4)="000"
-	-	Starting with trigger source: *Analog comparator*	ADCS(1)="1" ADATE(3)="1" ADST[2..0](4)="001"
-	-	Starting with trigger source: *Ext. Int. Request 0*	ADCS(1)="1" ADATE(3)="1" ADST[2..0](4)="010"
-	-	Starting with trigger source: *T/C0 compare match*	ADCS(1)="1" ADATE(3)="1" ADST[2..0](4)="011"
-	-	Starting with trigger source: *T/C0 overflow*	ADCS(1)="1" ADATE(3)="1" ADST[2..0](4)="100"
-	-	Starting with trigger source: *T/C1 compare match B*	ADCS(1)="1" ADATE(3)="1" ADST[2..0](4)="101"
-	-	Starting with trigger source: *T/C1 overflow*	ADCS(1)="1" ADATE(3)="1" ADST[2..0](4)="110"
-	-	Starting with trigger source: *T/C1 capture event*	ADCS(1)="1" ADATE(3)="1" ADST[2..0](4)="111"
Free running mode stop	ADFR(2)="0"	*Free running mode* stop	ADATE(3)="0"

Notes: 1. ADCS: Bit 6 - ADCSRA (ATmega128 & AT90CAN128).
2. ADFR: Bit 5 - ADCSRA (ATmega128).
3. ADATE: Bit 5 - ADCSRA (AT90CAN128).
4. ADST[2..0]: Bits 2..0 - ADCSRB (AT90CAN128).

I/O Registers

The I/O space definition of the ATmega128 and the AT90CAN128 is shown in the “Register Summary” section of the datasheets respectively.

All I/O registers are placed in the I/O space from address 0x20 up to 0xFF. All I/O locations may be accessed by the LD/LDS/LDD and ST/STS/STD instructions.

- The I/O registers from 0x20 up to 0x5F may be also accessed by the specific instructions IN and OUT **but** 0x20 must be subtracted to these addresses.
- I/O registers within the address range 0x20 - 0x3F also are directly **bit-accessible** using the SBI/CBI/SBIS/SBIC instructions **but** 0x20 must be subtracted to these addresses.
  Some of the status flags are cleared by writing a logical one. Note that the SBI instructions operates on such status flags in this address range.
- For the Extended I/O space from 0x60 - 0xFF in SRAM, **only** the ST and LD instructions can be used.

Note: **Migrating an assembler source code from ATmega128 to AT90CAN128 may force to change the assembler line of an I/O register access**.

Table 13. I/O Registers

ATmega128										AT90CAN128									
		Register Content										Register Content							
Add.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Add.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
(0x9D)	UCSR1C	-	UMSEL1	UPM1 [1,0]		USBS1	UCSZ1 [1,0]		UCPOL1	(0xCA)	*Idem*	*Idem*							
(0x9C)	UDR1	USART1 I/O Data Register								(0xCE)	*Idem*	*Idem*							
(0x9B)	UCSR1A	RXC1	TXC1	UDRE1	FE1	DOR1	UPE1	U2X1	MPCM1	(0xC8)	*Idem*	*Idem*							
(0x9A)	UCSR1B	RXCIE1	TXCIE1	UDRIE1	RXEN1	TCEN1	UCSZ12	RXB81	TXB81	(0xC9)	*Idem*	*Idem*							
(0x99)	UBRR1L	USART1 Baud Rate Register Low Byte								(0xCC)	*Idem*	*Idem*							
(0x98)	UBRR1H	-				USART1 Baud Rate Register High				(0xCD)	*Idem*	*Idem*							
(0x95)	UCSR0C	-	UMSEL0	UPM0 [1,0]		USBS0	UCSZ0 [1,0]		UCPOL0	(0xC2)	*Idem*	*Idem*							
(0x90)	UBRR0H	-				USART0 Baud Rate Register High				(0xC5)	*Idem*	*Idem*							
(0x8C)	TCCR3C	FOC3A	FOC3B	FOC3C	-					(0x92)	*Idem*	*Idem*							
(0x8B)	TCCR3A	COM3A [1,0]		COM3B [1,0]		COM3C [1,0]		WGM3 [1,0]		(0x90)	*Idem*	*Idem*							
(0x8A)	TCCR3B	ICNC3	ICES3	-	WGM3 [3,2]		CS3[2..0]			(0x91)	*Idem*	*Idem*							
(0x89)	TCNT3H	T/C3 Counter Register High Byte								(0x95)	*Idem*	*Idem*							
(0x88)	TCNT3L	T/C3 Counter Register Low Byte								(0x94)	*Idem*	*Idem*							

Table 13. I/O Registers (Continued)

ATmega128										AT90CAN128									
		Register Content										Register Content							
Add.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Add.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
(0x87)	OCR3AH	T/C3 Output Compare A Register High Byte								(0x99)	*Idem*	*Idem*							
(0x86)	OCR3AL	T/C3 Output Compare A Register Low Byte								(0x98)	*Idem*	*Idem*							
(0x85)	OCR3BH	T/C3 Output Compare B Register High Byte								(0x9B)	*Idem*	*Idem*							
(0x84)	OCR3BL	T/C3 Output Compare B Register Low Byte								(0x9A)	*Idem*	*Idem*							
(0x83)	OCR3CH	T/C3 Output Compare C Register High Byte								(0x9D)	*Idem*	*Idem*							
(0x82)	OCR3CL	T/C3 Output Compare C Register Low Byte								(0x9C)	*Idem*	*Idem*							
(0x81)	ICR3H	T/C3 Input Capture Register High Byte								(0x97)	*Idem*	*Idem*							
(0x80)	ICR3L	T/C3 Input Capture Register Low Byte								(0x96)	*Idem*	*Idem*							
(0x7D)	ETIMSK	-	-	ICIE3	OCIE3A	OCIE3B	TOIE3	OCIE3C	OCIE1C	(0x6F)	TIMSK1	-	-	ICIE1	-	OCIE1C	OCIE1B	OCIE1A	TOIE1
										(0x71)	TIMSK3	-	-	ICIE3	-	OCIE3C	OCIE3B	OCIE3A	TOIE3
(0x7C)	ETIFR	-	-	ICF3	OCF3A	OCF3B	TOV3	OCF3C	OCF1C	0x16-(0x36)	TIFR1	-	-	ICF1	-	OCF1C	OCF1B	OCF1A	TOV1
										0x18-(0x38)	TIFR3	-	-	ICF3	-	OCF3C	OCF3B	OCF3A	TOV3
(0x7A)	TCCR1C	FOC1A	FOC1B	FOC1C	-					(0x82)	*Idem*	*Idem*							
(0x79)	OCR1CH	T/C1 Output Compare C Register High Byte								(0x8D)	*Idem*	*Idem*							
(0x78)	OCR1CL	T/C1 Output Compare C Register Low Byte								(0x8C)	*Idem*	*Idem*							
(0x74)	TWCR	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	-	TWIE	(0xBC)	*Idem*	*Idem*							
(0x73)	TWDR	TWI I/O Data Register								(0xBB)	*Idem*	*Idem*							
(0x72)	TWAR	TWA[6..0]							TWGCE	(0xBA)	*Idem*	*Idem*							
(0x71)	TWSR	TWS[7..3]					-	TWPS [1,0]		(0xB9)	*Idem*	*Idem*							
(0x70)	TWBR	TWI Bit Rate Register								(0xB8)	*Idem*	*Idem*							
(0x6F)	OSCCAL	CAL[7..0]								(0x66)	*Idem*	-	CAL[6..0]						
(0x6D)	XMCRA	-	SRL[2..0]			SRW0 [1,0]		SRW11	-	(0x74)	XMCRA	SRE	SRL[2..0]			SRW11	SRW10	SRW0 [1,0]	

Table 13. I/O Registers (Continued)

ATmega128										AT90CAN128									
		Register Content										Register Content							
Add.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Add.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
(0x6C)	XMCRB	XMBK	-	-	-	-	XMM[2..0]			(0x75)	*Idem*	*Idem*							
(0x6A)	EICRA	ISC3 [1,0]		ISC2 [1,0]		ISC1 [1,0]		ISC0 [1,0]		(0x69)	*Idem*	*Idem*							
(0x68)	SPMCSR	SPMIE	RWWSB	-	SWWSRE	BLBSET	PGWRT	PGERS	SPMEM	0x37-(0x57)	*Idem*	*Idem*							
(0x65)	PORTG	-	-	-	PORTG[4..0]					0x14-(0x34)	*Idem*	*Idem*							
(0x64)	DDRG	-	-	-	DDG[4..0]					0x13-(0x33)	*Idem*	*Idem*							
(0x63)	PING	-	-	-	PING[4..0]					0x12-(0x32)	*Idem*	*Idem*							
(0x62)	PORTF	PORTF[7..0]								0x11-(0x31)	*Idem*	*Idem*							
(0x61)	DDRF	DDF[7..0]								0x10-(0x30)	*Idem*	*Idem*							
0x3F-(0x5F)	SREG	I	T	H	S	V	N	Z	C	*Idem*	*Idem*	*Idem*							
0x3E-(0x5E)	SPH	Stack Pointer Register High Byte								*Idem*	*Idem*	*Idem*							
0x3D-(0x5D)	SPL	Stack Pointer Register Low Byte								*Idem*	*Idem*	*Idem*							
0x3C-(0x5C)	XDIV (see page 3)	XDIVEN	XDIV[6..0]							(0x61)	CLKPR	CLKPCE	-	-	-	CLKPS[3..0]			
0x3B-(0x5B)	RAMPZ	-	-	-	-	-	-	-	RAMPZ0	0x3B-(0x5B)	*Idem*	*Idem*							
0x3A-(0x5A)	EICRB	ISC7 [1,0]		ISC6 [1,0]		ISC5 [1,0]		ISC4 [1,0]		(0x6A)	*Idem*	*Idem*							
0x39-(0x59)	EIMSK	INT[7..0]								0x1D-(0x3D)	*Idem*	*Idem*							
0x38-(0x58)	EIFR	INTF[7..0]								0x1C-(0x3C)	*Idem*	*Idem*							
0x37-(0x57)	TIMSK (see page 9) (see page 9)	OCIE2	TOIE2	ICIE1	OCIE1A	OCIE1B	TOIE1	OCIE0	TOIE0	(0x6E)	TIMSK0	-	-	-	-	-	-	OCIE0A	TOIE0
										(0x6F)	TIMSK1	-	-	ICIE1	-	OCIE1C	OCIE1B	OCIE1A	TOIE1
										(0x70)	TIMSK2	-	-	-	-	-	-	OCIE2A	TOIE2
0x36-(0x56)	TIFR (see page 9) (see page 9)	OCF2	TOV2	ICF1	OCF1A	OCF1B	TOV1	OCF0	TOV0	0x15-(0x35)	TIFR0	-	-	-	-	-	-	OCF0A	TOV0
										0x16-(0x36)	TIFR1	-	-	ICF1	-	OCF1C	OCF1B	OCF1A	TOV1
										0x17-(0x37)	TIFR2	-	-	-	-	-	-	OCF2A	TOV2

Table 13. I/O Registers (Continued)

ATmega128										AT90CAN128									
		Register Content										Register Content							
Add.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Add.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x35-(0x55)	MCUCR	SRE	SRW10	SE	SM1	SM0	SM2	IVSEL	IVCE	(0x74)	XMCRA	SRE	SRL[2..0]			SRW11	SRW10	SRW0 [1,0]	
										0x33-(0x53)	SMCR	-	-	-	-	SM[2..0]			SE
										0x35-(0x55)	MCUCR	JTD	-	-	PUD	-	-	IVSEL	IVCE
0x34-(0x54)	MCUCSR	JTD	-	-	JTRF	WDRF	BORF	EXTRF	PORF	0x35-(0x55)	MCUCR	JTD	-	-	PUD	-	-	IVSEL	IVCE
										0x34-(0x54)	MCUSR	-	-	-	JTRF	WDRF	BORF	EXTRF	PORF
0x33-(0x53)	TCCR0 (see page 9)	FOC0	WGM00	COM0 [1,0]		WGM01	CS0[2..0]			(0xB0)	TCCR2A	FOC2A	WGM20	COM2A [1,0]		WGM21	CS2[2..0]		
0x32-(0x52)	TCNT0 (see page 9)	T/C0 Counter Register								(0xB2)	TCNT2	T/C2 Counter Register							
0x31-(0x51)	OCR0 (see page 9)	T/C0 Output Compare Register								(0xB3)	OCR2A	T/C2 Output Compare A Register							
0x30-(0x50)	ASSR (see page 9)	-	-	-	-	AS0	TCN0UB	OCR0UB	TCR0UB	(0xB6)	*Idem*	-	-	-	EXCLK	AS2	TCN2UB	OCR2UB	TCR2UB
0x2F-(0x4F)	TCCR1A	COM1A [1,0]		COM1B [1,0]		COM1C [1,0]		WGM1 [1,0]		(0x80)	*Idem*	*Idem*							
0x2E-(0x4E)	TCCR1B	ICNC1	ICES1	-	WGM1 [3,2]		CS1[2..0]			(0x81)	*Idem*	*Idem*							
0x2D-(0x4D)	TCNT1H	T/C1 Counter Register High Byte								(0x85)	*Idem*	*Idem*							
0x2C-(0x4C)	TCNT1L	T/C1 Counter Register Low Byte								(0x84)	*Idem*	*Idem*							
0x2B-(0x4B)	OCR1AH	T/C1 Output Compare A Register High Byte								(0x89)	*Idem*	*Idem*							
0x2A-(0x4A)	OCR1AL	T/C1 Output Compare A Register Low Byte								(0x88)	*Idem*	*Idem*							
0x29-(0x49)	OCR1BH	T/C1 Output Compare B Register High Byte								(0x8B)	*Idem*	*Idem*							
0x28-(0x48)	OCR1BL	T/C1 Output Compare B Register Low Byte								(0x8A)	*Idem*	*Idem*							
0x27-(0x47)	ICR1H	T/C1 Input Capture Register High Byte								(0x87)	*Idem*	*Idem*							
0x26-(0x46)	ICR1L	T/C1 Input Capture Register Low Byte								(0x86)	*Idem*	*Idem*							
0x25-(0x45)	TCCR2 (see page 9)	FOC2	WGM20	COM2 [1,0]		WGM21	CS2[2..0]			0x24-(0x44)	TCCR0A	FOC0A	WGM00	COM0A [1,0]		WGM01	CS0[2..0]		
0x24-(0x44)	TCNT2 (see page 9)	T/C2 Counter Register								0x26-(0x46)	TCNT0	T/C0 Counter Register							
0x23-(0x43)	OCR2 (see page 9)	T/C2 Output Compare Register								0x27-(0x47)	OCR0A	T/C0 Output Compare A Register							

Table 13. I/O Registers (Continued)

ATmega128										AT90CAN128									
		Register Content										Register Content							
Add.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Add.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x22-(0x42)	OCDR	OCDR[7..0]								0x31-(0x51)	*Idem*	*Idem*							
		IDRD	OCDR[6..0]																
0x21-(0x41)	WDTCR	-	-	-	WDCE	WDE	WDP[2..0]			(0x60)	*Idem*	*Idem*							
0x20-(0x40)	SFIOR (see page 9) (see page 10)	TMS	-	-	ADHSM	ACME	PUD	PSR0	PSR321	0x23-(0x43)	GTCCR	TSM	-	-	-	-	-	PSR2	PSR310
										(0x7B)	ADCSRB	ADHSM	ACME	-	-	-	ADTS[2..0]		
										0x35-(0x55)	MCUCR	JTD	-	-	PUD	-	-	IVSEL	iVCE
0x1F-(0x3F)	EEARH	-				EEPROM Address Register High				0x22-(0x42)	*Idem*	*Idem*							
0x1E-(0x3E)	EEARL	EEPROM Address Register Low Byte								0x21-(0x41)	*Idem*	*Idem*							
0x1D-(0x3D)	EEDR	EEPROM I/O Data Register								0x20-(0x40)	*Idem*	*Idem*							
0x1C-(0x3C)	EECR	-	-	-	-	EERIE	EEMWE	EEWE	EERE	0x1F-(0x3F)	*Idem*	*Idem*							
0x1B-(0x3B)	PORTA	PORTA[7..0]								0x02-(0x22)	*Idem*	*Idem*							
0x1A-(0x3A)	DDRA	DDA[7..0]								0x01-(0x21)	*Idem*	*Idem*							
0x19-(0x39)	PINA	PINA[7..0]								0x00-(0x20)	*Idem*	*Idem*							
0x18-(0x38)	PORTB	PORTB[7..0]								0x05-(0x25)	*Idem*	*Idem*							
0x17-(0x37)	DDRB	DDB[7..0]								0x04-(0x24)	*Idem*	*Idem*							
0x16-(0x36)	PINB	PINB[7..0]								0x03-(0x23)	*Idem*	*Idem*							
0x15-(0x35)	PORTC	PORTC[7..0]								0x08-(0x28)	*Idem*	*Idem*							
0x14-(0x34)	DDRC	DDC[7..0]								0x07-(0x27)	*Idem*	*Idem*							
0x13-(0x33)	PINC	PINC[7..0]								0x06-(0x26)	*Idem*	*Idem*							
0x12-(0x32)	PORTD	PORTD[7..0]								0x0B-(0x2B)	*Idem*	*Idem*							
0x11-(0x31)	DDRD	DDD[7..0]								0x0A-(0x2A)	*Idem*	*Idem*							
0x10-(0x30)	PIND	PIND[7..0]								0x09-(0x29)	*Idem*	*Idem*							
0x0F-(0x2F)	SPDR	SPI I/O Data Register								0x2E-(0x4E)	*Idem*	*Idem*							
0x0E-(0x2E)	SPSR	SPIF	WCOL	-	-	-	-	-	SPI2X	0x2D-(0x4D)	*Idem*	*Idem*							
0x0D-(0x2D)	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	0x2C-(0x4C)	*Idem*	*Idem*							
0x0C-(0x2C)	UDR0	USART0 I/O Data Register								(0xC6)	*Idem*	*Idem*							
0x0B-(0x2B)	UCSR0A	RXC0	TXC0	UDRE0	FE0	DOR0	UPE0	U2X0	MPCM0	(0xC0)	*Idem*	*Idem*							
0x0A-(0x2A)	UCSR0B	RXCIE0	TXCIE0	UDRIE0	RXEN0	TCEN0	UCSZ02	RXB80	TXB80	(0xC1)	*Idem*	*Idem*							

Table 13. I/O Registers (Continued)

ATmega128										AT90CAN128									
		Register Content										Register Content							
Add.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Add.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x09-(0x29)	UBRR0L	USART0 Baud Rate Register Low Byte								(0xC4)	*Idem*	*Idem*							
0x08-(0x28)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS [1,0]		0x30-(0x50)	*Idem*	*Idem*							
0x07-(0x27)	ADMUX	REFS [1,0]		ADLAR	MUX[4..0]					(0x7C)	*Idem*	*Idem*							
0x06-(0x26)	ADCSRA (see page 10)	ADEN	ADSC	ADRF	ADIF	ADIE	ADPS[2..0]			(0x7A)	*Idem*	*Idem*	*Idem*	ADATE	*Idem*	*Idem*	*Idem*		
0x05-(0x25)	ADCH	ADC Data Register High Byte								(0x79)	*Idem*	*Idem*							
0x04-(0x24)	ADCL	ADC Data Register Low Byte								(0x78)	*Idem*	*Idem*							
0x03-(0x23)	PORTE	PORTE[7..0]								0x0E-(0x2E)	*Idem*	*Idem*							
0x02-(0x22)	DDRE	DDE[7..0]								0x0D-(0x2D)	*Idem*	*Idem*							
0x01-(0x21)	PINE	PINE[7..0]								0x0C-(0x2C)	*Idem*	*Idem*							
0x00-(0x20)	PINF	PINF[7..0]								0x0F-(0x2F)	*Idem*	*Idem*							

Note: Some AT90CAN128 I/O registers are not listed in the hereinabove table because there is no corresponding registers/peripherals in ATmega128 (i.e. CAN registers).

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