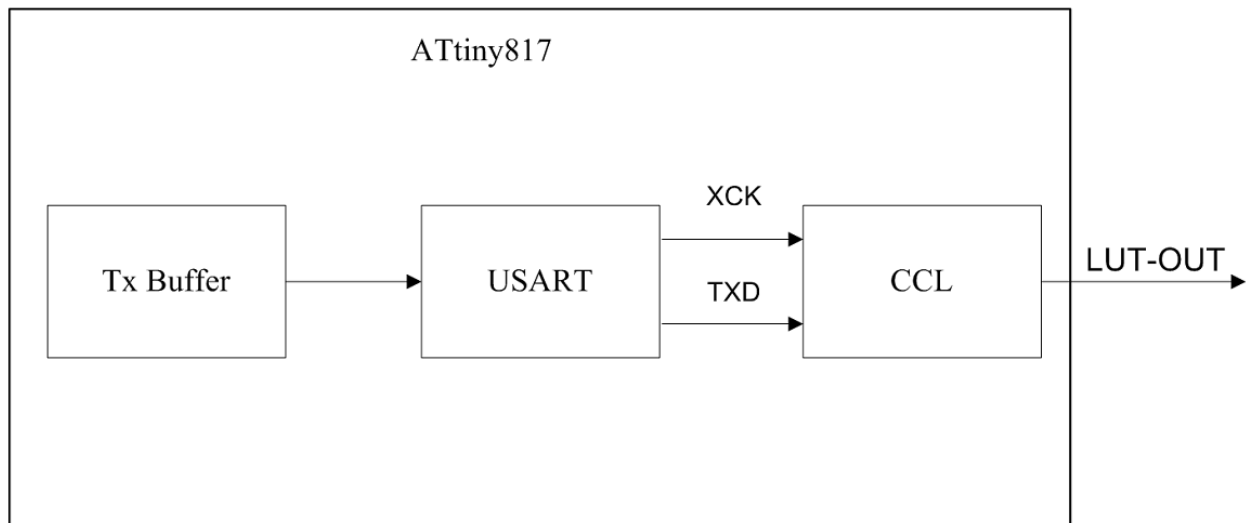

Manchester Encoder Using USART and CCL on ATtiny817

Introduction

Manchester coding is a coding technique widely used in digital telecommunication. It is a line coding in which the encoding of each data bit is either low then high, or high then low, of equal time. The encoded signal, therefore, is self-clocking, which means that the clock signal can be recovered from the encoded data.

This application note describes an approach to set up the Microchip ATtiny817 tinyAVR® 8-bit microcontroller to execute Manchester encoding with USART and Configurable Custom Logic (CCL) hardware modules.

Figure 1. Connection Diagram of Encoder



Another method of Manchester encoding is using Timer and GPIO modules. The Timer affords the time base of Manchester clock and the GPIO pin is used to generate Manchester code. In comparison, this application takes advantage of hardware resource USART and CCL, which reduce the CPU load remarkably.

Features

- Manchester Encoding
- Demonstrates Advantage of Combining USART and CCL (Configurable Custom Logic)

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1. Related Items

The following list contains links to the most relevant documents:

- <http://www.microchip.com/wwwproducts/en/attiny817>
- [Manchester code in Wikipedia](#)

2. Manchester Code

Manchester coding was first developed and published by G.E. Thomas in 1943. This was the first convention of Manchester coding and is known as the G.E. Thomas convention. This was followed by a convention used in low-speed Ethernet standards and is known as the IEEE® 802.3 convention.

2.1 G.E. Thomas Convention

The G. E. Thomas convention of Manchester encoding states that a bit value of “1” is a transition from “1” to “0” and a bit value of “0” is a transition from “0” to “1”.

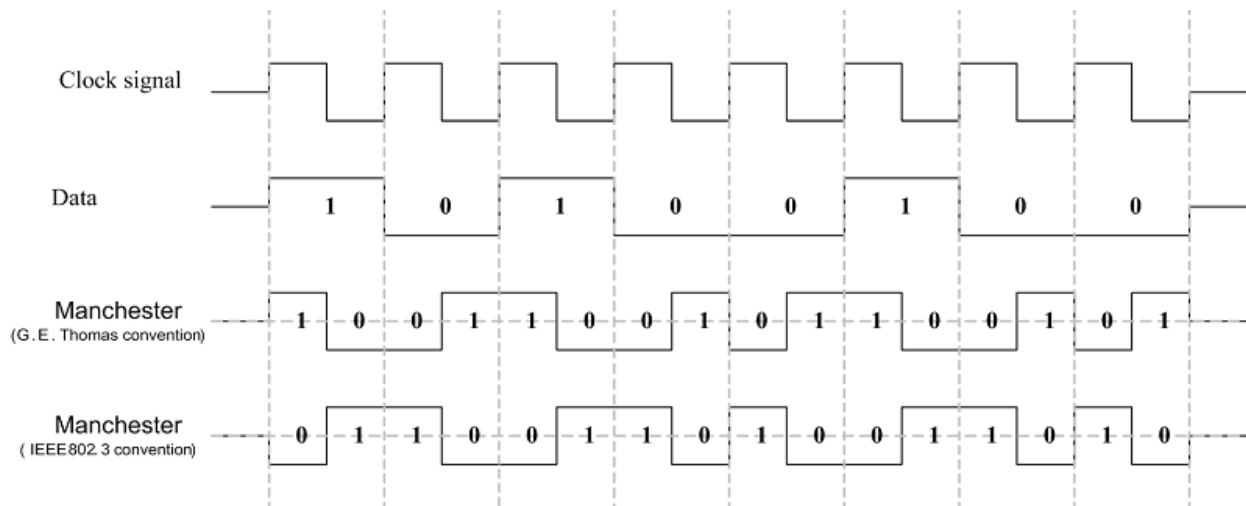
The encoding of the data can be done simply by using XNOR between the data and the clock signal.

2.2 IEEE 802.3 Convention

The IEEE 802.3 convention of Manchester encoding states that a bit value of “1” is a transition from “0” to “1” and a bit value of “0” is a transition from “1” to “0”.

The encoding of the data can be done using XOR between the data and the clock signal.

Figure 2-1. Signal Encoding Conventions



3. Manchester Encoding

For Manchester encoding, the USART needs to operate in SPI Master mode. SCK of USART is used as the Manchester clock signal. Transmit data from the USART_TXDATA register is used as Manchester data. To encode the data, the CCL linked with USART is used to execute XNOR logic for the G. E Thomas convention, as shown in [Figure 2-1](#). For the IEEE 802.3 convention, XOR logic should be implemented for clock and data. To keep aligned, the same XNOR logic in CCL is used, but the data executes NOT logic in advance. The output is connected to the CCL LUT-OUT pin.

3.1 USART Registers Configuration

1. Set Control Register C (USART_CTRLC).

Bit	7	6	5	4	3	2	1	0
	CMODE[1:0]		PMODE[1:0]		SBMODE	UDORD	UCPHA	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	

- **Bit 7:6 – CMODE[1:0]: USART Communication Mode**
Select Master SPI communication mode provided with a synchronous clock and data output.
- **Bit 5:4 – PMODE[1:0]: Parity Mode**
- **Bit 3 – SBMODE: Stop Bit Mode**
- **Bit 2 – UDORD: Data Order**
This bit selects either LSB or MSB of the data to be transmitted first. Default is used here.
- **Bit 1 – UCPHA: Clock Phase**
This bit determines if data is sampled on the trailing edge of XCK.

2. Set Baud Register (USART_BAUD).

Bit	15	14	13	12	11	10	9	8
	BAUD[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	BAUD[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

- **Bit 15:0 – BAUD[15:0]: USART Baud Rate**
For Master SPI mode, only ten MSBs are valid. The calculation equations are described in the data sheet.

3. Set Control Register A (USART_CTRLA).

Bit	7	6	5	4	3	2	1	0
	RXCIE	TXCIE	DREIE	RXSIE	LBME	ABEIE	RS485[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

- **Bit 7 – RXCIE: Receive Complete Interrupt Enable**
- **Bit 6 – TXCIE: Transmit Complete Interrupt Enable**

- **Bit 5 – DREIE: Data Register Empty Interrupt Enable**
Set this interrupt to enable for data sending.
 - **Bit 4 – RXSIE: Receiver Start Frame Interrupt Enable**
 - **Bit 3 – LBME: Loop-back Mode Enable**
 - **Bit 2 – ABEIE: Auto-baud Error Interrupt Enable**
 - **Bits 1:0 – RS485[1:0]: RS485 Mode**
4. Set Control Register B (USART_CTRLB).

Bit	7	6	5	4	3	2	1	0
	RXEN	TXEN		SFDEN	ODME	RXMODE[1:0]		MPCM
Access	R/W	R/W		R/W	R/W	R/W	R/W	R/W
Reset	0	0		0	0	0	0	0

- **Bit 7 – RXEN: Receiver Enable**
- **Bit 6 – TXEN: Transmitter Enable**
Set to enable USART transmitter.
- **Bit 4 – SFDEN: Start Frame Detection Enable**
- **Bit 3 – ODME: Open Drain Mode Enable**
- **Bits 2:1 – RXMODE[1:0]: Receiver Mode**
- **Bit 0 – MPCM: Multiprocessor Communication Mode**

3.2 CCL Registers Configuration

1. Set LUT Control Register B (CCL_LUTCTRLB).

Bit	7	6	5	4	3	2	1	0
	INSEL1[3:0]				INSEL0[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

- **Bits 7:4 – INSEL1[3:0]: LUT n Input 1 Source Selection**
Select USART TXD as the input source.
- **Bits 3:0 – INSEL0[3:0]: LUT n Input 0 Source Selection**
Select USART XCK as the input source.

2. Set TRUTH TABLE (CCL_TRUTH).

Bit	7	6	5	4	3	2	1	0
	TRUTH[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

- **Bits 7:0 – TRUTH[7:0]: Truth Table**
Set to 0x99 (0b10011001) as XNOR logic.

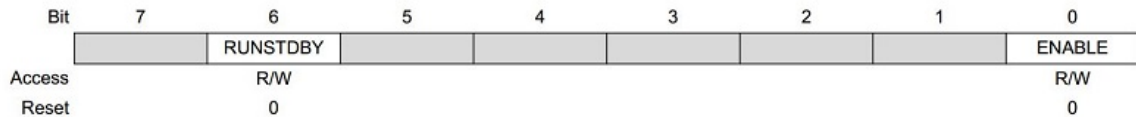
3. Set LUT Control Register A (CCL_LUTCTRLA).

Bit	7	6	5	4	3	2	1	0
	EDGEDET	CLKSRC	FILTSEL[1:0]		OUTEN			ENABLE
Access	R/W	R/W	R/W	R/W	R/W			R/W
Reset	0	0	0	0	0			0

- **Bit 7 – EDGEDET: Edge Detection**

- **Bit 6 – CLKSRC: Clock Source Selection**
- **Bits 5:4 – FILTSEL[1:0]: Filter Selection**
Enable filter as XCK and TXD may not synchronize precisely.
- **Bit 3 – OUTEN: Output Enable**
Set to enable output.
- **Bit 0 – ENABLE: LUT Enable**
Set to enable LUT.

4. Set Control Register A (CCL_CTRLA).



- **Bit 6 – RUNSTDBY: Run in Standby**
- **Bit 0 – ENABLE: Enable**
Set to enable CCL peripheral.

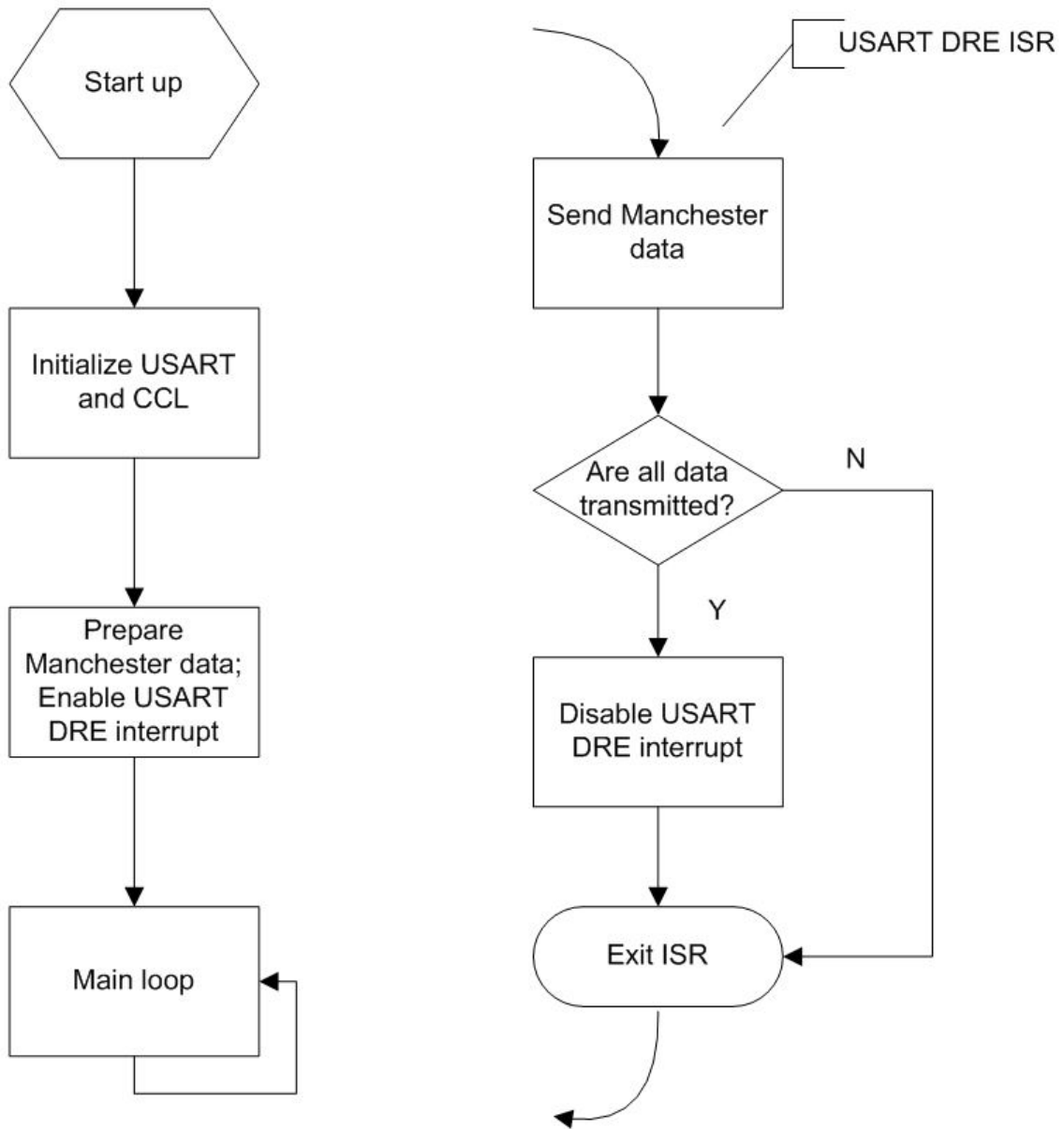
3.3 Other Configuration

1. Implement USART DRE Interrupt Service Routine.
Manchester data is entered to the USART TXDATA register here.
2. Set CCL pin.
Set the CCL LUT-OUT pin as an output in the I/O PORT register.

3.4 Encoding Flowchart

First, the USART and CCL should be initialized to encoding state. Then prepare Manchester data and enable USART DRE interrupt. Manchester code is sent inside the Interrupt Service Routine. The flowchart is shown in the figure below.

Figure 3-1. Flowchart



4. Get Source Code from Atmel | START

The example code is available through Atmel | START, which is a web-based tool that enables configuration of application code through a Graphical User Interface (GUI). The code can be downloaded for both Atmel Studio 7.0 and IAR Embedded Workbench® via the direct example code-link(s) below or the *BROWSE EXAMPLES* button on the Atmel | START front page.

Atmel | START web page: <http://microchip.com/start>

Example Code

AVR42817 Manchester Encoder

- http://start.atmel.com/#application/Atmel:avr42817_manchester_encoder:0.0.1::Application:AVR42817_Manchester_encoder

Press *User guide* in Atmel | START for details and information about example projects. The *User guide* button can be found in the example browser, and by clicking the project name in the dashboard view within the Atmel | START project configurator.

Atmel Studio

Download the code as an .atzip file for Atmel Studio from the example browser in Atmel | START, by clicking *DOWNLOAD SELECTED EXAMPLE*. To download the file from within Atmel | START, click *EXPORT PROJECT* followed by *DOWNLOAD PACK*.

Double-click the downloaded .atzip file and the project will be imported to Atmel Studio 7.0.

IAR Embedded Workbench

For information on how to import the project in IAR Embedded Workbench, open the Atmel | START user guide, select *Using Atmel Start Output in External Tools*, and *IAR Embedded Workbench*. A link to the Atmel | START user guide can be found by clicking *About* from the Atmel | START front page or *Help And Support* within the project configurator, both located in the upper right corner of the page.

5. Manchester Diagram

The following diagrams are the output waveform snapshots of an example project where the yellow signal is USART XCK, the purple signal is USART TXDATA, and the blue is CCL OUT. The demonstrated Manchester data is "0x00, 0x01, 0x02".

Figure 5-1. G. E. Thomas Convention

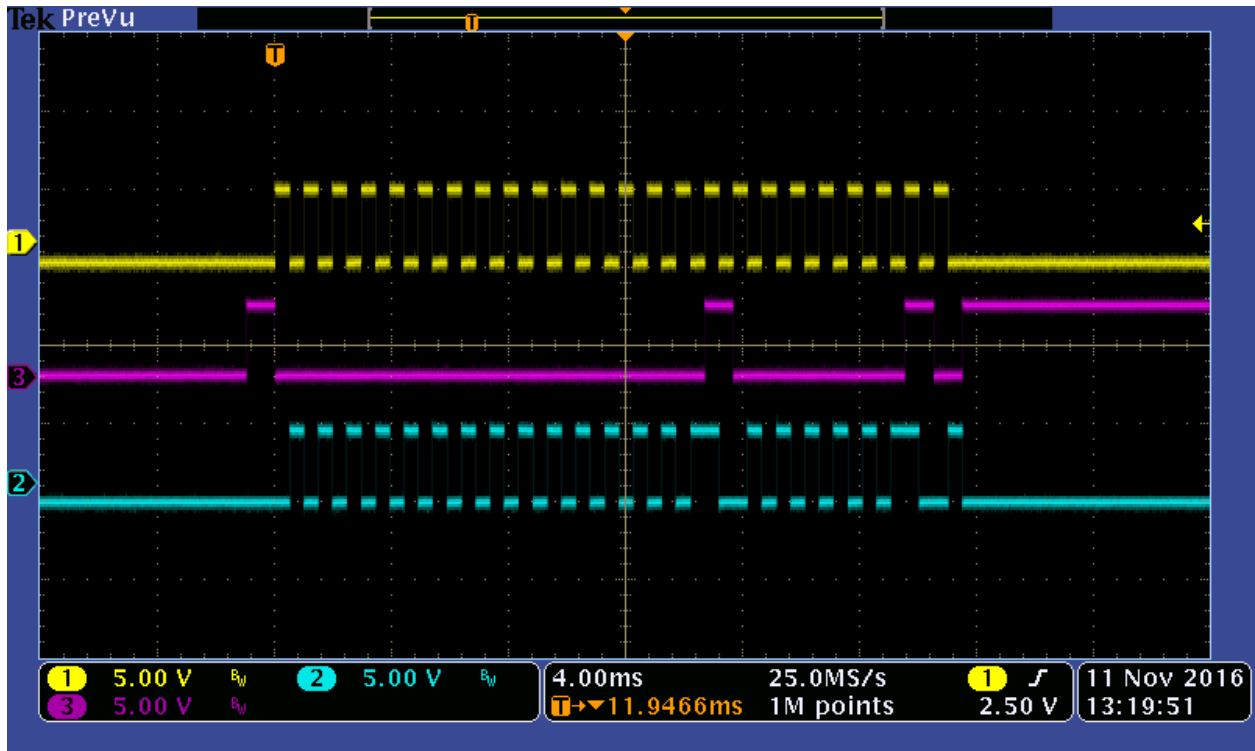
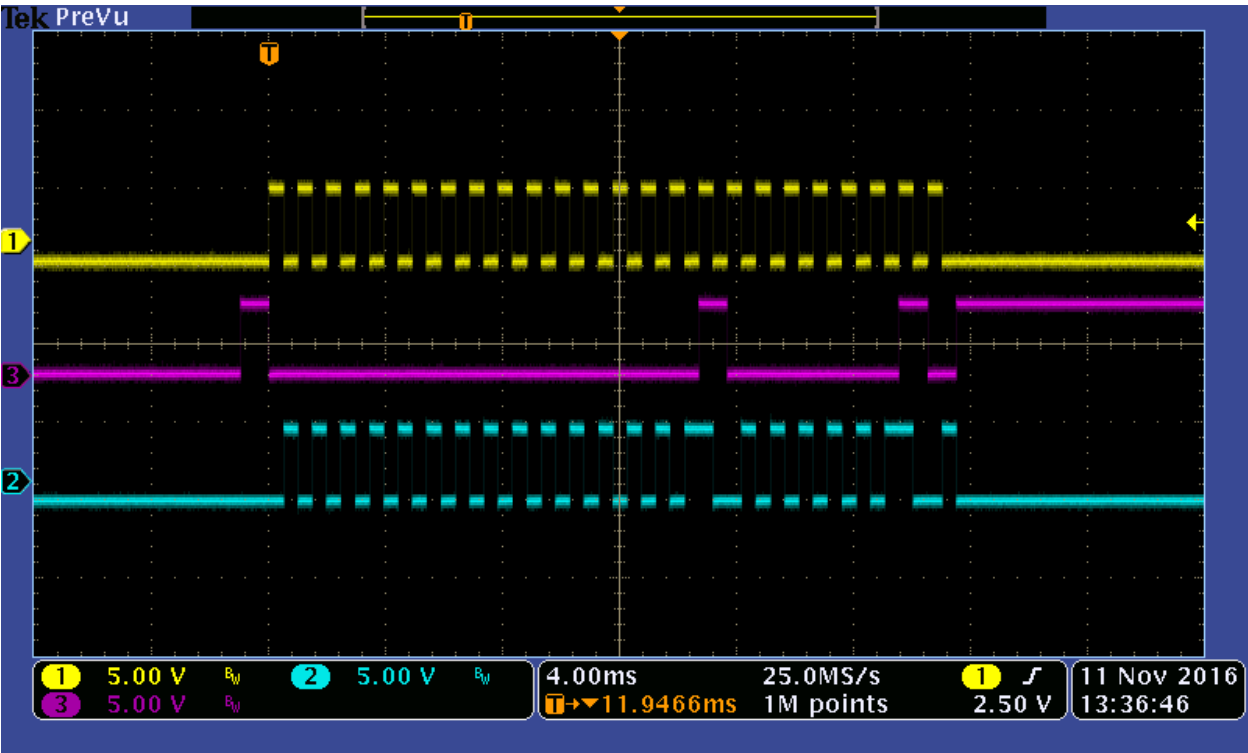


Figure 5-2. IEEE 802.3 Convention



6. Revision History

Doc. Rev.	Date	Comments
B	02/2018	Updated START example link.
A	04/2017	Initial document release.

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