

Digitally Controlled Oscillator with Clock Switching on 8-Bit PIC[®] Microcontrollers

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INTRODUCTION

The oscillator module handles the clock source selection for 8-bit PIC[®] microcontrollers. Within this module is an internal high-frequency oscillator (HFINTOSC), an external high-frequency oscillator (EXTOSC), a Secondary Oscillator block (SOSC), a PLL and other low-frequency oscillators. Figure 1 shows how the oscillators are connected in the oscillator module.

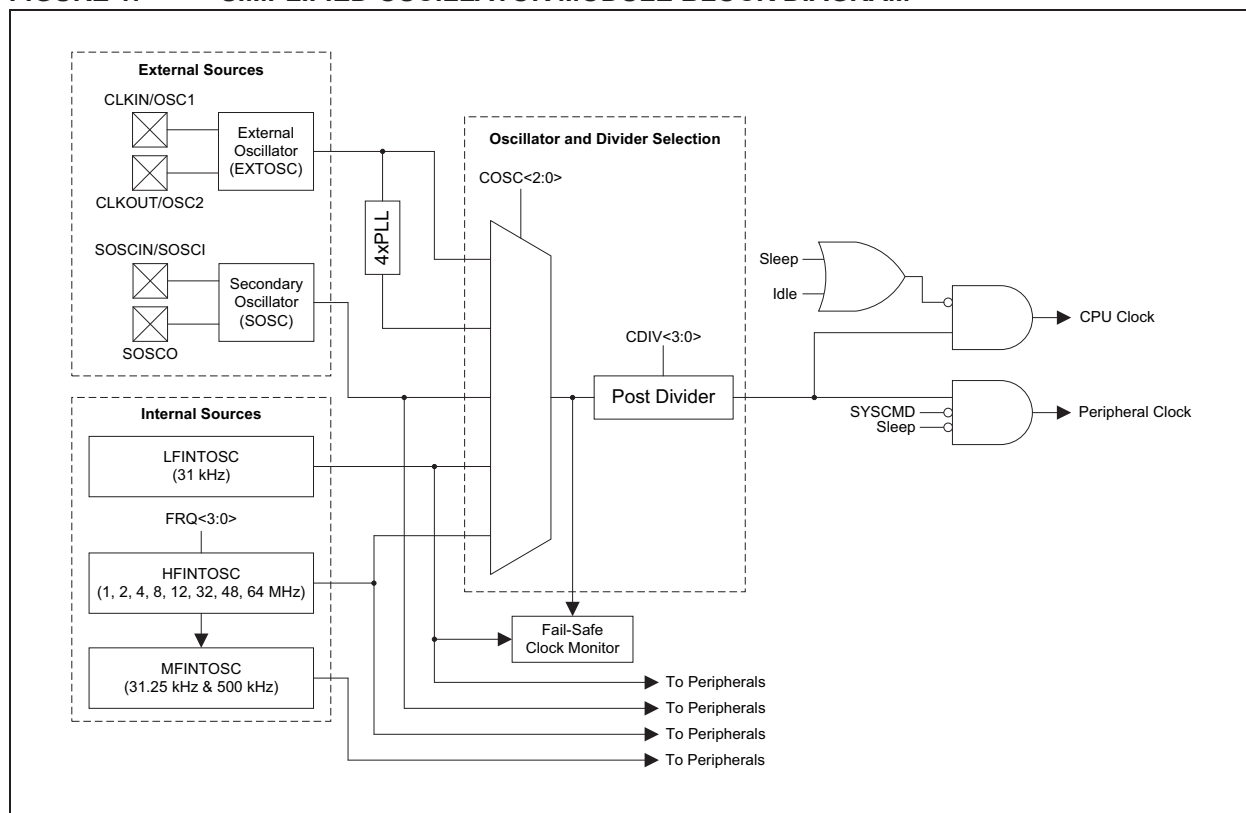
This Technical Brief covers the internal oscillator's features, functions and operation. This document discusses the functionality in the oscillator module; how it operates with clock switching and the effects of the 8-bit PIC MCU's power-saving features.

OSCILLATOR MODULE

The oscillator module provides a diversity of clock sources and features for the CPU, and various peripherals. Though the system clock is initially configured in the Configuration Words, the user may adjust the clock frequency or change the clock source in the user code. Figure 1 shows the module's block diagram. The diagram includes the clock sources, clock source and postscaler selection, a 4xPLL circuit, Fail-Safe Clock Monitor (FSCM) and Peripheral Module Disable (PMD) support. To learn more on the module, refer to the "Oscillator Module Technical Brief" (TB3148).

Note: The availability of the Peripheral Module Disable (PMD) for the System Clock (SYSCMD) is device-specific. Refer to the device data sheet to check if this feature is present in the device.

FIGURE 1: SIMPLIFIED OSCILLATOR MODULE BLOCK DIAGRAM



High-Frequency Internal Oscillator

The HFINTOSC is the module's most commonly used internal oscillator with a frequency range up to 64 MHz. The HFINTOSC operating frequency is determined by the combination of the OSCFRQ and N/CDIV settings, with a default value determined by RSTOSC. Figure 2 shows the available oscillator settings in the Configuration Words.

This oscillator is also used as the reference for the constant frequency outputs of the MFINTOSC peripheral clocks. The MFINTOSC frequencies are digital divisors of the HFINTOSC set to provide both 31.25 and 500 kHz.

FIGURE 2: INITIALIZING HFINTOSC AS THE SYSTEM CLOCK SOURCE THROUGH RSTOSC AND FEXTOSC IN MPLAB® X IDE

Address	Name	Value	Field	Option	Category	Setting
300000	CONFIG1L EC		RSTOSC	HFINTOSC...	Reset Oscillator Selection	HFINTOSC with HFFRQ = 4 MHz and CDIV = 4:1
				HFINTOSC 64MHz		HFINTOSC with HFFRQ = 64 MHz and CDIV = 1:1
				EXTOSC 4PLL		EXTOSC with 4x PLL, with EXTOSC operating per FEXTOSC bits
				RESERVED		Reserved
				SOSC		Secondary Oscillator
				LFINTOSC		Low-Frequency Oscillator
				HFINTOSC 1MHz		HFINTOSC with HFFRQ = 4 MHz and CDIV = 4:1
				EXTOSC		EXTOSC operating per FEXTOSC bits (device manufacturing default)
			FEXTOSC	OFF	External Oscillator Selection	Oscillator not enabled
				LP		LP (crystal oscillator) optimized for 32.768 kHz; PFM set to low power
				XT		XT (crystal oscillator) above 100 kHz, below 8 MHz; PFM set to medium power
				HS		HS (crystal oscillator) above 8 MHz; PFM set to high power
				RESERVED		Reserved (DO NOT USE)
				OFF		Oscillator not enabled
				ECL		EC (external clock) below 100 kHz; PFM set to low power
				ECM		EC (external clock) for 500 kHz to 8 MHz; PFM set to medium power
				ECH		EC (external clock) above 8 MHz; PFM set to high power

Auto-Enable

Regardless of the system clock source (external or internal), the HFINTOSC is enabled when a peripheral uses the MFINTOSC as a clock source. Since the oscillator frequency is a factor in the device power operation, it takes into account the OSCFRQ setting of HFINTOSC. For lower power consumption with MFINTOSC, the OSCFRQ must have the least value set.

Frequency Selection

At Reset, the HFINTOSC operating frequency is determined by RSTOSC. In the user code, the frequency can be varied in the OSCFRQ register. The operating frequency can also be postscaled further through clock switching. Table 1 provides a list of selectable frequencies under OSCFRQ. At OSCFRQ frequencies above 4 MHz, power consumption is higher and start-up time is longer. These effects are caused by the internal PLL blocks used to achieve the higher frequencies.

TABLE 1: SELECTABLE HFINTOSC FREQUENCIES (kHz)

OSCFRQ <3:0>	NDIV/CDIV <3:0>									
	1 <0>	2 <1>	4 <2>	8 <3>	16 <4>	32 <5>	64 <6>	128 <7>	256 <8>	512 <9>
1 MHz <0>	1000	500	250	125	62.5	31.25	15.63	7.81	3.91	1.95
2 MHz <1>	2000	1000	500	250	125	62.5	31.25	15.63	7.81	3.91
4 MHz <2>	4000	2000	1000 ⁽¹⁾	500	250	125	62.5	31.25	15.63	7.81
8 MHz <3>	8000	4000	2000	1000	500	250	125	62.5	31.25	15.63
12 MHz <4>	12000	6000	3000	1500	750	375	187.5	93.75	46.88	23.44
16 MHz <5>	16000	8000	4000	2000	1000	500	250	125	62.5	31.25
32 MHz <6>	32000 ⁽¹⁾	16000	8000	4000	2000	1000	500	250	125	62.5
48 MHz <7> ⁽²⁾	48000	24000	12000	6000	3000	1500	750	375	187.5	93.75
64 MHz <8> ⁽²⁾	64000 ⁽¹⁾	32000	16000	8000	4000	2000	1000	500	250	125

Note 1: These are default oscillator settings determined by the RSTOCS bits.

2: These options are for PIC18 only and are not available in PIC16.

Frequency Tuning

HFINTOSC frequency can be fine-tuned in the user code. This is done by writing to the OSTUNE register in 6-bit two's complement (Sign bit + 5 bits). With an OSTUNE value of zero, the oscillator is tuned to the center frequency. Once OSTUNE is modified, the frequency begins to shift without affecting code execution. However, there is no indication whether the shift has occurred. The frequency can be shifted up to 3.2% of the calibrated value, in 64 steps, as configured in the OSTUNE register.

Clock Switching

The clock switching feature of the oscillator module allows the user to change both the system clock source and frequency divider by writing to the New Oscillator Source (NOSC) and New Divider Selection (NDIV) request bits of the Oscillator Control register.

Writing to the NOSC bits initiates a switch between clock sources. Between internal and external clock sources, switching adds a certain delay before the next code execution. The CPU will confirm if the new oscillator source is available and waits for the oscillator to stabilize before it is ready for use.

The operating frequency of HFINTOSC and the other sources can be postscaled further with a write to the NDIV bits. Table 1 shows more options of configurable frequencies, through combinations of the OSCFRQ

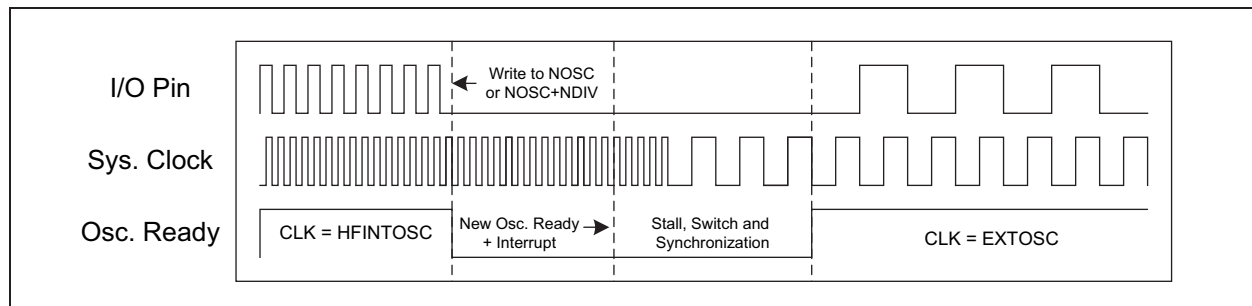
and N/CDIV bits. For a postscaler-only switch, the clock source is immediately ready, hence the delay is negligible.

Examples of switching sources and postscalers are shown in Figure 3 and Figure 4, respectively. The figures show the behavior of toggling an I/O pin before and after a clock switch. Sample codes for these figures are shown in Example 1 and Example 2. Having NOSC and NDIV combined in the same register avoids having two switching processes. With a single write to the control register, there is less risk to over-clocking and underclocking in the intermediate state. To learn more about the switching process, refer to TB3148.

Fail-Safe Clock Monitor

In cases where the external oscillator fails, this oscillator module feature selects the HFINTOSC in the COSC bits to ensure that the device will continue to operate. The device will operate with the frequency set in OSCFRQ and retain the postscaler setting in N/CDIV. An Oscillator Fail Interrupt (OSCIF) is provided to give the user an option to resolve the external clock failure while the system runs on the HFINTOSC. The condition is cleared either upon Reset, after Sleep or a successful switch through NOSC and NDIV.

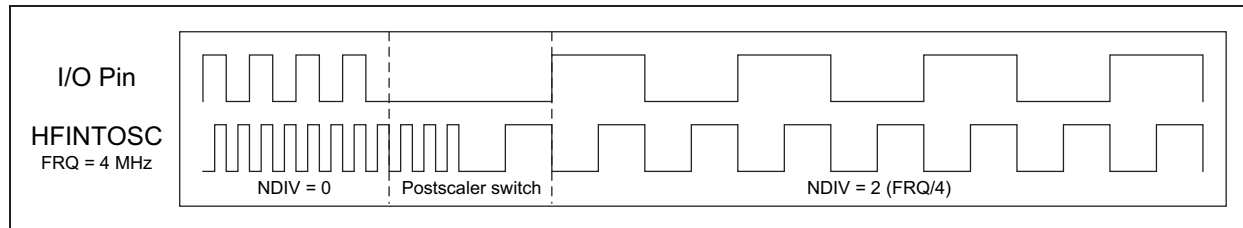
FIGURE 3: INTERNAL-EXTERNAL CLOCK SOURCE SWITCHING



EXAMPLE 1: INTERNAL-EXTERNAL CLOCK SOURCE SWITCHING SAMPLE CODE

```
// Switch from Internal to External Osc. (similar frequencies with a postscaler of 4)
// NOSC = 7; NDIV = 2;
OSCCON1 = 0x72;
// Wait here until the new osc. settings are ready
// to ensure operation with the new settings.
while(!OSCCON3bits.ORDY);
// Add your program code below
```

FIGURE 4: HFINTOSC POSTSCALER SWITCHING



EXAMPLE 2: HFINTOSC POSTSCALER SWITCHING SAMPLE CODE

```
// Switch HFINTOSC freq. from a post-scaler of 1 to 4
OSCCON1bits.NDIV = 0x02;
// Wait here (optional since the same osc. source is used)
while(!OSCCON3bits.ORDY);
// Add your program code below
```

POWER SAVING FEATURES

Generally, all internal oscillators, including HFINTOSC, are unaffected when the device enters Doze, Idle or Sleep mode. These modes only control or disable the configured system clock. Peripherals which directly use the internal oscillators still continue to operate.

For oscillator modules with PMD support, the PMD feature disables the use of the clock source for any peripheral. Similar to the previous modes, this does not have any effect on the internal oscillators and on the operation of the peripherals they serve.

For a more detailed discussion about these power-saving features, refer to *“Doze, Idle and PMD Features of 8-Bit PIC® Microcontrollers” (TB3144)*.

CONCLUSION

The digitally controlled oscillator of 8-bit PIC microcontrollers offers a wide range of selectable frequencies for the system and peripheral clock sources. The oscillator module provides an easy and smooth process for switching operating frequencies. Power-saving features have no effect on the internal oscillator, which ensures normal operation for peripherals alongside lower power consumption.

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