Complex Programmable Logic Device

ATF15xx Power-On Reset Hysteresis Feature

APPLICATION NOTE

Abstract

For some applications, a larger power reset hysteresis is required to prevent an Atmel® ATF15xx Complex Programmable Logic Device (CPLD) from resetting its registers due to supply voltage dips or glitches. For other applications, it might be more desirable to reset the registers in an ATF15xx CPLD when the supply voltage dips or glitches. To be compatible with both of these application types, the Power-On (or power-up) Reset (POR) hysteresis of the ATF15xx CPLD can be programmed to ***Large*** or ***Small*** by the user. This application note provides the details of this programmable feature.

Features

- Small vs. Large POR Hysteresis
- Recommended Settings for 5.0V and 3.3V ATF15xx CPLDs
- Design Software Option Settings

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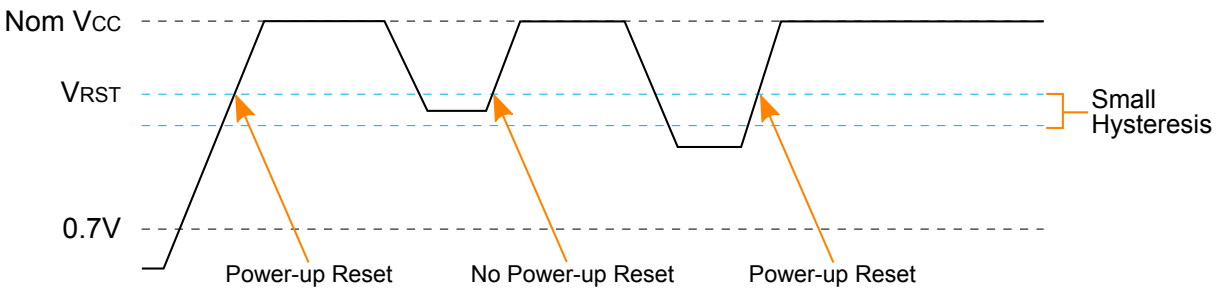
1. Overview

The ATF15xx CPLDs are designed with a power-up reset function to reset all registers (D/T flip-flops or latches) when V_{CC} rises slightly above the power-up reset voltage level (V_{RST}). When V_{CC} falls below the power-down voltage level and then subsequently rises above V_{RST}, the registers return to the reset state. The hysteresis between the power-up reset voltage level and power-down voltage level is controlled by the POR Hysteresis programmable option and can be set to ***Small*** or ***Large***. This programmable feature gives users the flexibility to choose the power-up reset hysteresis level that is most suitable for the intended application.

1.1. Small POR Hysteresis

When the POR Hysteresis option is set to ***Small***, the power-down voltage level is just slightly below V_{RST}. Therefore, whenever V_{CC} drops slightly below V_{RST}, the ATF15xx registers reset. This behavior is depicted in the below figure.

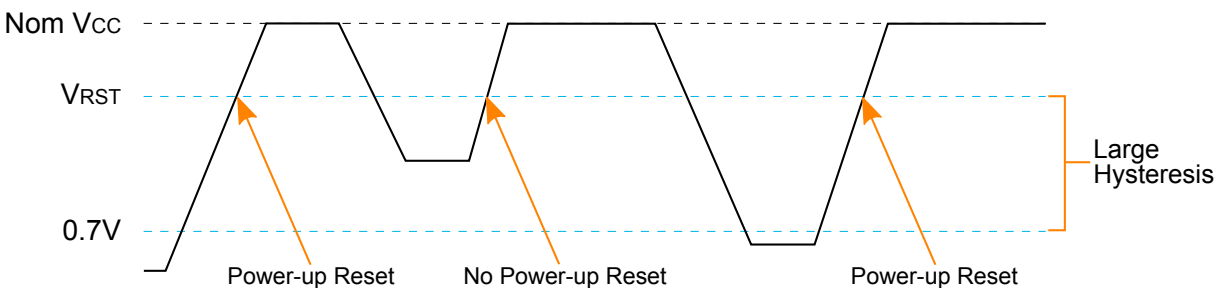
Figure 1-1 Reset Behaviors with POR Hysteresis Set to Small



1.2. Large POR Hysteresis

When the POR Hysteresis option is set to ***Large***, the power-down voltage level is approximately 0.7V. Therefore, the ATF15xx registers reset only when V_{CC} drops below 0.7V and then subsequently rises above V_{RST}. This behavior is depicted in the below figure. When the POR Hysteresis option is set to ***Large***, the ATF15xx I_{CC} is reduced by several hundred µA. This is especially significant for the ATF15xxASL and ATF15xxASVL low-power devices in order to minimize power consumption.

Figure 1-2 Reset Behaviors with POR Hysteresis Set to Large



1.3. Power-up Requirements

Due to the asynchronous nature of reset and uncertainty of how V_{CC} actually rises in the system, the following power-up conditions are required:

1. The V_{CC} rise must be monotonic.
2. After reset occurs, all input and feedback setup times must be met before driving the clock pin high.
3. The clock must remain stable during device power-up.
4. When the POR Hysteresis option is set to Large, the following condition is added to ensure that the registers are properly re-initialized when V_{CC} rises again: If V_{CC} falls to around 2.0V, it must shut off completely before the ATF15xx can be powered up again.

1.4. Recommendation

For the ATF15xxAS/ASL 5.0V CPLDs, V_{RST} is typically midway between the specified minimum power supply voltage and ground. Therefore, the margin for V_{CC} dips or noise is generally sufficient even when POR Hysteresis is set to ***Small***. However, for the ATF15xxASV/ASVL 3.3V CPLDs, V_{RST} is typically just below the specified minimum power supply voltage and the available margin is reduced. In applications where the supply voltage falls close to the specified minimum power supply voltage, Atmel recommends increasing the margin for falling V_{CC} by setting the POR Hysteresis option to ***Large***. With the Large POR Hysteresis option selected, the power-down voltage level drops to a much lower level to prevent the registers from resetting due to small V_{CC} dips, noise or glitches.

2. Design Option Setting

The POR Hysteresis option setting can be specified in the design source file or in the design development software tool graphical user interface.

2.1. ProChip Designer

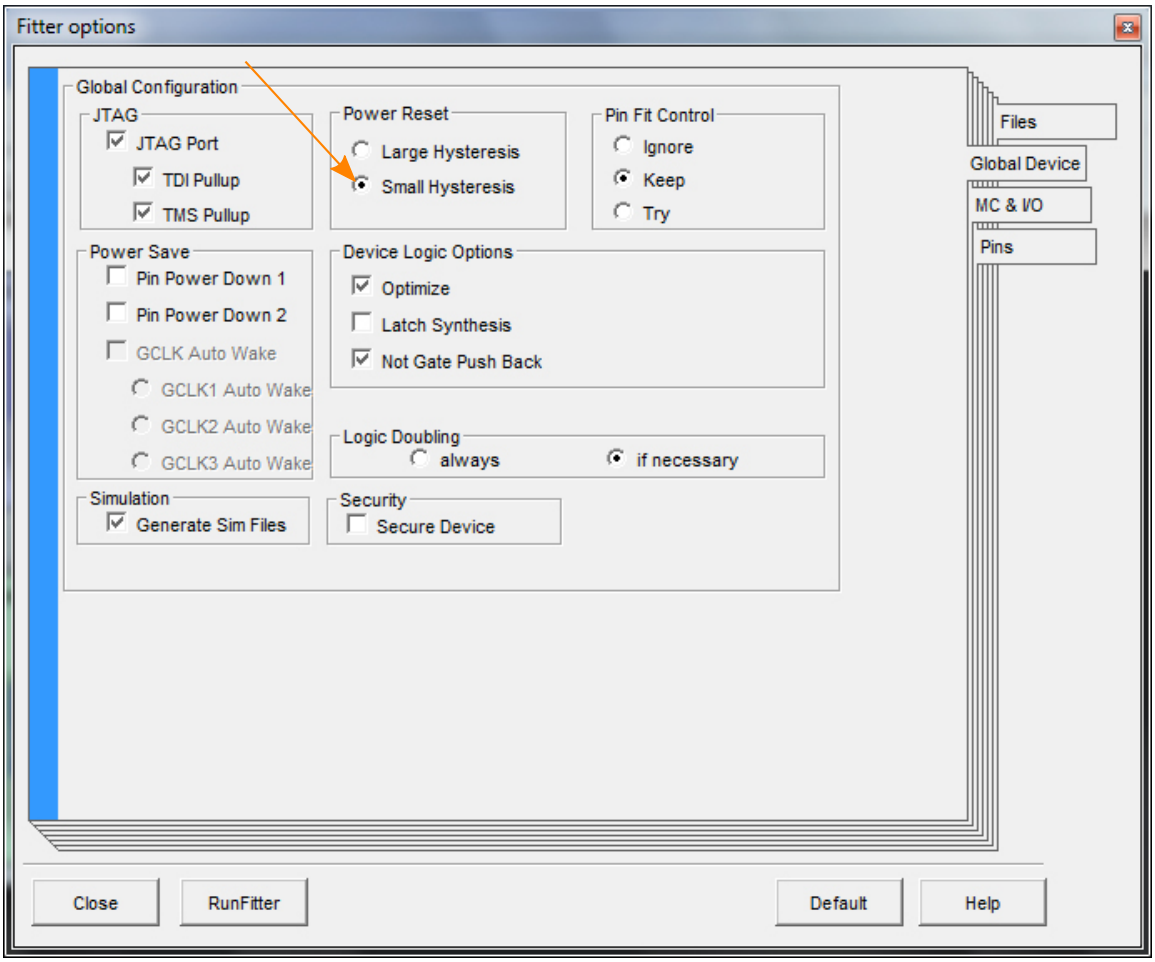
To specify the POR Hysteresis option setting in the Atmel ProChip Designer:

1. Open the ***Fitter options*** window by clicking on the ***Atmel Fitter*** button under the ***Device Fitter*** process.
2. Select the ***Global Device*** tab.
3. Check either the ***Large Hysteresis*** or ***Small Hysteresis*** radio button under ***Power Reset*** as shown in the below figure.

The ProChip Designer default setting is ***Small*** for ATF15xxAS/ASL 5.0V device types and ***Large*** for ATF15xxASV/ASVL 3.3V device types.

The ProChip Designer can be downloaded from: www.atmel.com/tools/PROCHIPDESIGNERV5_0.aspx

Figure 2-1 ProChip Designer POR Hysteresis Option Setting



2.2. WinCUPL

To set the POR Hysteresis option to ***Small*** in Atmel WinCUPL, the following property statement in the CUPL design file must be included.

```
PROPERTY ATMEL {POWER_RESET = OFF};
```

To set the POR Hysteresis option to ***Large*** in WinCUPL, the following property statement in the CUPL design file must be included.

```
PROPERTY ATMEL {POWER_RESET = ON};
```

The default setting in WinCUPL is ***Small*** for all ATF15xx device types.

WinCUPL can be downloaded from: www.atmel.com/tools/WINCUPL.aspx

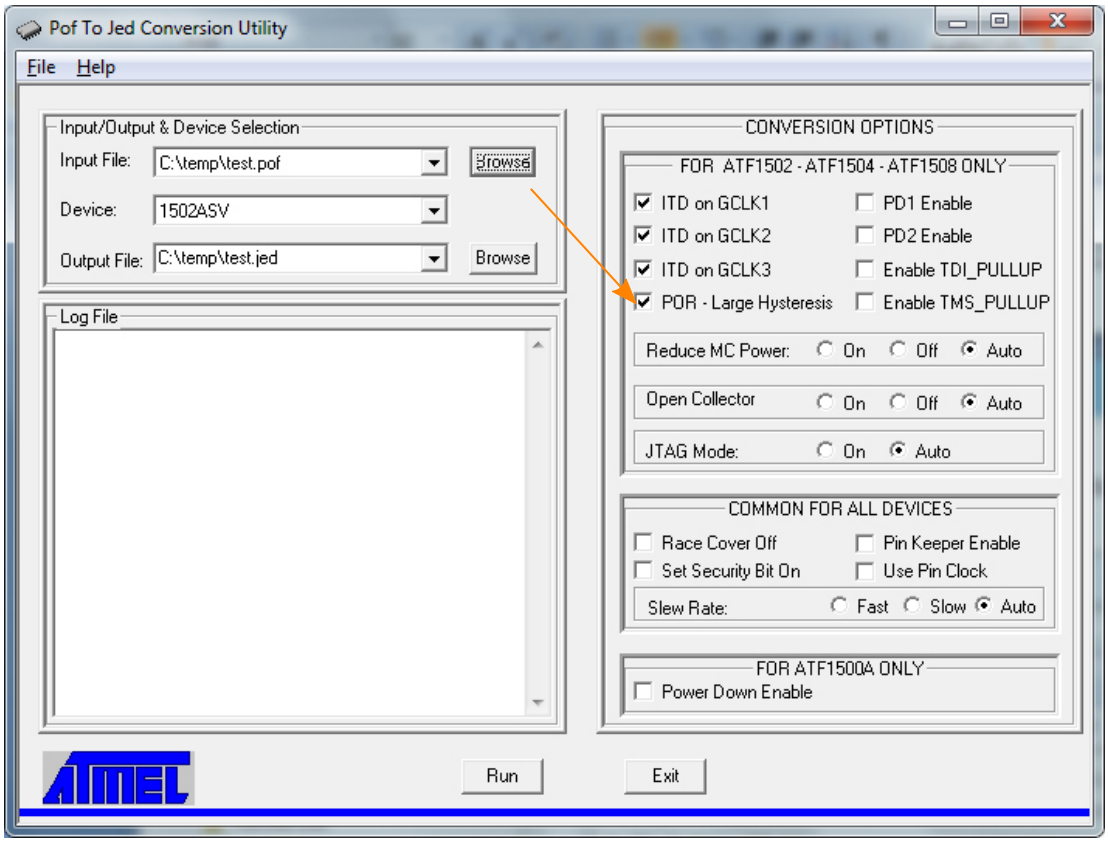
2.3. POF2JED

To set the POR Hysteresis option to ***Large*** in Atmel POF2JED GUI, check the box ***POR – Large Hysteresis*** as shown in the below figure. Otherwise, uncheck this box to set the POR Hysteresis option to ***Small***.

The POF2JED default setting in is ***Small*** for ATF15xxAS/ASL 5.0V device types and ***Large*** for ATF15xxASV/ASVL 3.3V device types.

The POF2JED can be downloaded from: www.atmel.com/tools/POF2JED.aspx

Figure 2-2 POF2JED POR Hysteresis Option Setting



3. Revision History

Doc Rev.	Date	Comments
A	10/2015	Initial document release.

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