

PIC16F527 Silicon Errata and Data Sheet Clarification

The PIC16F527 device that you have received conforms functionally to the current Device Data Sheet (DS40001652C), except for the anomalies described in this document.

The silicon issues and affected revisions are summarized in [Table 1](#).

The errata described in this document will be addressed in future revisions of the PIC16F527 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of [Table 1](#) apply to the current silicon revision (**A2**).

Data Sheet clarifications and corrections start on [page 3](#), following the discussion of silicon issues.

TABLE 1: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions ⁽¹⁾	
				A1	A2
Sleep Mode	Wake-up	1.	Device Reset Timer affects wake-up operations.	X	

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

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Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the Affected Silicon Revisions tables apply to the current silicon revision (**A2**).

1. Module: Sleep Mode

Enabling the Device Reset Timer (DRT), along with certain other conditions, will prevent the device from “Wake-up Inline” and “Wake-up and Vector”. This includes the wake-up by PORTx on Pin Change Interrupt, Comparator 1 and 2 change Interrupt and Watchdog Wake-up Inline. See [Table 2](#) below for affected wake-up conditions. “Wake-up Reset” and “Watchdog Wake-up Reset” do not apply to this errata.

TABLE 2: AFFECTED WAKE-UP CONDITIONS

	In Sleep	GIE Bit	WUR Bit
Wake-up and Vector	Yes	1	0
Wake-up Inline	Yes	0	0
Watchdog Wake-up Inline	Yes	X	0

Work around

Method 1: If the DRT is not needed, disable DRT by clearing the DRTEN bit in the Configuration Word register.

Method 2: If the DRT is needed, the following selections need to be made prior to executing a SLEEP instruction.

- The ‘PSA: Prescaler Assignment Bit’ in the OPTION register needs to be set to ‘1’ (Prescaler assigned to the Watchdog Timer (WDT))
- The ‘PS<2:0>: Prescaler Rate Select bits’ in the OPTION register need to be set to a value greater than ‘0’.

When using “Watchdog Wake-up Inline”, the requirement that the PS<2:0> (Prescaler Rate Select bits) must be set to a value greater than ‘0’, does not apply. Although, when using a value of ‘0’ the device will wake-up from Sleep with a prescaler rate of 1:2.

When using “Wake-up and Vector” or “Wake-up Inline”, the state of the WDT is irrelevant and it can be either enabled or disabled in the Configuration Word register.

Affected Silicon Revisions

A1	A2						
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001652C):

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: OPTION Register

Register 4-2 (OPTION REGISTER): Note 2 for the Option register should be read as follows:

Note 2: The $\overline{\text{RAWU}}$ bit of the OPTION register must be **cleared** to enable the RAIF function in the INTCON0 register.

2. Module: INTCON0 Register

Register 8-2 (INTCON0 REGISTER): Note 1 and 2 for the INTCON0 register should be read as follows:

Note 1: This bit only functions when the $\overline{\text{C1WU}}$ or $\overline{\text{C2WU}}$ bits are **cleared** (see [Register 10-1](#) and [Register 10-2](#)).

Note 2: The $\overline{\text{RAWU}}$ bit of the OPTION register must be **cleared** to enable this function (see [Register 4-2](#)).

3. Module: CM1CON0 Register

Register 10-1 (CM1CON0: Comparator C1 Control Register): Note 3 for the CM1CON0 register should be read as follows:

Note 3: The $\overline{\text{C1WU}}$ bit must be **cleared** to enable the CWIF function. See the INTCON0 register (see [Register 8-2](#)) for more information.

4. Module: CM2CON0 Register

Register 10-2 (CM2CON0: Comparator C2 Control Register): Note 3 for the CM2CON0 register should be read as follows:

Note 3: The $\overline{\text{C2WU}}$ bit must be **cleared** to enable the CWIF function. See the INTCON0 register (see [Register 8-2](#)) for more information.

5. Module: Interrupts

In the Interrupts Operation section 8.11.1, the paragraph about the comparator and interrupt-on-change flags should be read as follows:

The comparator and interrupt-on-change flags must be enabled for use. One or both of the comparator outputs can be enabled to affect the interrupt flag by **clearing** the $\overline{\text{C1WU}}$ bit in the CM1CON0 register and the $\overline{\text{C2WU}}$ bit in the CM2CON0 register. The interrupt-on-change flag is enabled by **clearing** the $\overline{\text{RAWU}}$ bit in the OPTION register.

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APPENDIX A: DOCUMENT REVISION HISTORY

Rev. A Document (8/2014)

Initial release of this document.

Rev. B Document (2/2015)

Added silicon revision A2.

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