AT93C86A

Three-Wire Automotive Temperature Serial EEPROM 16-Kbit (2,048 x 8 or 1,024 x 16)

Features

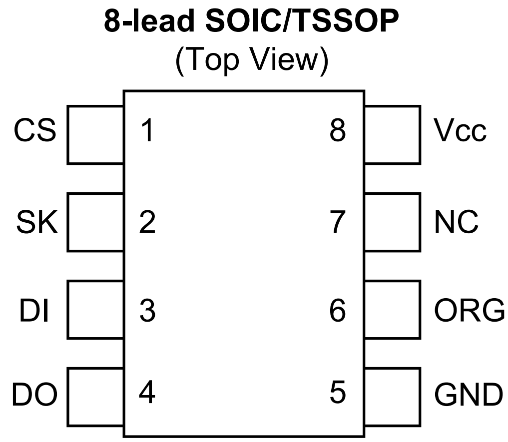
- Medium-Voltage and Standard-Voltage Operations:
  - V_{CC} = 2.7V to 5.5V
- User-Selectable Internally Organized as 2,048 x 8 (16K) or 1,024 x 16 (16K)
- Automotive Temperature Range: -40°C to +125°C
- Three-Wire Serial Interface
- Sequential Read Operation
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- 2 MHz Clock Rate (5V)
- Self-Timed Write Cycle within 10 ms Maximum
- Automotive AEC-Q100 Qualified
- High Reliability:
  - Endurance: 1,000,000 write cycles
  - Data retention: 100 years
- Green Package Options (Lead-free/Halide-free/RoHS compliant)

Packages

- 8-Lead SOIC and 8-Lead TSSOP

Table of Contents

1. Package Types (not to scale)



2. Pin Descriptions

The descriptions of the pins are listed in Table 2-1.

Table 2-1. Pin Function Table

Name	8-Lead SOIC	8-Lead TSSOP	Function
CS	1	1	Chip Select
SK	2	2	Serial Data Clock
DI	3	3	Serial Data Input
DO	4	4	Serial Data Output
GND	5	5	Ground
ORG	6	6	Internal Organization
NC	7	7	No Connect
V_{CC}	8	8	Device Power Supply

2.1 Chip Select (CS)

The Chip Select (CS) pin is used to control device selection. The AT93C86A is selected when the CS pin is high. When the device is not selected, data will not be accepted via the Serial Data Input (DI) pin, and the Serial Output (DO) pin will remain in a high-impedance state.

2.2 Serial Data Clock (SK)

The Serial Data Clock (SK) pin is used to synchronize the communication between a master and the AT93C86A. Instructions, addresses or data present on the Serial Data Input (DI) pin is latched in on the rising edge of SK, while output on the Serial Data Output (DO) pin is also clocked out on the rising edge of SK.

2.3 Serial Data Input (DI)

The Serial Data Input (DI) pin is used to transfer data into the device. It receives instructions, addresses and data. Data is latched on the rising edge of the Serial Data Clock (SK).

2.4 Serial Data Output (DO)

The Serial Data Output (DO) pin is used to transfer data out of the AT93C86A. During a read sequence, data is shifted out on this pin after the rising edge of the Serial Data Clock (SK).

This pin also outputs the Ready/Busy status of the part if CS is brought high after being low for a minimum of t_{cs} and an erase or write operation has been initiated.

2.5 Ground (GND)

The ground reference for the power supply. The Ground (GND) pin should be connected to the system ground.

2.6 Internal Organization (ORG)

The Internal Organization (ORG) pin is used to select between the x16 or x8 memory organizations of the device. When the ORG pin is tied to V_{CC}, the x16 memory organization is selected. When the ORG pin is tied to GND, the x8 memory organization is selected.

If the ORG pin is left unconnected and the application does not load the input beyond the capability of the internal 1 MΩ pull-up resistor, then the x16 organization is selected.

2.7 Device Power Supply (V_{CC})

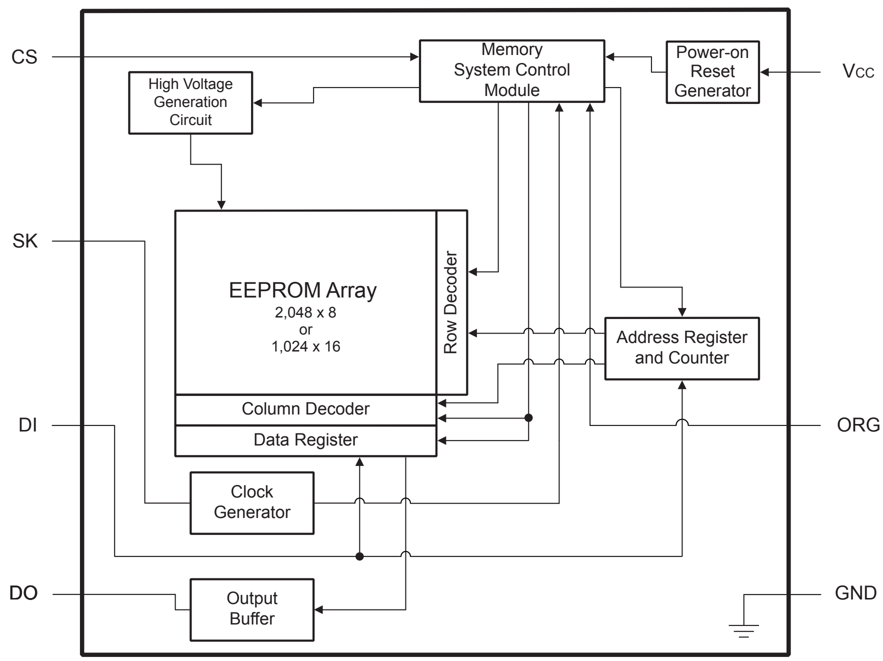
The Device Power Supply (V_{CC}) pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.

3. Description

The AT93C86A provides 16,384 bits of Serial Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 1,024 words of 16 bits each (when the ORG pin is connected to V_{CC}) and 2,048 words of 8 bits each (when the ORG pin is tied to GND). The device is optimized for use in many automotive applications where low-power and low-voltage operations are essential. The AT93C86A is available in space-saving 8-lead SOIC and 8-lead TSSOP packages. All packages operate from 2.7V to 5.5V.

The AT93C86A is enabled through the Chip Select (CS) pin and accessed via a three-wire serial interface consisting of Data Input (DI), Data Output (DO), and Serial Data Clock (SK). Upon receiving a `READ` instruction at DI, the address is decoded, and the data is clocked out serially on the DO pin. The write cycle is completely self-timed, and no separate erase cycle is required before write. The write cycle is only enabled when the part is in the Erase/Write Enable state. When CS is brought high following the initiation of a write cycle, the DO pin outputs the Ready/Busy status of the part.

3.1 Block Diagram



Note:

1. When the ORG pin is connected to V_{CC}, the x16 organization is selected. When it is connected to GND, the x8 organization is selected. If the ORG pin is left unconnected, and the application does not load the input beyond the capability of the 10 MΩ pull-up resistor, then the x16 organization is selected.

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Temperature under bias	-55°C to +125°C
Storage temperature	-65°C to +150°C
V_{CC}	6.25V
Voltage on any pin with respect to ground	-1.0V to +7.0V
DC output current	5.0 mA
ESD protection	2 kV

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.2 DC and AC Operating Range

Table 4-1. DC and AC Operating Range

AT93C86A		
Operating Temperature (Case)	Automotive Temperature Range	-40°C to +125°C
V_{CC} Power Supply	Low-Voltage Grade	2.7V to 5.5V

4.3 DC Characteristics

Table 4-2. DC Characteristics[1]

Parameter	Symbol	Minimum	Typical	Maximum	Units	Test Conditions
Supply Voltage	V_{CC1}	2.7	—	5.5	V	
Supply Voltage	V_{CC2}	4.5	—	5.5	V	
Supply Current	I_{CC1}	—	0.5	2.0	mA	V_{CC} = 5.0V, Read at 1 MHz
Supply Current	I_{CC2}	—	0.5	2.0	mA	V_{CC} = 5.0V, Write at 1 MHz
Standby Current (2.7V Option)	I_{SB1}	—	6.0	10.0	µA	V_{CC} = 2.7V, CS = 0V
Standby Current (5.0V Option)	I_{SB2}	—	10.0	15.0	µA	V_{CC} = 5.0V, CS = 0V
Input Leakage Current	I_{IL}	—	0.1	3.0	µA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	—	0.1	3.0	µA	V_{OUT} = 0 to V_{CC}
Input Low-Voltage	V_{IL}	-0.6	—	0.8	V	2.7V ≤ V_{CC} ≤ 5.5V (Note 2)
Input High-Voltage	V_{IH}	2.0	—	V_{CC} + 1	V	2.7V ≤ V_{CC} ≤ 5.5V (Note 2)

...........continued

Parameter	Symbol	Minimum	Typical	Maximum	Units	Test Conditions
Output Low-Voltage	V_{OL}	—	—	0.4	V	$2.7V \le V_{CC} \le 5.5V$, $I_{OL} = 2.1$ mA
Output High-Voltage	V_{OH}	2.4	—	—	V	$2.7V \le V_{CC} \le 5.5V$, $I_{OH} = -0.4$ mA

Note:

1. Applicable over recommended operating range from: $T_A = -40°C$ to $+125°C$, $V_{CC} = 2.5V$ to $5.5V$ (unless otherwise noted).
2. V_{IL} min and V_{IH} max are reference only and are not tested.

4.4 AC Characteristics

Table 4-3. AC Characteristics[1]

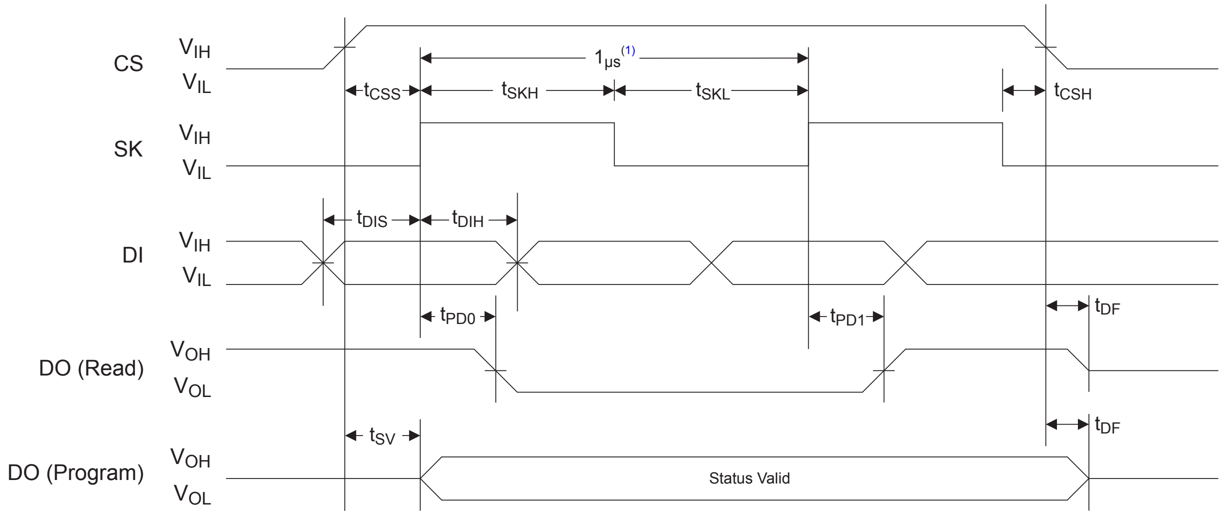
Parameter	Symbol	Minimum	Typical	Maximum	Units	Test Conditions
Clock Frequency, SK	f_{SK}	0	—	2	MHz	$4.5V \le V_{CC} \le 5.5V$
		0	—	1	MHz	$2.7V \le V_{CC} \le 5.5V$
High Time, SK	t_{SKH}	250	—	—	ns	$2.7V \le V_{CC} \le 5.5V$
Low Time, SK	t_{SKL}	250	—	—	ns	$2.7V \le V_{CC} \le 5.5V$
Minimum CS Low Time	t_{CS}	250	—	—	ns	$2.7V \le V_{CC} \le 5.5V$
CS Setup Time	t_{CSS}	50	—	—	ns	$2.7V \le V_{CC} \le 5.5V$, Relative to SK
DI Setup Time	t_{DIS}	100	—	—	ns	$2.7V \le V_{CC} \le 5.5V$, Relative to SK
CS Hold Time	t_{CSH}	0	—	—	ns	Relative to SK
DI Hold Time	t_{DIH}	100	—	—	ns	$2.7V \le V_{CC} \le 5.5V$, Relative to SK
Output Delay to 1	t_{PD1}	—	—	250	ns	$4.5V \le V_{CC} \le 5.5V$
		—	—	500	ns	$2.7V \le V_{CC} \le 5.5V$
Output Delay to 0	t_{PD0}	—	—	250	ns	$4.5V \le V_{CC} \le 5.5V$
		—	—	500	ns	$2.7V \le V_{CC} \le 5.5V$
CS to Status Valid	t_{SV}	—	—	250	ns	$2.7V \le V_{CC} \le 5.5V$
CS to DO in High-impedance	t_{DF}	—	—	100	ns	$4.5V \le V_{CC} \le 5.5V$, $CS = V_{IL}$
		—	—	150	ns	$2.7V \le V_{CC} \le 5.5V$, $CS = V_{IL}$
Write Cycle Time	t_{WP}	0.1	4	10	ms	$2.7V \le V_{CC} \le 5.5V$

Note:

1. Applicable over recommended operating range from $T_A = -40°C$ to $+125°C$, V_{CC} = As Specified, C_L = 1 TTL Gate and 100 pF (unless otherwise noted).

4.5 Synchronous Data Timing

Figure 4-1. Synchronous Data Timing



Note:

1. This is the minimum SK period.

4.6 Electrical Specifications

4.6.1 Power-Up Requirements and Reset Behavior

During a power-up sequence, the V_{CC} supplied to the AT93C86A should monotonically rise from GND to the minimum V_{CC} level, as specified in Table 4-1, with a slew rate no faster than 0.1 V/µs.

4.6.1.1 Device Reset

To prevent inadvertent write operations or any other spurious events from occurring during a power-up sequence, the AT93C86A includes a Power-on Reset (POR) circuit. Upon power-up, the device will not respond to any commands until the V_{CC} level crosses the internal voltage threshold (V_{POR}) that brings the device out of Reset and into Standby mode.

The system designer must ensure the instructions are not sent to the device until the V_{CC} supply has reached a stable value greater than or equal to the minimum V_{CC} level. Additionally, once the V_{CC} is greater than or equal to the minimum V_{CC} level, the bus master must wait at least t_{PUP} before sending the first command to the device. See Power-up Conditions[1] for the values associated with these power-up parameters.

Table 4-4. Power-up Conditions[1]

Symbol	Parameter	Min.	Max.	Units
t_{PUP}	Time required after V_{CC} is stable before the device can accept commands	100	—	µs
V_{POR}	Power-on Reset Threshold Voltage	—	1.5	V
t_{POFF}	Minimum time at V_{CC} = 0V between power cycles	500	—	ms

Note:

1. These parameters are characterized but they are not 100% tested in production.

If an event occurs in the system where the V_{CC} level supplied to the AT93C86A drops below the maximum V_{POR} level specified, it is recommended that a full power cycle sequence be performed by first driving the V_{CC} pin to GND, waiting at least the minimum t_{POFF} time and then performing a new power-up sequence in compliance with the requirements defined in this section.

4.6.2 Pin Capacitance

Table 4-5. Pin Capacitance[1]

Symbol	Test Condition	Max.	Units	Conditions
C_{OUT}	Output Capacitance (DO)	5	pF	V_{OUT} = 0V, T_A = 25°C, F = 1.0 MHz, V_{CC} = +5V
C_{IN}	Input Capacitance (CS, SK, DI, ORG)	5	pF	V_{IN} = 0V, T_A = 25°C, F = 1.0 MHz, V_{CC} = +5V

Note:

1. This parameter is characterized but is not 100% tested in production.

4.6.3 EEPROM Cell Performance Characteristics

Table 4-6. EEPROM Cell Performance Characteristics

Operation	Test Condition	Min.	Max.	Units
Write Endurance[1]	T_A = 25°C, V_{CC} = 5.0V	1,000,000	—	Write Cycles
Data Retention[1]	T_A = 55°C	100	—	Years

Note:

1. Performance is determined through characterization and the qualification process.

5. Device Commands and Addressing

The AT93C86A is accessed via a simple and versatile three-wire serial communication interface. Device operation is controlled by seven instructions issued by the Host processor. A valid instruction starts with a rising edge of CS and consists of a Start bit (SB), followed by the appropriate opcode, and the desired memory address location.

Table 5-1. AT93C86A Instruction Set

Instruction	SB	Opcode	Address		Data		Comments
			X8(1)	X16(1)	X8	X16	
`READ`	1	10	A_{10}-A_0	A_9-A_0			Reads data stored in memory at specified address.
`EWEN`	1	00	11XXXXXXXXX	11XXXXXXXX			Write Enable must precede all programming modes.
`ERASE`	1	11	A_{10}-A_0	A_9-A_0			Erases memory location A_N-A_0.
`WRITE`	1	01	A_{10}-A_0	A_9-A_0	D_7-D_0	D_{15}-D_0	Writes memory location A_N-A_0.
`ERAL`	1	00	10XXXXXXXXX	10XXXXXXXX			Erases all memory locations. Valid only at V_{CC2}. See Table 4-2.
`WRAL`	1	00	01XXXXXXXXX	01XXXXXXXX	D_7-D_0	D_{15}-D_0	Writes all memory locations. Valid only at V_{CC2}. See Table 4-2
`EWDS`	1	00	00XXXXXXXXX	00XXXXXXXX			Disables all programming instructions.

Note:

1. The ‘`X`’ in the address field represents a “don’t care” bit and must be sent to the device.

Table 5-2. Organization Key for Timing Diagrams

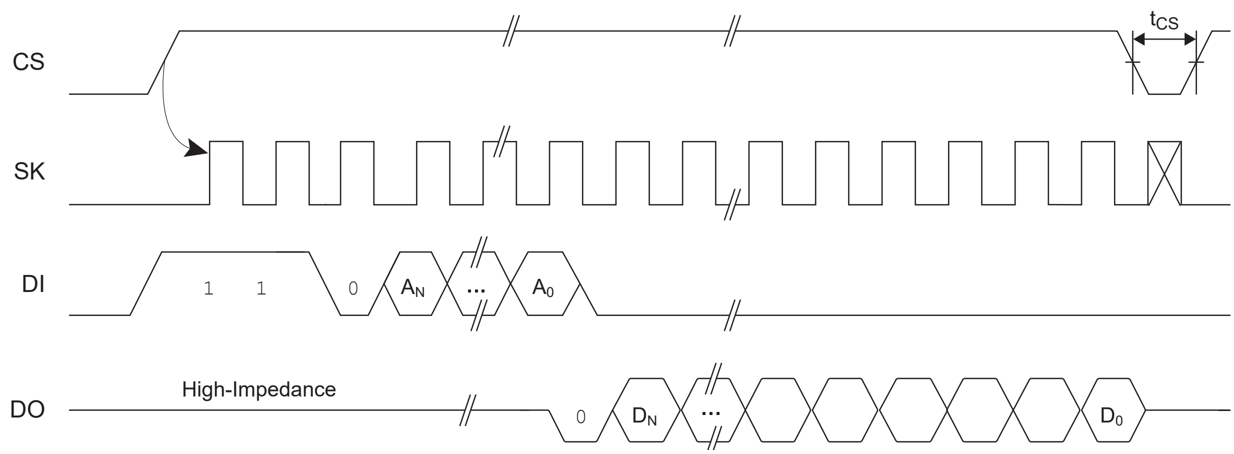
I/O	AT93C86A (16K)	
	x8	x16
A_N	A_{10}	A_9
D_N	D_7	D_{15}

5.1 READ

The `READ` instruction contains the address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the DO pin. Output data changes are synchronized with the rising edges of the SK pin. The AT93C86A supports sequential read operations. The device will automatically increment the internal Address Pointer and clock out the next memory location as long as Chip Select (CS) is held high. In this case, the dummy bit (Logic ‘`0`’) will not be clocked out between memory locations, thus allowing for a continuous stream of data to be read.

Note: A dummy bit (logic ‘`0`’) precedes the initial 8-bit or 16-bit data output string.

Figure 5-1. READ Timing

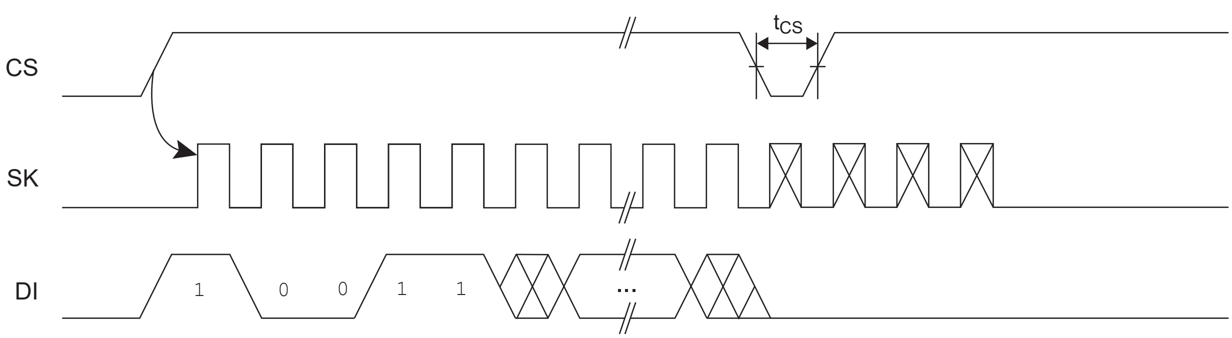


5.2 Erase/Write Enable (EWEN)

To ensure data integrity, the part automatically goes into the Erase/Write Disable (`EWDS`) state when power is first applied. An Erase/Write Enable (`EWEN`) instruction must be executed first before any programming instructions can be carried out.

Note: Once in the write-enabled state, programming remains enabled until an `EWDS` instruction is executed, or V_{CC} power is removed from the part.

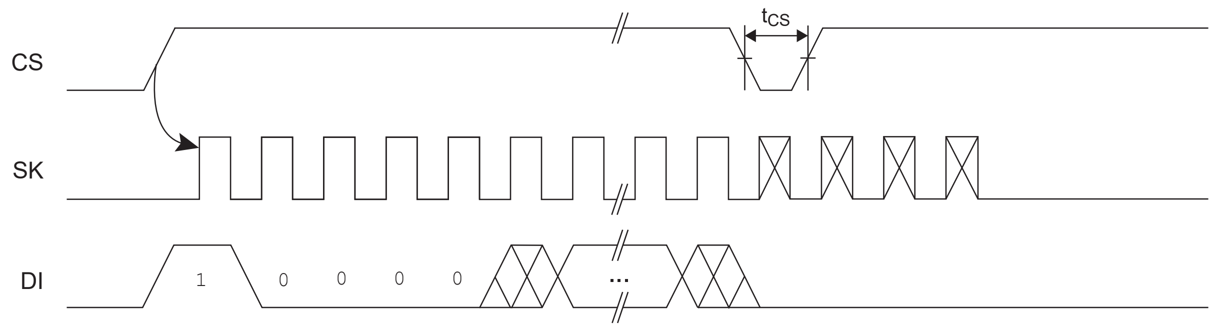
Figure 5-2. EWEN Timing



5.3 Erase/Write Disable (EWDS)

To protect against accidental data disturbance, the Erase/Write Disable (`EWDS`) instruction disables all programming modes and should be executed after all programming operations. The operation of the `READ` instruction is independent of both the `EWEN` and `EWDS` instructions and can be executed at any time.

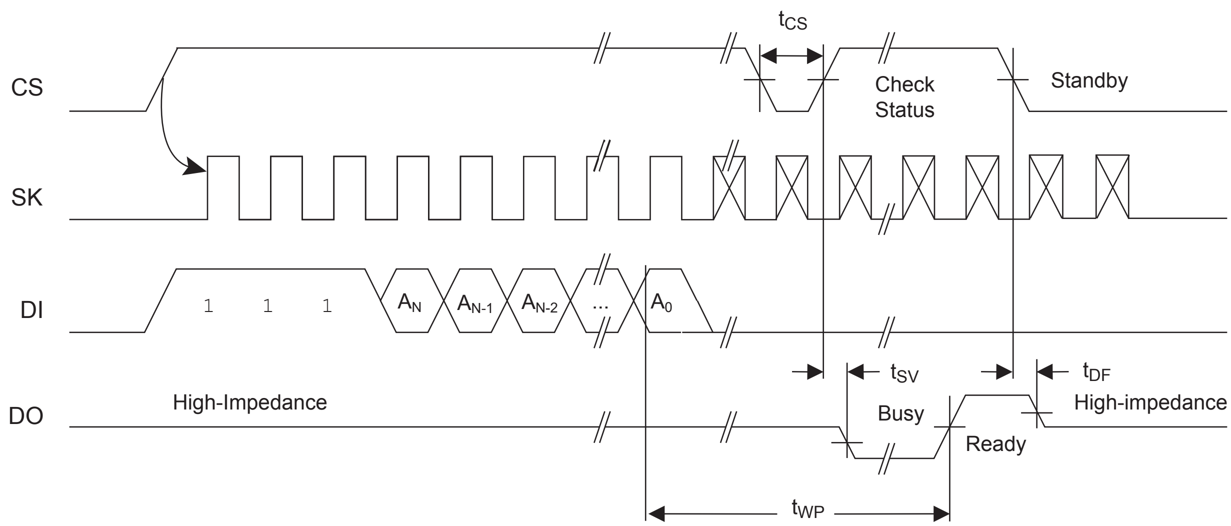
Figure 5-3. EWDS Timing



5.4 Erase Operation (ERASE)

The `ERASE` instruction programs all bits in the specified memory location to the logic '`1`' state. The self-timed erase cycle starts once the `ERASE` instruction and address are decoded. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of t_{CS}. A logic '`1`' at the DO pin indicates that the selected memory location has been erased, and the part is ready for another instruction.

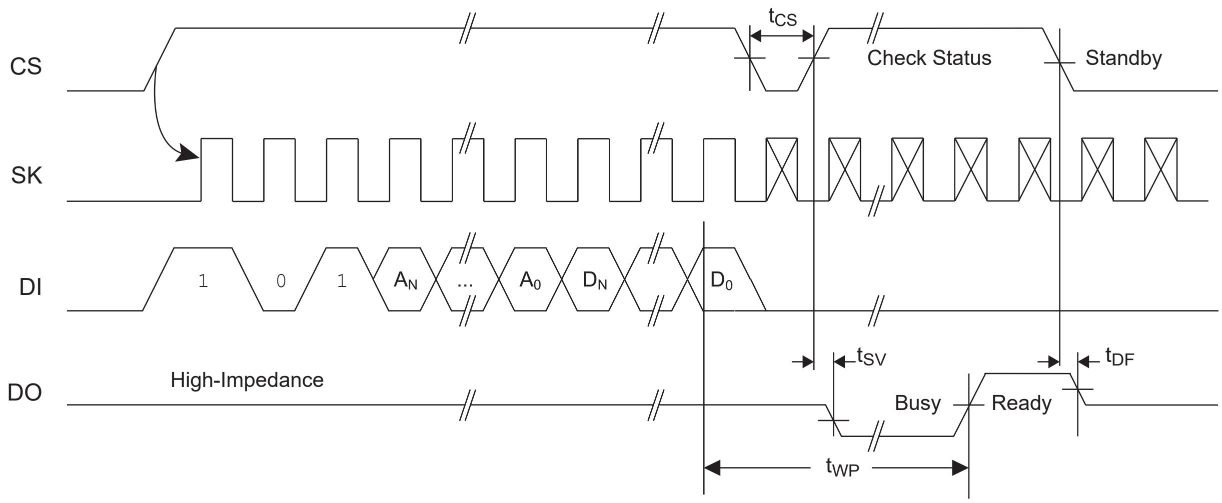
Figure 5-4. ERASE Timing



5.5 Write Operation (WRITE)

The `WRITE` instruction contains the 8 bits or 16 bits of data to be written into the specified memory location. The self-timed programming cycle, t_{WP}, starts after the last bit of data is received at DI pin. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of t_{CS}. A logic '`0`' at DO indicates that programming is still in progress. A logic '`1`' indicates that the memory location at the specified address has been written with the data pattern contained in the instruction, and the part is ready for further instructions. A Ready/Busy status cannot be obtained if CS is brought high after the end of the self-timed programming cycle, t_{WP}.

Figure 5-5. WRITE Timing

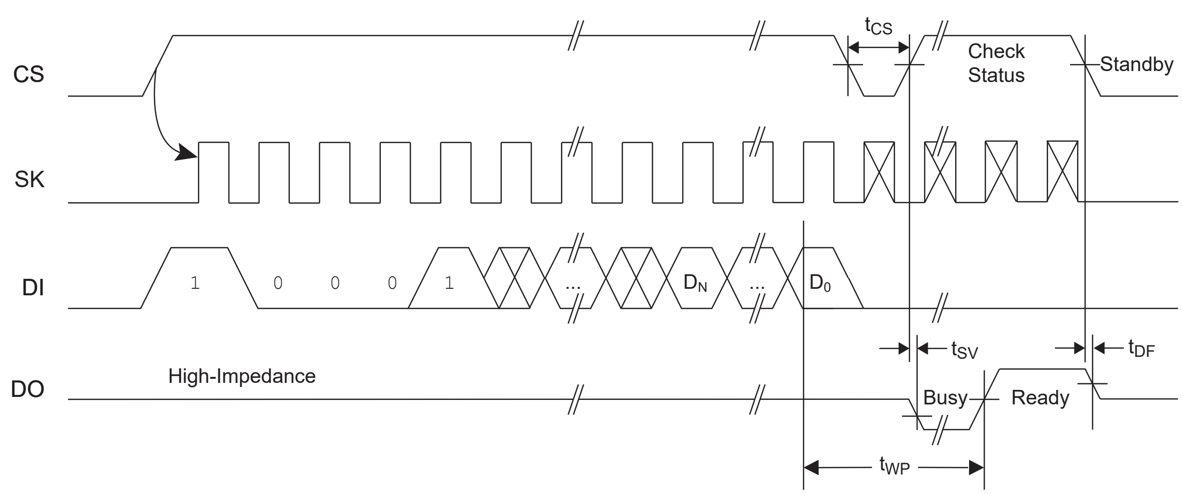


5.6 Write All (WRAL)

The Write All (`WRAL`) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of t_{CS}.

Note: The `WRAL` instruction is valid only at V_{CC2} (see Table 4-2).

Figure 5-6. WRAL Timing

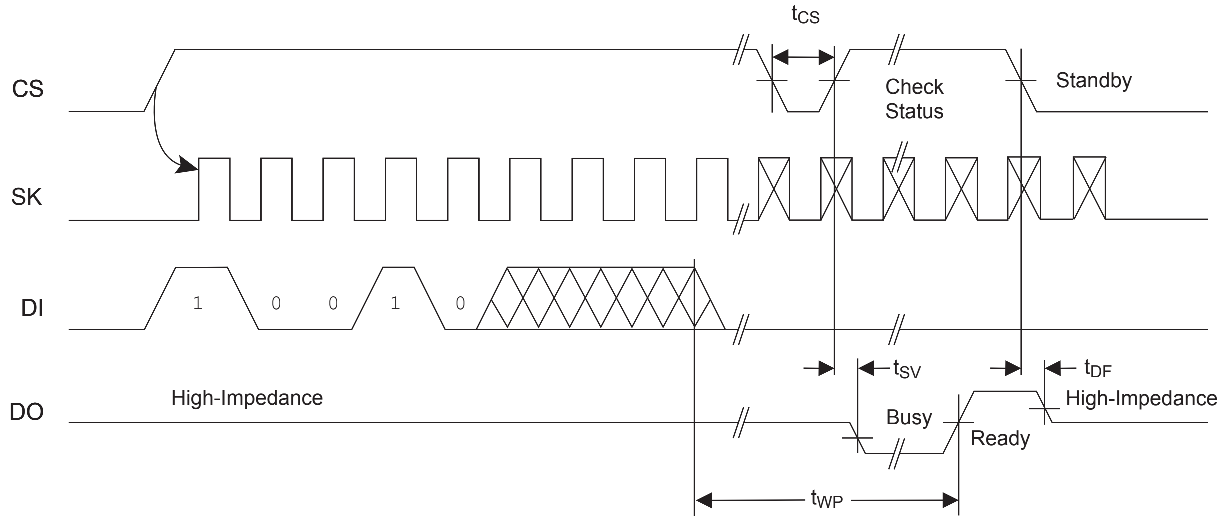


5.7 Erase All (ERAL)

The Erase All (`ERAL`) instruction programs every bit in the memory array to the logic '`1`' state and is primarily used for testing purposes. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of t_{CS}.

Note: The `ERAL` instruction is valid only at V_{CC2} (see Table 4-2).

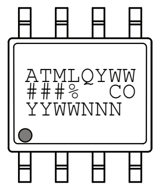
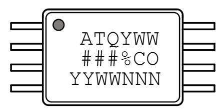
Figure 5-7. ERAL Timing



6. Packaging Information

6.1 Package Marking Information

AT93C86A: Package Marking Information

8-lead SOIC	8-lead TSSOP
	

Catalog Number Truncation

AT93C86A	Truncation Code ###: 86A

Date Codes					**Voltages**
YY = Year		Y = Year		WW = Work Week of Assembly	% = Minimum Voltage
16: 2016	20: 2020	6: 2016	0: 2020	02: Week 2	Blank: 2.7V min
17: 2017	21: 2021	7: 2017	1: 2021	04: Week 4	
18: 2018	22: 2022	8: 2018	2: 2022	...	
19: 2019	23: 2023	9: 2019	3: 2023	52: Week 52	

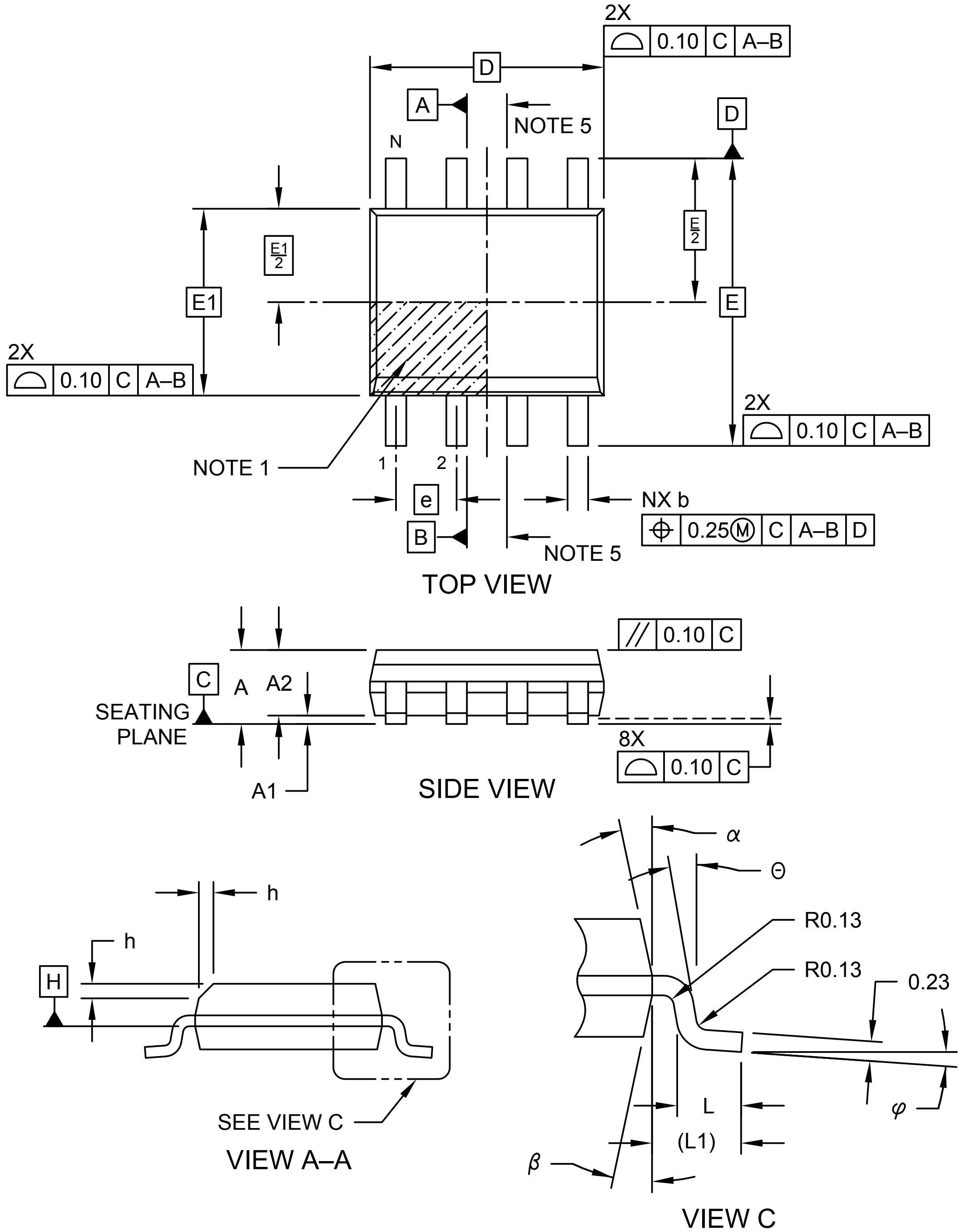
Country of Origin	**Device Grade**	**Atmel Truncation**
CO = Country of Origin	Q: Automotive Grade	AT: Atmel ATM: Atmel ATML: Atmel

Lot Number or Trace Code

NNN = Alphanumeric Trace Code

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

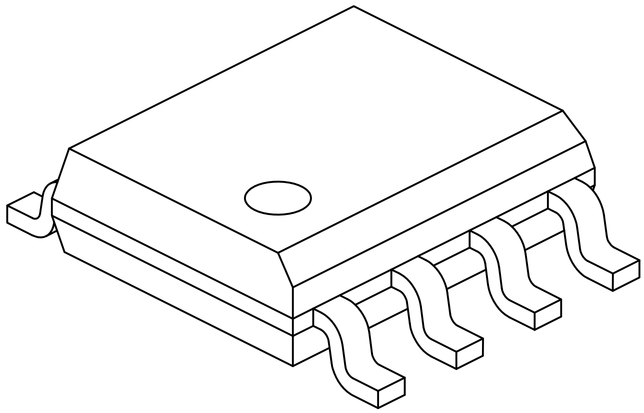
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-SN Rev F Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

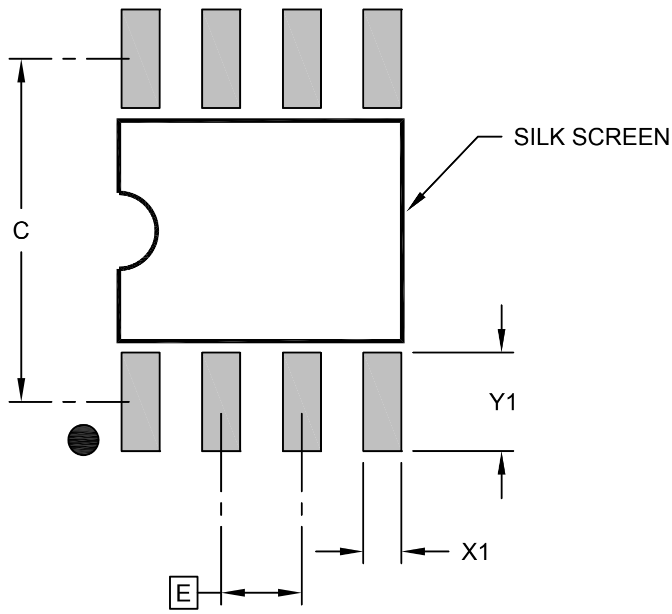
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev F Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

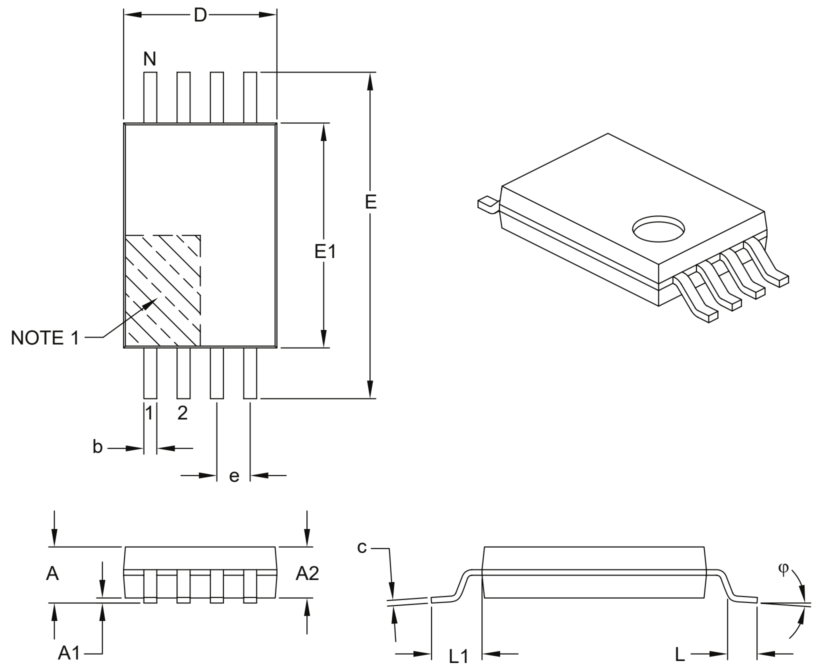
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev F

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E	6.40 BSC		
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	2.90	3.00	3.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

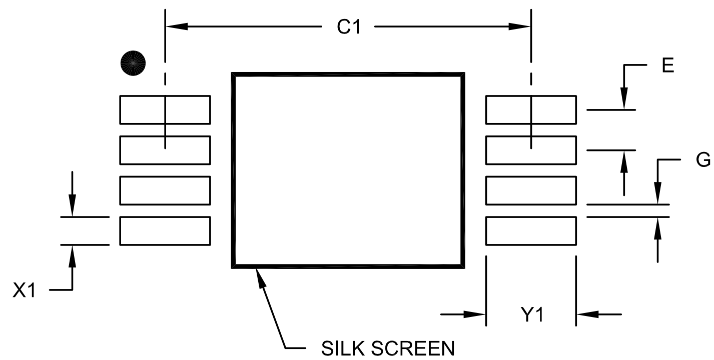
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086B

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2086A

7. Revision History

Revision A (February 2020)
Updated to the Microchip template. Microchip DS20006303 replaces Atmel document 5096. Updated Package Marking Information. Removed lead finish designation. Updated trace code format in package markings. Updated section content throughout for clarification. Updated the SOIC and TSSOP package drawings to Microchip format.

Atmel AT93C86A 5096 Revision H (January 20017)
Added Bulk (Tube) shipping carrier option. Changed standard quantity Tape and Reel ption to "T". Updated Atmel ordering code information table.

Atmel AT93C86A 5096 Revision G (February 2016)
Updated 8S1 package drawing and ordering information layout. Added the section, "Power Recommendation".

Atmel AT93C86A 5096 Revision F (October 2014)
Updated packages 8S1 and 8A2 to 8X, template, Atmel logos, and disclaimer page. No change in functional specification

Atmel AT93C86A 5096 Revision E (January 2008)
Moved to new template. Replaced Table 5 with correct version

Atmel AT93C86A 5096 Revision D (February 2007)
Removed PDIP package offering. Removed Pb'd part numbers.

Atmel AT93C86A 5096 Revision C (September 2006)
Revision history implemented. Removed 'Preliminary' status from data sheet.

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A T 9 3 C 8 6 A - 1 0 S Q - 2.7 - T

Shipping Carrier Option
Blank = Bulk (Tubes)
T = Tape and Reel, Standard Quantity Option

Product Family
93C = Microwire-compatible Three-Wire Serial EEPROM

Operating Voltage
2.7 = 2.7V to 5.5V

Device Density
86 = 16-Kilobit

Package Device Grade
Q = AutomotiveTemperature Range (-40°C to +125°C)

Device Revision

Package Type
S = SOIC
T = TSSOP

Speed Type
10 = Default value

Examples

Device	Package	Package Drawing Code	Package Option	Voltage Range	Shipping Carrier Option	Device Grade
AT93C86A-10SQ-2.7-T	SOIC	SN	S	2.7V to 5.5V	Tape and Reel	Automotive Temperature (-40°C to 125°C)
AT93C86A-10TQ-2.7	TSSOP	ST	T	2.7V to 5.5V	Bulk (Tubes)	

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