PIC24FJ128GC010 Family Silicon Errata and Data Sheet Clarification

The PIC24FJ128GC010 family devices that you have received conform functionally to the current Device Data Sheet (DS30009312**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC24FJ128GC010 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**B3**).

Data Sheet clarifications and corrections start on Page 6, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 3 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 3 programmer/debugger or PICkit 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various PIC24FJ128GC010 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision
		B3
PIC24FJ128GC010	85H	04H
PIC24FJ128GC006	89H	
PIC24FJ64GC010	84H	
PIC24FJ64GC006	88H	

Note 1: The Device and Revision IDs (DEVID and DEVREV) are located at the last two implemented addresses in program memory.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)
				B3
12-Bit Pipeline A/D	Sample Lists	1.	When multiple sample lists are configured to perform auto-scan, A/D errors may occur.	X
12-Bit Pipeline A/D	Sample Lists	2.	The A/D may not consistently generate sample list interrupt flag events when the FRC is used to derive the A/D clock.	X
12-Bit Pipeline A/D	Calibration	3.	The A/D does not hardware self-calibrate correctly when the A/D module is first powered on.	X
12-Bit Pipeline A/D	Accumulation	4.	The A/D accumulation feature with the ACCIF interrupt generation enabled.	X
12-Bit Pipeline A/D	Accuracy	5.	Unexpected A/D results under specific conditions.	X
Output Compare	Accuracy	6.	Very low speed or frequency output compare operations relying on an external timer.	X
CTMU	Edge Enable	7.	Enabling edges (EDGEN = 1) can generate a glitch.	X
CTMU	Pulse or Delay Generation	8.	Pulse or Delay Generation mode is not functional.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**B3**).

1. Module: 12-Bit Pipeline A/D

When multiple sample lists are configured to perform auto-scan operations, and are triggered simultaneously (or close enough that the first sample list is still busy when the subsequent one is triggered), unexpected A/D result values may be generated.

Work around

If using auto-scan operations, only enable and trigger one sample list at a time.

Affected Silicon Revisions

B3						
X						

2. Module: 12-Bit Pipeline A/D

The A/D may not consistently generate sample list-specific interrupt flag events, SLxIF (ADSTATL<3:0>), when the FRC is used to derive the A/D clock (e.g., by setting the ADRC bit (ADCON3<15>)).

Work around

Sample list interrupts are generated normally when using the system clock to derive the A/D clock (e.g., ADRC = 0), even if the system clock is derived from the FRC. Alternatively, if the ADRC bit is set, the firmware may still use the top level A/D interrupt, AD1IF (IFS0<13>), as the AD1IF flag event and the A/D result data is still generated normally.

Affected Silicon Revisions

B3						
X						

3. Module: 12-Bit Pipeline A/D

The A/D does not hardware self-calibrate correctly when the A/D module is first powered on.

Work around

In order to reliably initiate a hardware self-calibration of the A/D, the firmware needs to turn on the A/D, wait until ADREADY = 1 and then write '1' to the ADCAL bit to initiate a new calibration operation. The A/D will then perform the self-calibration in the background. Once it is done, it will set the ADREADY bit to '1' and the A/D will be ready to use.

Affected Silicon Revisions

B3						
X						

4. Module: 12-Bit Pipeline A/D

When using the A/D accumulation feature with the ACCIF interrupt generation enabled (ACIE = 1), the ACCIF (ADSTATL<4>) interrupt flag is not set if the accumulation operation was started with a COUNT<7:0> (ACCONL<7:0>) value of '1'.

Work around

The ACCIF interrupt works normally for all other accumulation count values (other than '1'). If only one A/D measurement is planned, it is suggested not to use the accumulation feature. Perform a normal A/D measurement instead.

Affected Silicon Revisions

B3						
X						

5. Module: 12-Bit Pipeline A/D

Unexpected A/D result data may occur when the ADC is operated in Single-Ended Input mode and the analog input voltage is within the upper 1/3 of the ADC input voltage range.

Work around

A normal result is obtained when operating in Differential Input mode. If the application uses Single-Ended Input mode, a normal result can be obtained if the application simultaneously does all of the following:

- The positive ADC reference voltage is maintained lower than (AV_{DD} – 0.5V). This can be implemented either with an external reference or by using the internal BGBUF1 source (e.g., configured for 2.048V or 2.560V).
- The ADC is operated with the REFPUMP bit (ADCON2<1>) = 1.
- The ADC is maintained continuously converting at a high rate (e.g., ≥ 4 Msps). This can be implemented by using a low-priority list with a continuous trigger option to keep the ADC busy. The conversions required by the application should be done by using higher priority lists. The code in Example 1 shows the settings for the low priority list to maintain the high conversion rate.

EXAMPLE 1: LOW-PRIORITY LIST CONFIGURATION TO MAINTAIN A HIGH CONVERSION RATE

```
//Configure Sample List 3 (SL3, which has lowest priority) to continuously use all free
//ADC clock cycles by performing dummy conversion operations on an internal channel VREF-.
ADL3CONL = 0;
ADL3CONH = 0;
ADL3CONLbits.SLSIZE = 1-1; //1 channel is scanned.
ADL3CONLbits.SLTSRC = 2;   //Trigger is generated every clock when SAMP = 0.
ADTBLx = 124;              //124 = VREF-. Replace ADTBLx with real value after allocating SL0-SL2.
ADL3CONLbits.SLEN = 1;     //Enable SL3.
ADL3CONLbits.SAMP = 0;     //Trigger SL3 on every ADC clock period.
//Use Sample Lists 0-2 for sampling the actual application ADC channel(s) of interest.
//The SL0-SL2 have higher priority than SL3 trigger events, so having SL3 free running
//at speed doesn't decrease the useful ADC bandwidth/sample rate achievable on SL0-SL2.
//Note: Avoid auto-scan when using multiple sample lists (see errata #1).
```

Affected Silicon Revisions

B3						
X						

6. Module: Output Compare

Certain very low-speed or frequency output compare operations, relying on an external timer (e.g.,Timer2), may not work correctly if the external timer is configured for a prescalar setting other than 1:1.

Work around

If using output compare operations with an external timer, configure the timer to operate in the 1:1 Prescaler mode.

Affected Silicon Revisions

B3						
X						

7. Module: CTMU

Enabling edges (EDGEN = 1) generates a glitch (edge) if the CTEDx pin is set for a falling edge and the level on this pin is low, or if the CTEDx pin is set for a rising edge and the level on this pin is high.

Work around

External AND logic can be used for each CTEDx pin to gate these control signals. EDGEN should not be changed (always set to '1').

Affected Silicon Revisions

B3						
X						

8. Module: CTMU

When the CTMU is configured in Pulse or Delay Generation mode with the TGEN bit = 1 (CTMUCON1[12] = 1), the EDG1STAT and EDG2STAT bits (CTMUCON2[9:8]) do not get set. The CTMU current source is always disabled.

Work around

None.

Affected Silicon Revisions

B3						
X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS30009312**D**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Electrical Characteristics

In Table 37-28, the test conditions for A/D Accuracy Parameters AD21, AD22, AD23 and AD24 have changed. The Minimum and Maximum values for AD21 (Integral Nonlinearity) are modified. The changes are shown below in bold.

TABLE 37-28: 12-BIT PIPELINE A/D MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	Symbol	Characteristic	Min.	Typ	Max.	Units	Conditions
A/D Accuracy							
AD21	INL	Integral Nonlinearity	**-9**	—	**+9**	LSb	**AVSS = VREFL = 0V, AVDD = 3.3V, VREFH = 2.56V**
AD22	DNL	Differential Nonlinearity	-3	—	+3	LSb	**AVSS = VREFL = 0V, AVDD = 3.3V, VREFH = 2.56V**
AD23	GERR	Gain Error	-8	—	+8	LSb	**AVSS = VREFL = 0V, AVDD = 3.3V, VREFH = 2.56V**
AD24	EOFF	Offset Error	-12	—	+12	LSb	**AVSS = VREFL = 0V, AVDD = 3.3V, VREFH = 2.56V**

APPENDIX A: REVISION HISTORY

Rev A Document (5/2013)

Initial release of this document.

Rev B Document (9/2013)

Added data sheet clarifications 1 (Device Overview), 2-3 (Electrical Characteristics), 4 (CMxCON Register), 5 (DOZE<2:0> and DOZEN Bits), 6 (Decoupling Capacitors) and 7 (DACxCON Register).

Rev C Document (4/2014)

Corrects device family to “PIC24FJ128GC010 family”, to be consistent with the family name provided on all other literature.

Corrects the module titles for data sheet clarifications 4 though 7, to be consistent with existing practice. The clarifications themselves are unaffected.

Added data sheet clarifications 8 (Power-Saving Features) and 9 (12-Bit High-Speed, Pipeline A/D Converter).

Rev D Document (10/2014)

Removes all data sheet clarifications as they were addressed in the new revision of the data sheet.

Rev E Document (12/2016)

Updated existing silicon errata issue 5 (12-Bit Pipeline A/D).

Rev F Document (4/2017)

Added data sheet clarification 1 (Electrical Characteristics).

Rev G Document (11/2022)

Added silicon errata issue 8 (CTMU).

NOTES:

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