AN3020

USB-to-SPI Bridging with Microchip USB72xx Hubs

Author: *Shiva Balasubramanian*
Microchip Technology Inc.

INTRODUCTION

The USB-to-SPI bridging feature of Microchip USB hubs provides system designers with an expanded system control and a potential BOM reduction. The use of a separate USB-to-SPI device is no longer required and a downstream USB port is not lost as a result of implementing the standalone USB-to-SPI device. This feature is available on Microchip hubs that contain an internal Hub Feature Controller (HFC) and a Serial Peripheral Interface (SPI) interface. These hubs include USB7202, USB7250, USB7251, USB7252 and USB7256.

Commands may be sent from the USB Host to the internal HFC device in the Microchip hub to perform the following functions:

- Get Hub Information
- Reset the Hub
- Force Boot from Internal ROM
- Enable SPI Pass-Through Interface
- Disable SPI Pass-Through Interface
- SPI Pass-Through Read/Write

Sections

This document includes the following topics:

References

Consult the following documents for details on the specific parts referred to in this document:

- *Microchip USB7202 Data Sheet*
- *Microchip USB7250 Data Sheet*
- *Microchip USB7251 Data Sheet*
- *Microchip USB7252 Data Sheet*
- *Microchip USB7256 Data Sheet*
- *Microchip SST26VF016B Data Sheet*
- *Microchip AN2935 Configuration of the USB7202/USB7206/USB725x Application Note*

GENERAL INFORMATION

The USB72xx series of USB hubs supports native USB Type-C on the upstream side and a combination of native USB Type-C and standard USB 2.0 ports on the downstream side. On successful enumeration of the hub, the USB device tree on the host shows a USB2.0 hub instance, a USB3.0 hub instance, and a third device which is the HFC. Refer to Table 1 for details on the default HFC settings by part number.

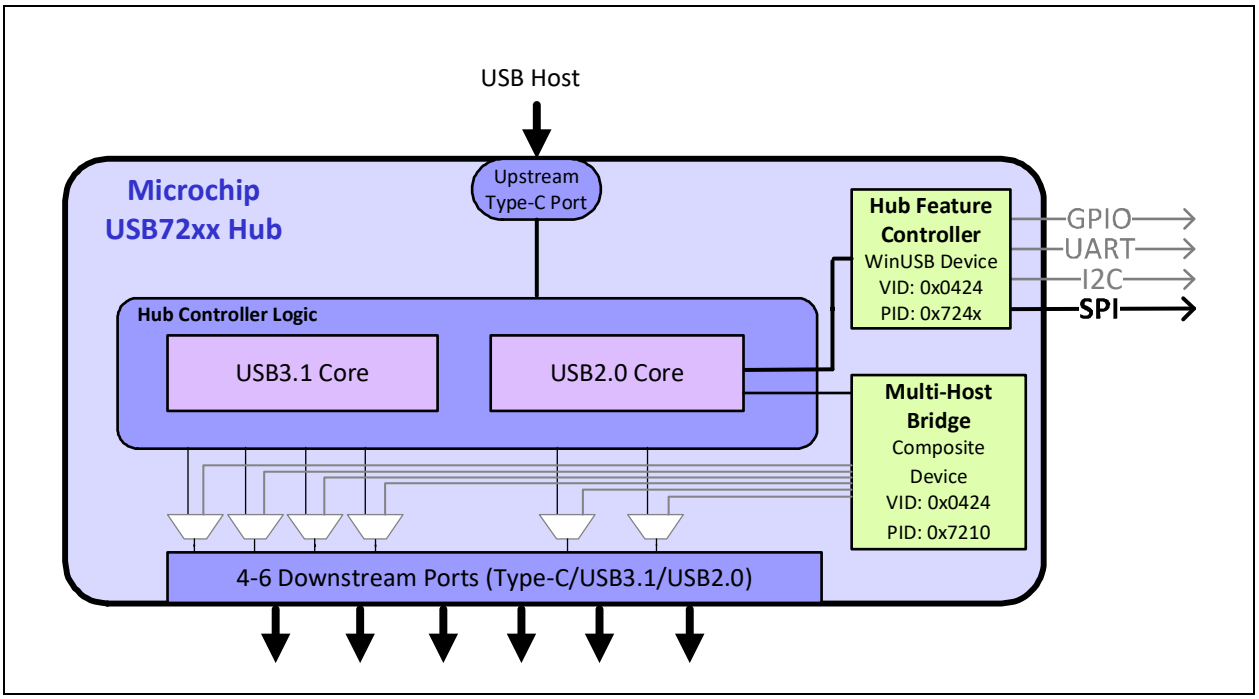
TABLE 1: DEFAULT SETTINGS FOR HUB FEATURE CONTROLLER ENABLE

Part Number	Part Summary	Hub Controller Default Setting	USB3 PID	USB2 PID
USB7202	4-Port USB3.1 Gen2 Hub	Enabled on Port 6	0x7202	0x4202
USB7206	6-Port USB3.1 Gen2 Hub	Enabled on Port 8	0x7206	0x4206
USB7250	4-Port USB3.1 Gen2 Hub with power delivery on 3 ports	Enabled on Port 6	0x7250	0x4250
USB7251	4-Port USB3.1 Gen2 Hub with power delivery on 2 ports	Enabled on Port 6	0x7251	0x4251
USB7252	4-Port USB3.1 Gen2 Hub with power delivery on 1 port	Enabled on Port 6	0x7252	0x4252
USB7256	6-Port USB3.1 Gen2 Hub with power delivery on 1 port	Enabled on Port 8	0x7256	0x4256

The HFC is a USB device that enumerates on an extra internal non-removable USB2.0 port (See Figure 1.). It is mapped to the highest numbered port on the hub. The base Product ID (PID) for the HFC is 0x7240. Based on the features enabled in an SKU, the last nibble of this PID may vary. The HFC is enabled by default in all the SKUs and can be disabled by setting bit 8 of the runtime flag register at address 0xBFD23408.

To use the bridging features of the hub, all bridging host commands must be addressed to the HFC which in turn will transmit the data to the appropriate serial interface lines.

FIGURE 1: MICROCHIP HUB FEATURE CONTROLLER BLOCK DIAGRAM



SPI Bridging Commands

The following SPI functions are supported:

- Get Hub Information
- Reset the Hub
- Force Boot from Internal ROM
- Disable the SPI Pass-Through Interface
- Enable the SPI Pass-Through Interface
- SPI Pass-Through Read/Write

GET HUB INFORMATION

The host can get information about the hub by issuing the GET_HUB_INFO command. In response, the hub sends a packet that contains information about the device revision, firmware version, and boot mode.

RESET THE HUB

The host can soft reset the hub externally by issuing the CMD_DEV_RESET command. This forces the hub firmware to start execution from 0x000000 and go through the boot sequence again.

FORCE BOOT FROM INTERNAL ROM

In situations where the hub is executing out of an external SPI ROM and the host wants to perform SPI pass-through transfers with the SPI ROM, this command sequence can be used to force the hub to boot and execute from the internal ROM.

ENABLE THE SPI PASS-THROUGH INTERFACE

To acquire the SPI interface, the host must send a CMD_SPI_ENTER_PASSTHRU SETUP packet before performing any SPI read/write commands. The SPI interface may operate at either 30 MHz or 60 MHz.

DISABLE THE SPI PASS-THROUGH INTERFACE

The SPI pass-through interface can be disabled after read/write operations by sending a CMD_SPI_EXIT_PASSTHRU SETUP packet.

SPI PASS-THROUGH READ/WRITE

The SPI pass-through interface allows single-/multi-byte write access and read access. In case of these operations, the SPI interface functions as a complete pass-through, which means any SPI data sent as a payload in the USB transfer gets transferred to the SPI lines directly. Therefore, the host must properly arrange data payloads in the appropriate SPI-compatible format and bit order, including the SPI slave device address. Up to 256 bytes can be written to an SPI peripheral using an SPI Write command sequence.

Data can also be read from an SPI peripheral using a combination of SPI read/write pass-through transfers. The host first needs to send a SETUP packet that informs the hub about the number of bytes to be read. Following this command, the hub stores the requested data bytes in an internal register at 0xBFD22310. The SPI Read command sequence can then be initiated by the host to retrieve the data. Up to 512 bytes of data can be read per SPI Read command sequence.

SPI Interface SETUP Requirements

SPI MASTER INTERFACE

The SPI interface always acts as an SPI master.

SELECTING SPI FREQUENCY

The SPI interface can operate at either 30 MHz or 60 MHz. The hub firmware configures the SPI interface to operate at 60 MHz by default. This can be changed by writing to bit 7 of the SPI_CTL register at address 0xBF802400, where:

- `0` = 30 MHz
- `1` = 60 MHz

SPI firmware images are designed to operate at specific speeds. Refer to the release notes of the SPI firmware image in use prior to making any modifications to the SPI interface speed.

SPI MODES OF OPERATION

Both SPI modes 0 and 3 are supported:

- Mode 0: Clock Polarity = 0, Clock Edge = 1
- Mode 3: Clock Polarity = 1, Clock Edge = 0

Dual Output Enable mode is also supported.

The default mode of operation is Mode 0 with the Dual Output Enable mode disabled. If the mode of operation is to be modified, a register write to the SPI_CTL (0xBF802400) register must be performed.

PART NUMBER INFORMATION

Part Summary

In USB72xx devices, SPI interface signals are associated with dedicated pins. See Table 2 for information on the pins.

TABLE 2: USB72XX SPI INTERFACE PIN NUMBERS

Device	SPI_DI/ SPI_D1	SPI_CE_N	SPI_DO/ SPI_D0	SPI_CLK	SPI_D2	SPI_D3
USB7202	71	69	70	68	72	73
USB7206	71	69	70	68	72	73
USB7250	71	69	70	68	72	73
USB7251	71	69	70	68	72	73
USB7252	71	69	70	68	72	73
USB7256	71	69	70	68	72	73

MICROCHIP SOFTWARE SOLUTIONS

Microchip currently offers two publicly available software solutions to facilitate USB-to-SPI Bridging in a USB72xx series hub on Windows® and Linux®.

MPLAB Connect Configurator Package (For Windows®)

The MPLAB Connect Configurator (MPLABCC) package consists of both GUI-based and CLI-based tools which support USB-to-SPI Bridging in a standalone form. In addition, it contains a Dynamically Linked Library (DLL) for Windows which can be used for implementing USB-to-SPI Bridging feature in custom applications using C programming language. The MPLABCC DLL consists of the following:

- User's guide: A detailed description of how to use the DLL API to call each function
- Release notes
- Library files: A .dll and a .lib file
- Example code

Application Code Examples (For Linux®)

For implementing USB-to-SPI Bridging on Linux, you can use one of the following USB72xx Linux Application Code Examples (ACEs):

- ACE002 USB Pseudo-OTP Programmer: This ACE demonstrates how to program the pseudo-OTP and read it back using USB-to-SPI Bridging commands.
- ACE003 USB SPI Firmware Programmer: This ACE demonstrates how to program the hub firmware to different types of Microchip SPI flash memories using USB-to-SPI Bridging commands.
- ACE004 USB-to-SPI Bridging: This ACE demonstrates how to transfer data to and from the SPI interface in USB72xx using USB-to-SPI Bridging commands.

These application examples use libusb library for Linux to build and send USB packets as described in Low-Level Implementation. Each ACE is a full-feature code example that consists of:

- Example code with minimal abstraction and in-line comments describing the various steps involved
- A Makefile
- README

These ACEs can be used as standalone applications or can be integrated into existing applications.

Note:	Visit the product page on www.microchip.com for any of the hubs listed in this document to download the software solution for the desired operating system.

LOW-LEVEL IMPLEMENTATION

The USB-to-SPI Bridging features may be implemented at the lowest level if users have the ability to build USB packets. This approach is required if users are not using a Windows or Linux host system and cannot use the solutions described in Microchip Software Solutions.

The details of these low-level USB packets are shown in the following sub-sections.

Get Hub Information

The following GET_HUB_INFO SETUP packet must be sent to obtain the hub-related information (See Figure 2.). Refer to Table 3 for the USB SETUP command details.

TABLE 3: USB SETUP COMMAND: GET HUB INFORMATION

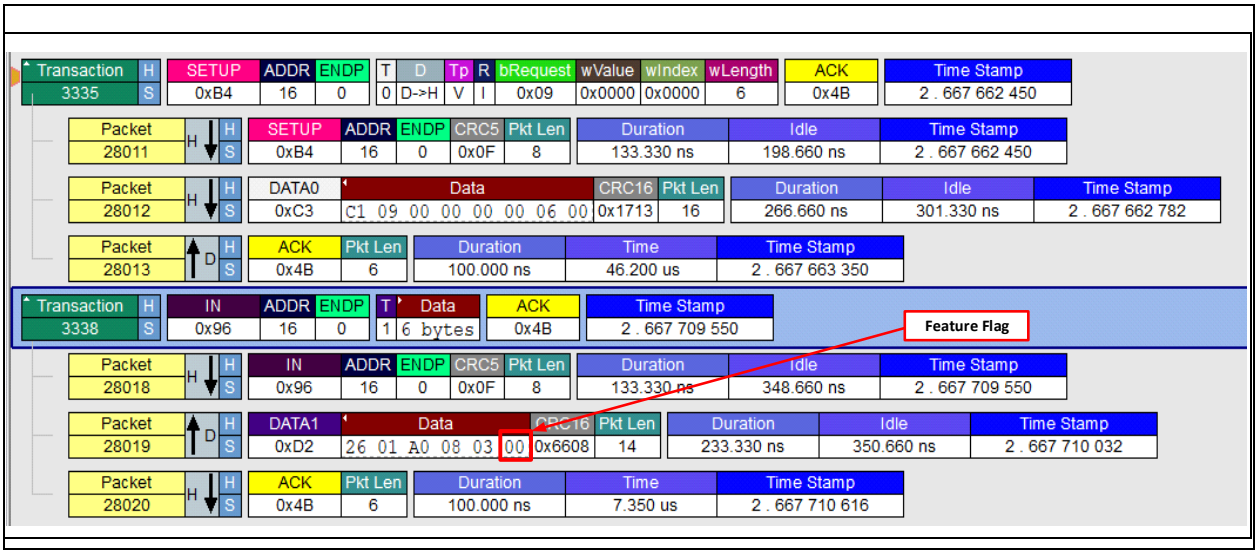
SETUP Packet	Value	Description
bmRequestType	0xC0	Host-to-device data transfer with a vendor-specific command that targets the device
bRequest	0x09	GET_HUB_INFO command
wValue	0x0000	Reserved
wIndex	0x0000	Reserved
wLength	0x0006	Size of the HUB_INFO structure

The hub responds with a Hub Information Structure (HUB_INFO) during the DATA phase (See Figure 2.). The details on the hub information structure (DATA phase) are in Table 4.

TABLE 4: HUB INFORMATION STRUCTURE (DATA PHASE)

Offset	Size	Field	Description
0x00	2	FW Revision	Firmware revision
0x02	1	Device Revision	Silicon mask revision 0xA0, 0xB0
0x03	2	ASIC Type	This is a byte coded field which means: MSB: 0x03 – HFC responds to this command LSB: 0x08 – Device belongs to USB72xx product family
0x05	1	Feature Flag	Bit 0: Current code execution area; 0: ROM, 1: SPI

FIGURE 2: GET_HUB_INFO (SETUP AND DATA PHASE)



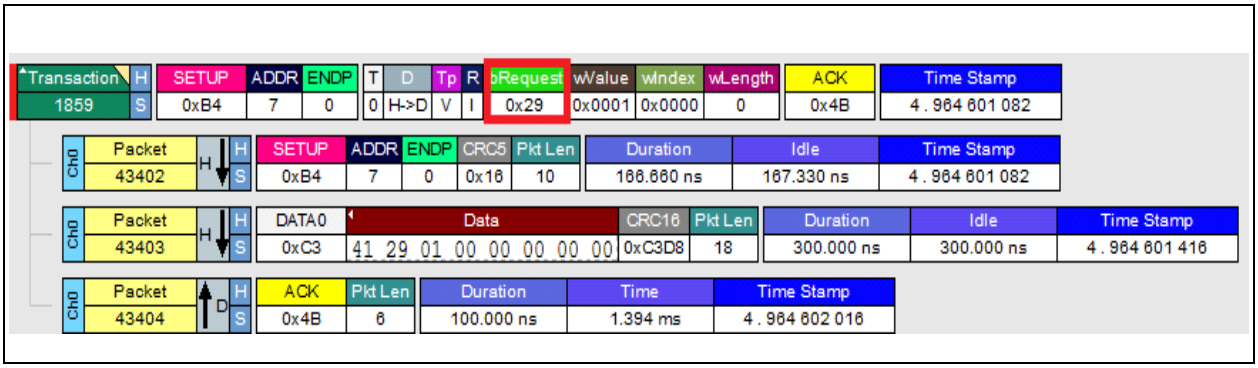
Reset the Hub

The hub can be soft reset externally from the host by issuing the CMD_DEV_RESET command. This command does not have a DATA phase (See Figure 3.). The existing device handle becomes invalid when the hub is reset. The host must acquire a new device handle by reopening the hub. Refer to Table 5 for the USB SETUP command information.

TABLE 5: USB SETUP COMMAND: RESETTING THE HUB

SETUP Packet	Value	Description
bmRequestType	0x41	Host-to-device data transfer with a vendor-specific command that targets the device
bRequest	0x29	CMD_DEV_RESET command
wValue	0x0001	Reserved
wIndex	0x0000	Reserved
wLength	0x0000	No DATA phase

FIGURE 3: RESETTING THE HUB (SETUP PHASE)



Force Boot from Internal ROM

If the hub is executing out of the external SPI ROM and the host must perform SPI pass-through operations on the SPI ROM, then the hub must be forced to execute from the internal ROM for the operations to succeed. This can be achieved with the following command sequence:

1. Write the disable the SPI (DSPI) signature to the XDATA memory location 0xBFD227EC (See Figure 4.). The hub checks for this signature during the boot sequence. Refer to Table 6 for the USB SETUP command.

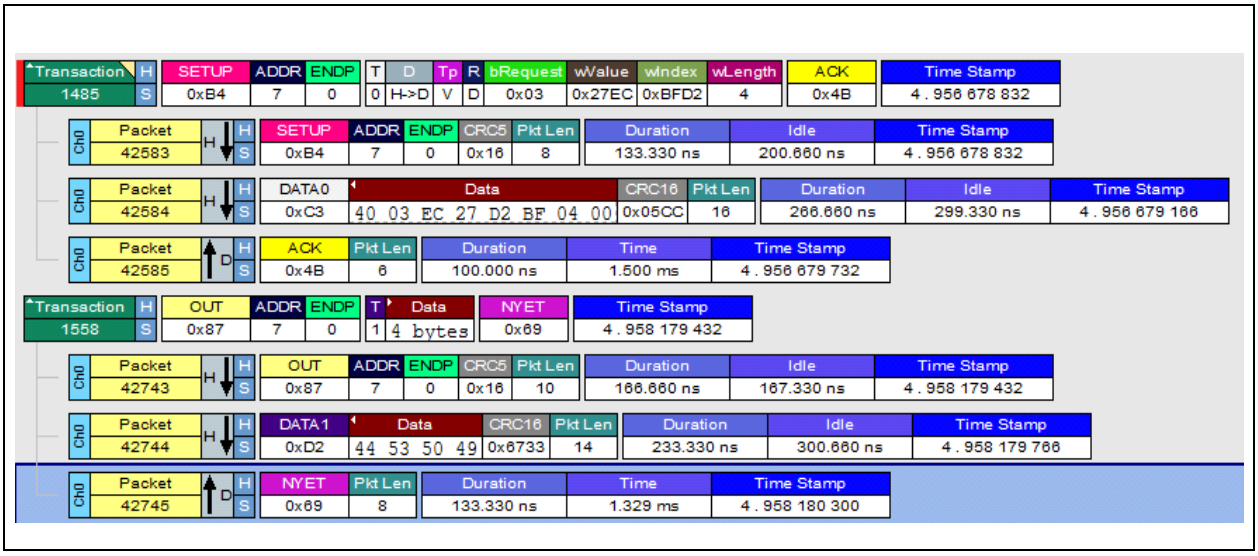
TABLE 6: USB SETUP COMMAND: WRITING DSPI SIGNATURE

SETUP Packet	Value	Description
bmRequestType	0x40	Vendor-specific command with host-to-device data transfer
bRequest	0x03	CMD_MEMORY_WRITE
wValue	0x27EC	ADDR_LO
wIndex	0xBFD2	ADDR_HI
wLength	0x0004	Number of data bytes to write

During the DATA phase of this transaction, the DSPI signature is sent to the hub.

EP0 OUT Data = 0x44, 0x53, 0x50, 0x49 (‘D’, ‘S’, 'P', ‘I’)

FIGURE 4: XDATA (0XBFD227EC) WRITE (SETUP AND DATA PHASE)



2. Set bit 3 of XDATA memory address 0xBFD1DA1C (See Figure 5.). See Table 7 for the USB SETUP command information.

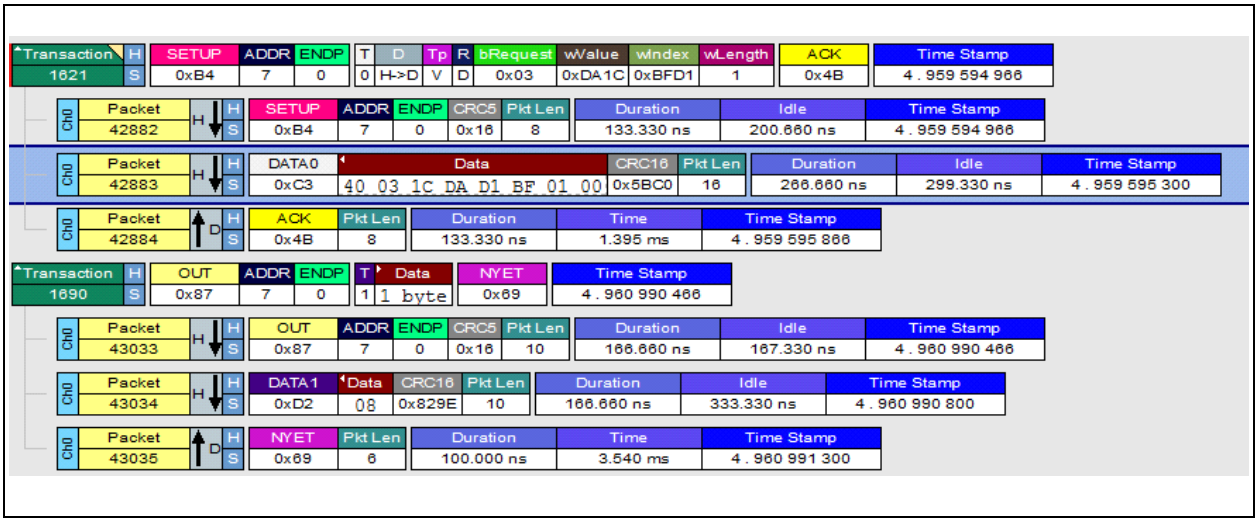
TABLE 7: USB SETUP COMMAND: SETTING BIT 3 AT 0XBFD1DA1C

SETUP Packet	Value	Description
bmRequestType	0x40	Vendor-specific command with host-to-device data transfer
bRequest	0x03	CMD_MEMORY_WRITE
wValue	0xDA1C	ADDR_LO
wIndex	0xBFD1	ADDR_HI
wLength	0x0001	Number of data bytes to write

During the DATA phase of this transaction, the signature 0x08 is sent to the hub (See Figure 5.).

EP0 OUT Data = 0x08

FIGURE 5: XDATA (0XBFD1DA1C) WRITE (SETUP AND DATA PHASE)



3. Reset the hub as specified in Reset the Hub on page 7.

Enable SPI Pass-Through Interface

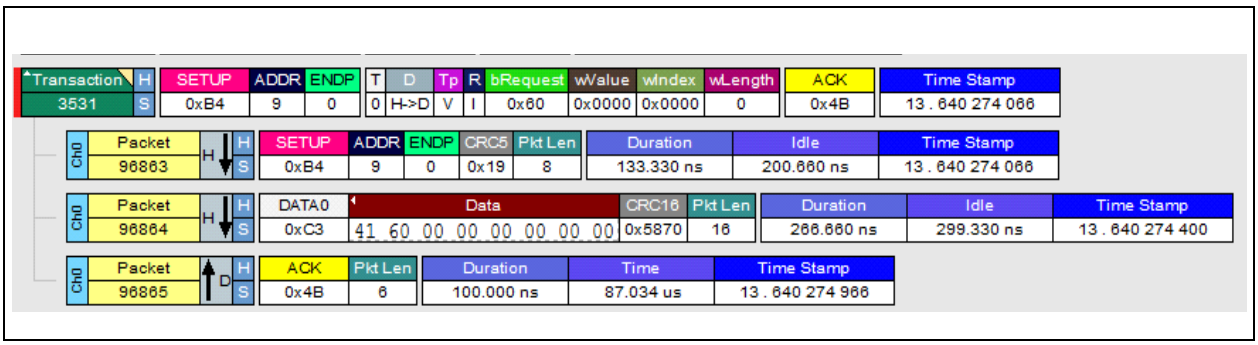
The following SETUP packet command is required to enable the SPI pass-through interface (See Figure 6.). The interface must be enabled before any read/write commands could be issued by the host.

Note: There is no DATA phase to this USB transaction. Refer to Table 8 for the USB SETUP command.

TABLE 8: USB SETUP COMMAND: ENABLING PASS-THROUGH INTERFACE

SETUP Packet	Value	Description
bmRequestType	0x41	Host-to-device data transfer with a vendor-specific command that targets the device
bRequest	0x60	CMD_SPI_ENTER_PASSTHRU
wValue	0x0000	Reserved
wIndex	0x0000	Reserved
wLength	0x0000	No DATA phase

FIGURE 6: ENABLE SPI PASS-THROUGH INTERFACE (SETUP PHASE)



Disable SPI Pass-Through Interface

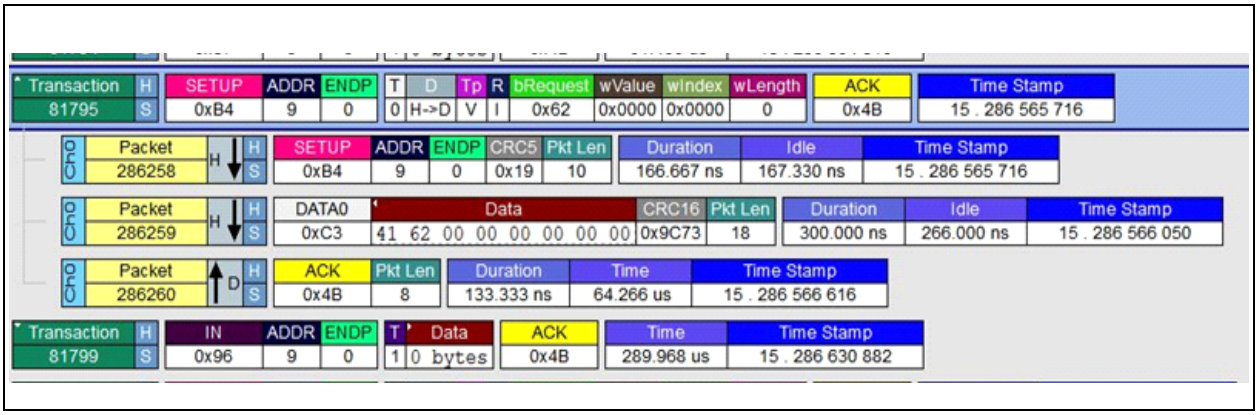
The following SETUP packet command is required to disable the SPI pass-through interface (See Figure 7.).

Note: There is no DATA phase to this USB transaction. Refer to Table 9 for the USB SETUP command.

TABLE 9: USB SETUP COMMAND: DISABLING SPI PASS-THROUGH INTERFACE

SETUP Packet	Value	Description
bmRequestType	0x41	Host-to-device data transfer with a vendor-specific command that targets the device
bRequest	0x62	CMD_SPI_EXIT_PASSTHRU
wValue	0x0000	Reserved
wIndex	0x0000	Reserved
wLength	0x0000	No DATA phase

FIGURE 7: DISABLE SPI PASS-THROUGH INTERFACE (SETUP PHASE)



SPI Pass-Through Read/Write

The SPI pass-through read/write command sequence consists of the following phases:

CMD_SPI_ACCESS PHASE

Note:	Prior to initiating this phase, ensure that bit 13 of the XDATA memory address 0xBFD23408 is set. For more details on this, refer to *AN2935 Configuration of the USB7202/USB7206/USB725x Application Note.*

The host sends the following SETUP packet command during the CMD_SPI_ACCESS phase. The non-zero wIndex in this case holds configurable fields that instruct the hub firmware to poll any Status bits (like Busy bits in case of an SPI Flash) during an SPI read/write access. Refer to Table 10 for the USB SETUP command.

TABLE 10: USB SETUP COMMAND: CMD_SPI_ACCESS

SETUP Packet	Value	Description
bmRequestType	0x41	Host-to-device data transfer with a vendor-specific command that targets the device
bRequest	0x61	CMD_SPI_PASS_THRU_WRITE
wValue	0xNNNN	Total length is the total number of data bytes to be sent to the SPI peripheral during the DATA phase that follows this SETUP packet. Total length = Signature length + Configurable field number + Command length + Response length (“SPID” Signature (4 bytes) + Configurable fields (4 bytes) + Number of bytes to transmit in the Command buffer + Number of bytes to receive in Response buffer)
wIndex	0xNN00	This value holds the number of configurable fields required for polling the Status bit. NN is the number of configurable fields. The configurable parameters are: • Status (Busy) bit location to Poll • Opcode for Status Read • Number of dummy bytes in the response • Index of the Response buffer to fetch the Status register value being polled Here NN is 04.
wLength	N	Number of bytes the SPI interface will transmit in the following data stage: wLength = Total length – Response length

DATA PHASE

During this phase, the host sends an OUT DATA packet to the SPI peripheral. This packet is formatted as follows:

EP0 DATA =

- Index 0: S (0x53)
- Index 1: P (0x50)
- Index 2: I (0x49)
- Index 3: D (0x44)
- Index 4: Busy bit (0x01)
- Index 5: Read Status opcode
- Index 6: Number of dummy bytes in response
- Index 7: Index of the Response buffer to fetch the Status register value being polled
- Index 8 to Index n: Command buffer data (command byte, address byte, dummy bytes, and up to 256 data bytes)

RETRIEVING THE DATA (APPLIES TO BLOCK READ ONLY)

These additional SETUP and DATA phases are applicable only in case of SPI Block Reads. During the previous DATA phase (See Data Phase on page 11.), based on the opcode, the hub retrieves the requested number of data bytes from the SPI peripheral and stores it internally in a register at location 0xBFD22310.

During this phase, the hub first sends the following SETUP packet to read the hub's internal register that contains the requested data. See Table 11 for the USB SETUP command.

TABLE 11: USB SETUP COMMAND: SPI BLOCK READ

SETUP Packet	Value	Description
bmRequestType	0xC0	Vendor-specific command with device-to-host to data transfer
bRequest	0x04	CMD_MEMORY_READ
wValue	0x2310	ADDR_LO
wIndex	0xBFD2	ADDR_HI
wLength	0xNNNN	Number of data bytes to be retrieved

This is followed by a DATA phase where the hub responds to the host with an IN packet containing the requested number of bytes retrieved from the SPI peripheral.

Single-Byte Instruction Write Example

Figure 8 shows an example where a single-byte instruction (WREN) is written to enable the write latch in case of a SST26VF016B SPI Flash memory. Refer to Table 12 for the USB SETUP command information.

TABLE 12: USB SETUP COMMAND: SPI SINGLE-BYTE WRITE

SETUP Packet	Value	Description
bmRequestType	0x41	Host-to-device data transfer with a vendor-specific command that targets the device
bRequest	0x61	CMD_SPI_PASS_THRU_WRITE
wValue	0x0009	Total length = Signature length (4 bytes) + Configurable field number (4 bytes) + Command length (1 byte) + Response length (0 byte)
wIndex	0x0400	Number of configurable fields for polling status The configurable parameters are: • Busy bit location to Poll (0x01) • RDSR opcode (0x05) • Number of dummy bytes in the response (0x00) • Index of the Response buffer to fetch the Status register value that was returned (0x01)
wLength	0x0009	Number of bytes the SPI interface will transmit in the following data stage: wLength = Total length – Response length wLength = 9 – 0 = 9 bytes

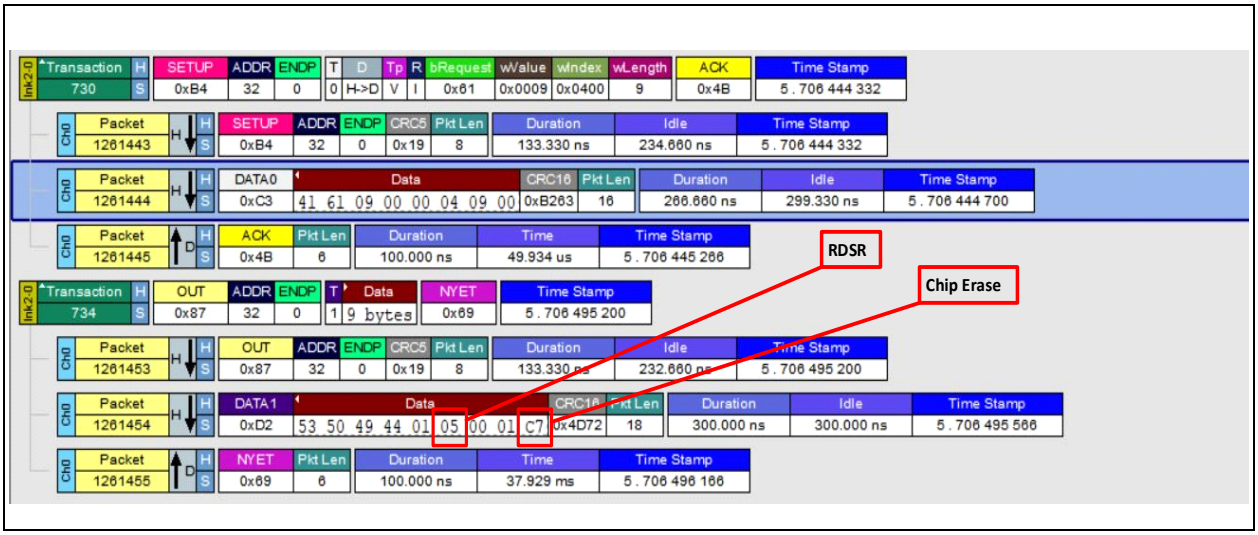
0x05 is the Read Status register (RDSR) instruction, and 0xC7 is the Chip Erase instruction for SST26VF016B.

During the DATA phase of this command sequence, the host sends an OUT packet containing nine bytes to the SPI Flash as shown in Figure 8.

EP0 OUT Data =

- Index 0: S (0x53)
- Index 1: P (0x50)
- Index 2: I (0x49)
- Index 3: D (0x44)
- Index 4: Busy Bit (0x01)
- Index 5: Read Status opcode (RDSR:0x05)
- Index 6: Number of dummy bytes in response (0x00)
- Index 7: Index of the Response buffer to fetch the read status byte (0x01)
- Index 8 to Index 9: Command buffer data [Command byte: Chip Erase (0xC7)]

FIGURE 8: SINGLE-BYTE SPI WRITE (SETUP AND DATA PHASE)



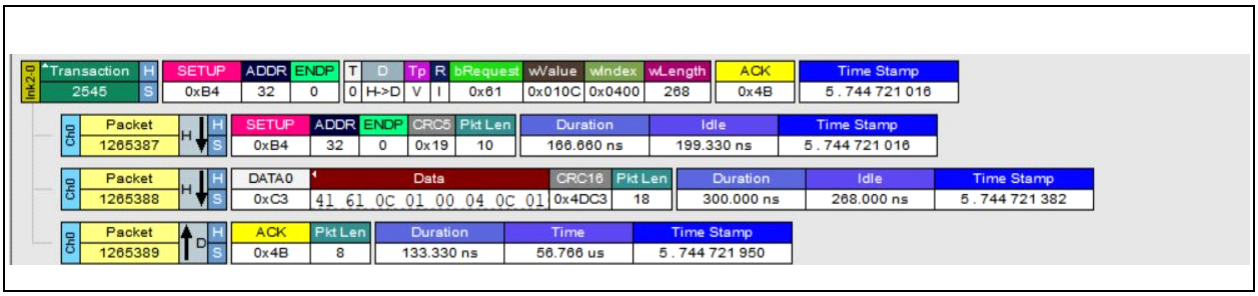
SPI Block Write Example

The SPI pass-through interface allows the host to perform a block write of up to 256 bytes. Figure 9 shows the SETUP packet for performing a block write to a SST26VF016B SPI Flash memory. See Table 13 for the USB SETUP command details.

TABLE 13: USB SETUP COMMAND: SPI BLOCK WRITE

SETUP Packet	Value	Description
bmRequestType	0x41	Host-to-device data transfer with a vendor-specific command that targets the device
bRequest	0x61	CMD_SPI_PASS_THRU_WRITE
wValue	0x010C	Total length = Signature length (4 bytes) + Configurable field number (4 bytes) + Command length (1-byte opcode + 3 bytes of address + 256 data bytes) + Response length (0 byte)
wIndex	0x0400	Number of configurable fields for polling status. The configurable parameters are: • Busy bit location to Poll (0x01) • RDSR opcode (0x05) • Number of dummy bytes in the response (0x00) • Index of the Response buffer to fetch the Status register value that was returned (0x01)
wLength	0x010C	Number of bytes the SPI interface will transmit in the following data stage: wLength = Total length – Response length wLength = 268 – 0 = 268 bytes (0x010C)

FIGURE 9: SPI BLOCK WRITE (SETUP PHASE)



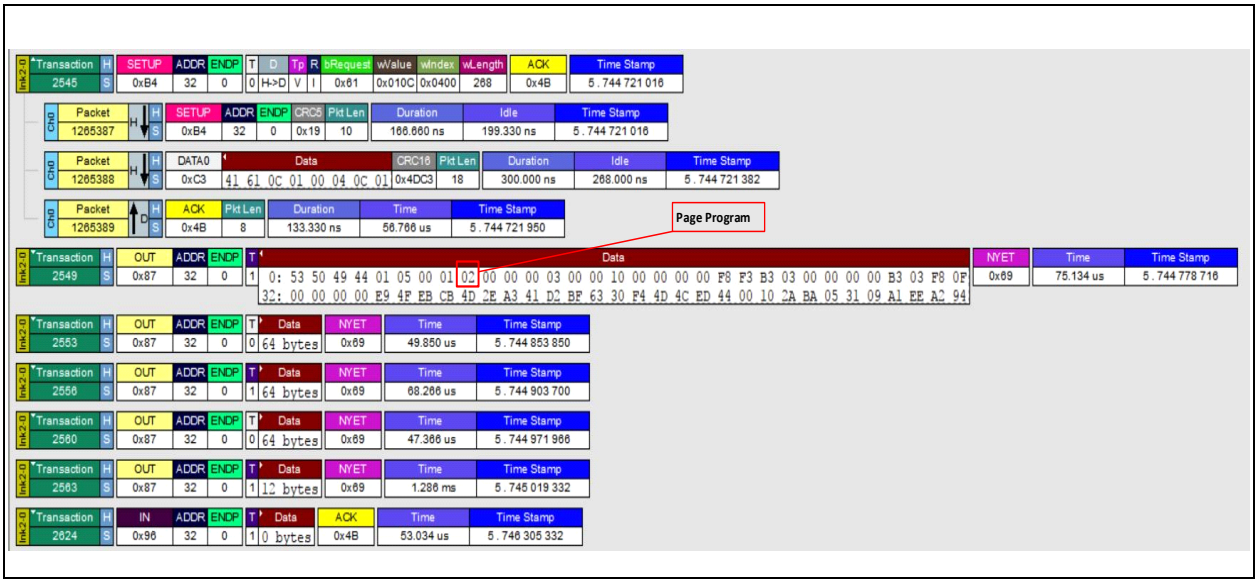
During the DATA phase (See Figure 10.) of this command sequence, 268 bytes are transferred to the SPI Flash via the hub's pass-through interface. The DATA packet consists of the following:

EP0 OUT Data =

- Index 0: S (0x53)
- Index 1: P (0x50)
- Index 2: I (0x49)
- Index 3: D (0x44)
- Index 4: Busy bit (0x01)
- Index 5: Read Status opcode (RDSR:0x05)
- Index 6: Number of dummy bytes in response (0x00)
- Index 7: Index of the Response buffer to fetch the read status byte (0x01)
- Index 8 to Index 267: Command buffer data [Command byte: PAGE PROGRAM (0x02), address byte (0x00, 0x00, 0x00), dummy byte (none), and up to 256 data bytes]

In this case, PAGE PROGRAM (0x02) instruction is specific to SST26VF016B.

FIGURE 10: SPI BLOCK WRITE (DATA PHASE)



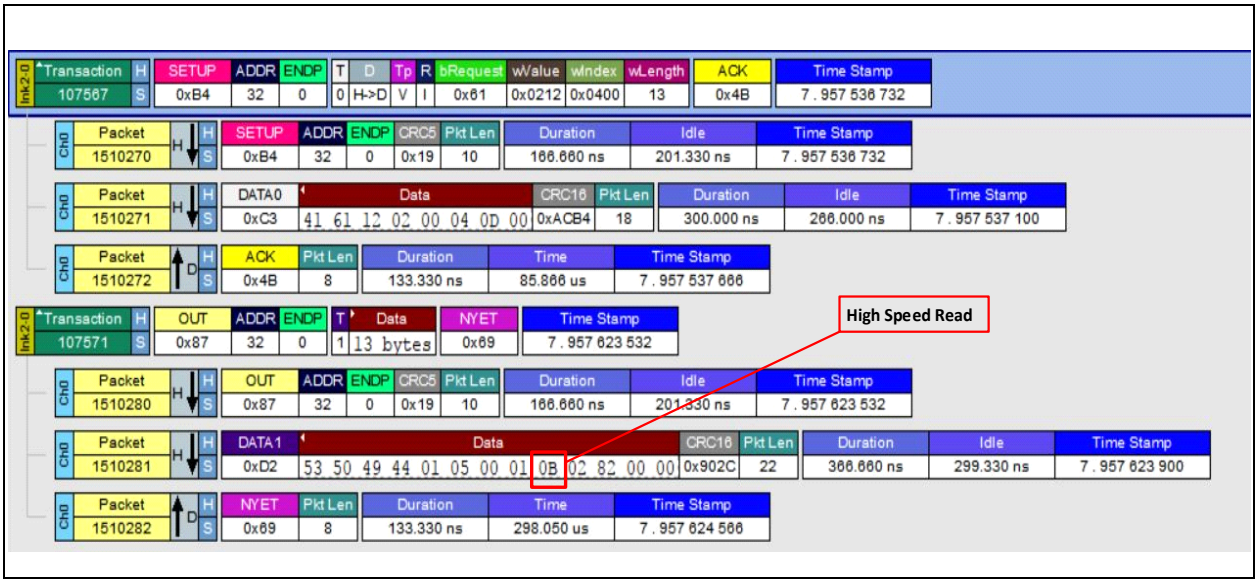
SPI Block Read Example

The SPI pass-through interface allows the host to perform a block read of up to 512 bytes. Figure 11 shows the SETUP packet for this transaction in case of a SST26VF016B SPI Flash memory. See Table 14 for the USB SETUP command information.

TABLE 14: USB SETUP COMMAND: SPI BLOCK READ

SETUP Packet	Value	Description
bmRequestType	0x41	Host-to-device data transfer with a vendor-specific command that targets the device
bRequest	0x61	CMD_SPI_PASS_THRU_WRITE
wValue	0x0212	Total length = Signature length (4 bytes) + Configurable field number (4 bytes) + Command length (1-byte opcode + 3 bytes of address +1 dummy byte) + Response length (512 data bytes) + 5 bytes (first five bytes to be ignored)
wIndex	0x0400	Number of configurable fields for polling status. The configurable parameters are: • Busy bit location to Poll (0x01) • RDSR opcode (0x05) • Number of dummy bytes in the response (0x00) • Index of the Response buffer to fetch the Status register value that was returned (0x01)
wLength	0x000D	Number of bytes the SPI interface will transmit in the following data stage: wLength = Total length – Response length wLength = 530 – 517 = 13 bytes (0x000D)

FIGURE 11: SPI BLOCK READ (SETUP PHASE 1 AND DATA PHASE 1)



During the DATA phase (See Figure 11.), 13 bytes are transferred to the hub. The DATA packet consists of the following:

EP0 OUT Data =

- Index 0: S (0x53)
- Index 1: P (0x50)
- Index 2: I (0x49)

- Index 3: D (0x44)
- Index 4: Busy bit (0x01)
- Index 5: Read Status opcode (RDSR: 0x05)
- Index 6: Number of dummy bytes in response (0x00)
- Index 7: Index of the Response buffer to fetch the read status byte (0x01)
- Index 8 to Index 12: Command buffer data [Command byte: HIGH SPEED READ (0x0B), address byte (0x02, 0x82, 0x00), dummy byte (0x00)]

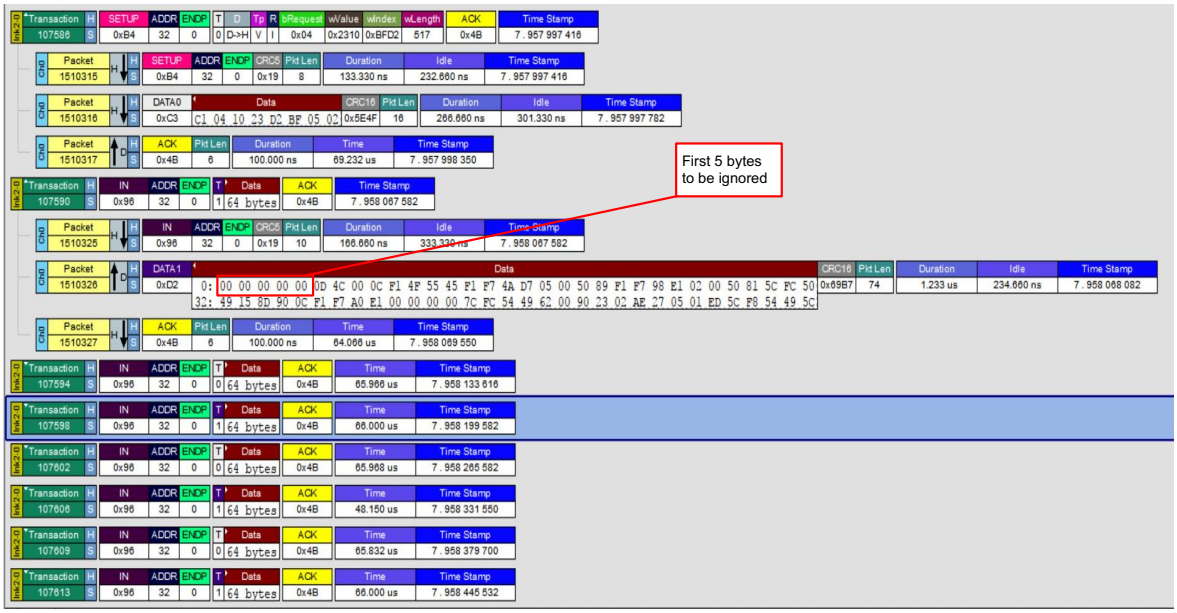
In this case, HIGH-SPEED READ (0x0B) instruction is specific to SST26VF016B.

The host then initiates the second SETUP phase by sending a SETUP packet for reading the hub's internal register at 0xBFD22310 containing the data bytes to be read. Figure 12 shows this SETUP packet. Refer to Table 15 for the USB SETUP command details.

TABLE 15: USB SETUP COMMAND: SPI BLOCK READ

SETUP Packet	Value	Description
bmRequestType	0xC0	Vendor-specific command with device-to-host-to-data transfer
bRequest	0x04	CMD_MEMORY_READ
wValue	0x2310	ADDR_LO
wIndex	0xBFD2	ADDR_HI
wLength	0x0205	Number of data bytes to be retrieved (517 bytes). The first five bytes of any SPI read must be ignored. Therefore, five must be added to the number of bytes to be read.

FIGURE 12: SPI BLOCK READ (SETUP PHASE 2 AND DATA PHASE 2)



During the DATA phase that follows this, the hub responds with IN packets (See Figure 12.) containing a total of 517 bytes retrieved from the SPI Flash via the pass-through interface. The first five bytes would return during the DATA phase are 0s, and they need to be ignored.

APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00003020A (05-14-19)	Initial release	

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ISBN: 978-1-5224-4505-0

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