Report
Gigabit Ethernet PHY Device Latency

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.2

Revision 1.2 was published in January 2010. SyncE discussion was updated.

1.2 Revision 1.1

Revision 1.1 was published in November 2009. Latency variability real world discussion was updated.

1.3 Revision 1.0

Revision 1.0 was the first release of this document. It was published in November 2009.

2 Introduction

The following markets have emerged recently within the Ethernet industry where performance is greatly affected by latency.

- Industrial Ethernet using IEEE-1588v1
- Carrier Ethernet using timing over packet (IEEE-1588v2 2008)
- Audio/ video bridging currently being defined by IEEE 802.1

As a result, systems architects as well as hardware and software designers now have to both consider and account for latency within their data interfaces.

Since Ethernet PHYs (both copper and fiber) are provisioned throughout the data interfaces of these applications, their latency needs to be considered as the systems in which they reside are designed. The following is a report of the latency introduced by the Vitesse Gigabit Ethernet PHY product line for different interfaces and across all supported speeds.

3 How Latency Values Were Obtained

This section describes how the latency values were obtained.

3.1 How Was Timing Done

The latency values in the following tables were obtained from simulations performed on each PHY's computer design model. In each case, the PHY was configured in a default mode and FIFOs were in default settings. Valid PPM variations were taken into account for the simulations.

3.2 What were the Start and Stop Points for Timing

The latency values below were measured from the start of packet arriving at the ingress and egress interface. For example, on the VSC8664 SGMII to 1000BT (CAT5) path the start of packet is measured from the point when the start of frame is detected at the SGMII interface from the MAC to the start of frame arriving at the outgoing CAT5 pins to the media partner.

4 How Much Would These Times Vary in the “Real World”

The basic function of the PHY can be thought of receiving data on one side in one format and converting the data to a different format and sending it out the other side. Extending the basic function is the understanding that each side of the PHY in addition to the difference in data format also operates on a different clock. Clock domains are connected by a FIFO. FIFOs have an inherent phase uncertainty. This uncertainty can cause a potential packet variation between the minimum and maximum latency. This design point is a result of the IEEE 802.3 specification.

Specifically the accuracy of the simulation numbers is expected to be within ± 8 bit times in the real world for SGMII and 1000 Mbps RGMII. Accuracy will be ±4 bit times for RGMII and MII 10/100 into the PHY from the MAC.

In the following tables the range minimum and maximum values will not be seen in a particular device because the device PPM will be fixed by the components and current operating conditions.

Note: A “bit time” is the time duration of a 0 or 1 being transmitted. For 1000/100/10BT the bit times are 1/10/100 ns.

4.1 SyncE Application

To improve the synchronization between sides of the PHY and a system the media source clock can be distributed using VSC8664 recovered clock support to provide SyncE support per the ITU-T G.8261/Y. 1361 specification. The recovered clock will be used by both sides of the PHY improving clock but not phase differences in clock domains. Given that temperature, process and other variations are constant these variations are further removed.

5 PHY End-to-End Latency

This section describes the PHY end-to-end latency.

5.1 VSC8664/VSC8634/VSC8538/VSC8558/VSC8658

The following table lists the SGMII/SERDES to 10/100/1000BASE-T transmit latency.

Table 1 • SGMII/SERDES to 10/100/1000BASE-T Transmit Latency

Speed (Mbps)	Minimum (ns)	Maximum (ns)
1000	120	132
100	220	280
10	1500	2100

The following table lists the 10/100/1000BASE-T to SGMII/SERDES receive latency.

Table 2 • 10/100/1000BASE-T to SGMII/SERDES Receive Latency

Speed (Mbps)	Minimum (ns)	Maximum (ns)
1000	260	292
100	370	460
10	2800	3900

The following table lists the SGMII to 1000BASE-X transmit latency.

Table 3 • SGMII/SERDES to 10/100/1000BASE-T Transmit Latency

Speed (Mbps)	Minimum (ns)	Maximum (ns)
1000	140	150

The following table lists the 1000BASE-X to SGMII receive latency.

Table 4 • 1000BASE-X to SGMII Receive Latency

Speed (Mbps)	Minimum (ns)	Maximum (ns)
1000	140	150

5.2 VSC8601/VSC8641

The following table lists the RGMII to 10/100/1000BASE-T transmit latency.

Table 5 • RGMII to 10/100/1000BASE-T Transmit Latency

Speed (Mbps	Minimum (ns)	Maximum (ns)
1000	80	84
100	170	200
10	1400	1500

The following table lists 10/100/1000BASE-T to RGMII receive latency.

Table 6 • 10/100/1000BASE-T to RGMII Receive Latency

Speed (Mbps)	Minimum (ns)	Maximum (ns)
1000	224	244
100	320	380
10	3100	3500

The following table lists the GMII to 10/100/1000BASE-T transmit latency.

Table 7 • GMII to 10/100/1000BASE-T Transmit Latency

Speed (Mbps)	Minimum (ns)	Maximum (ns)
1000	80	84
100	110	140
10	1000	1400

The following table lists the 10/100/1000BASE-T to GMII receive latency.

Table 8 • 10/100/1000BASE-T to GMII Receive Latency

Speed (Mbps)	Minimum (ns)	Maximum (ns)
1000	224	244
100	248	320
10	2100	3200

5.3 VSC8224/VSC8234/VSC8244

The following table lists the RGMII to 10/100/1000BASE-T transmit latency.

Table 9 • RGMII to 10/100/1000BASE-T Transmit Latency

Speed (Mbps)	Minimum (ns)	Maximum (ns)
1000	80	84
100	170	200
10	1400	1700

The following table lists the SERDES to RGMII receive latency

Table 10 • SERDES to RGMII Receive Latency

Speed (Mbps)	Minimum (ns)	Maximum (ns)
1000	75	75

The following table lists the 10/100/1000BASE-T to RGMII receive latency.

Table 11 • 10/100/1000BASE-T to RGMII Receive Latency

Speed (Mbps)	Minimum (ns)	Maximum (ns)
1000	224	244
100	320	380

Speed (Mbps)	Minimum (ns)	Maximum (ns)
10	3100	3500

The following table lists the RGMII to SERDES transmit latency.

Table 12 • RGMII to SERDES Transmit Latency

Speed (Mbps)	Minimum (ns)	Maximum (ns)
1000	75	75

The following table lists the SGMII/SERDES to 10/100/1000BASE-T transmit latency.

Table 13 • SGMII/SERDES to 10/100/1000BASE-T Transmit Latency

Speed (Mbps)	Minimum (ns)	Maximum (ns)
1000	114	132
100	220	280
10	1500	2100

The following table lists the 10/100/1000BASE-T to SGMII/SERDES receive latency.

Table 14 • 10/100/1000BASE-T to SGMII/SERDES Receive Latency

Speed (Mbps)	Minimum (ns)	Maximum (ns)
1000	252	292
100	362	460
10	2800	3900

Microsemi Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

VPPD-02521