KSZ8863RLL

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for Microchip KSZ8863RLL. These checklist items should be followed when utilizing the KSZ8863RLL in a new design. A summary of these items is provided in Section 9.0, "Hardware Checklist Summary," on page 20. Detailed information on these subjects can be found in the corresponding section:

2.0 GENERAL CONSIDERATIONS

2.1 Required Reference

The KSZ8863RLL implementor should have the *KSZ8863RLL Data Sheet* on hand.

2.2 Pin Check

Check the pinout of the part against the data sheet. Ensure that all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.3 Ground

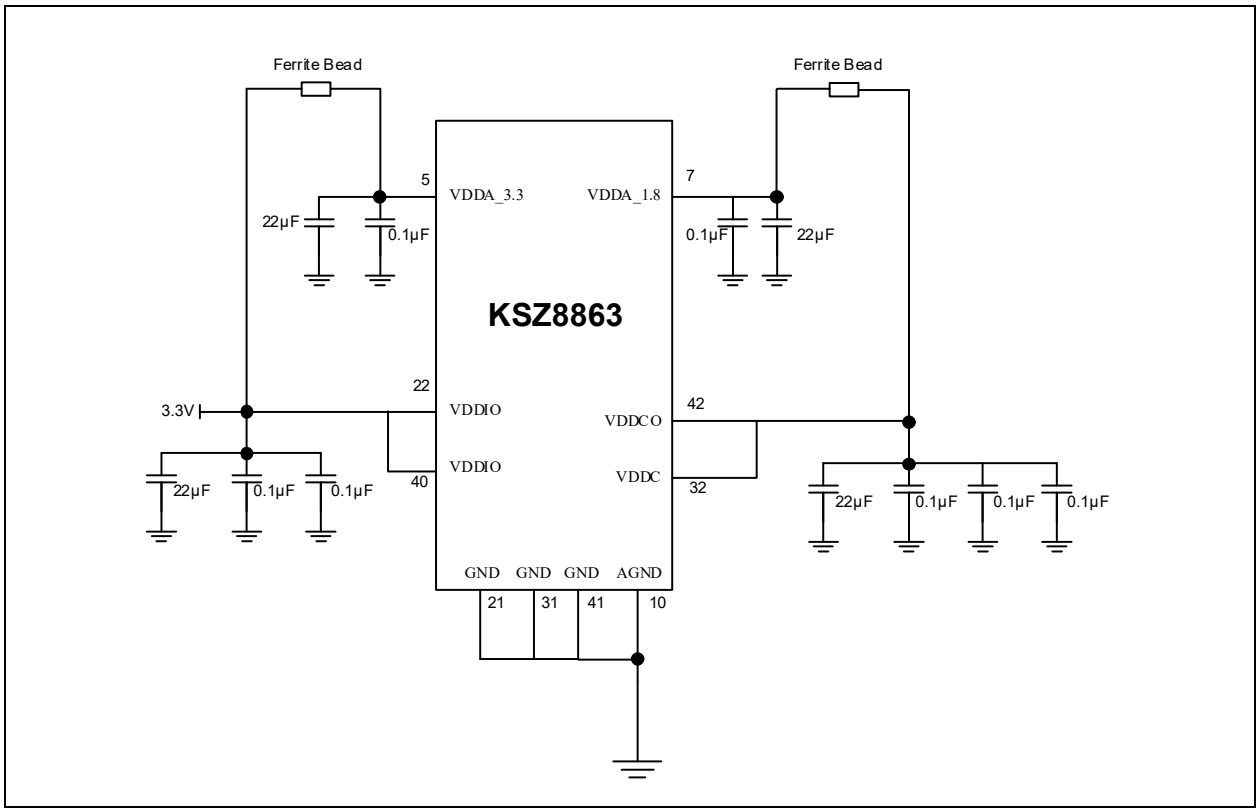
- The ground pins are pins 10, 21,31, and 41 (**GND**), and they should be connected to the solid ground plane on the board.
- It is recommended that all ground connections be tied together to the same ground plane. Separate ground planes are not recommended.

3.0 POWER

- Pin 5 of the KSZ8863RLL is the analog supply (**VDDA_3.3**). This supply should be isolated from the board 3.3V through a ferrite bead, with bulk capacitance on both sides of the bead.
- **VDDA_3.3** pin should have a 0.1 uF capacitor to decouple the device. The capacitor size should be SMD_0603 or smaller.
- Pins 40 and 22 (**VDDIO**) should be connected to the common board supply with the digital IO of the MAC/PHY mating to the digital interface, 1.8V to 3.3V.
- The KSZ8863RLL has an internal voltage regulator that outputs 1.8V on pin 42 (**VDDCO**). This is typically used instead of an external 1.8V supply to power **VDDA_1.8** and **VDDC**. When **VDDIO** = 1.8V, the internal regulator cannot provide 1.8V and an external 1.8V supply is required for **VDDA_1.8** and **VDDC**. Do not connect an external 1.8V supply to **VDDCO**.
- Pin 7 (**VDDA_1.8**) should be connected to **VDDCO** (pin 42) or the board 1.8V supply. This supply should be isolated by a ferrite bead and proper bulk capacitance.
- Pin 32 (**VDDC**) should be connected to Pin 42 (**VDDCO**) or the board 1.8V supply.

The power and ground connections are shown in Figure 3-1.

FIGURE 3-1: POWER AND GROUND CONNECTIONS



4.0 ETHERNET SIGNALS

4.1 PHY No. 1 Interface

- **TXP1** (pin 4): This pin is the transmit twisted pair output positive connection from the internal PHY. A 49.9Ω (1.0%) termination resistor with AC coupled to the digital ground through a 0.1 uF capacitor is required on this pin.
- **TXM1** (pin 3): This pin is the transmit twisted pair output negative connection from the internal PHY. A 49.9Ω (1.0%) termination resistor with AC coupled to the digital ground through a 0.1 uF capacitor is required on this pin.
- For transmit channel connection and termination details, refer to Figure 4-1.
- **RXP1** (pin 2): This pin is the receive twisted pair input positive connection to the internal PHY. A 49.9Ω (1.0%) termination resistor with AC coupled to the digital ground through a 0.1 uF capacitor is required on this pin.
- **RXM1** (pin 1): This pin is the receive twisted pair input negative connection to the internal PHY. A 49.9Ω (1.0%) termination resistor with AC coupled to the digital ground through a 0.1 uF capacitor is required on this pin.
- For receive channel connection and termination details, refer to Figure 4-2.

4.2 PHY No. 2 Interface

- **TXP2** (pin 12): This pin is the transmit twisted pair output positive connection from the internal PHY. A 49.9Ω (1.0%) termination resistor with AC coupled to the digital ground through a 0.1 uF capacitor is required on this pin.
- **TXM2** (pin 11): This pin is the transmit twisted pair output negative connection from the internal PHY. A 49.9Ω (1.0%) termination resistor with AC coupled to the digital ground through a 0.1 uF capacitor is required on this pin.
- For transmit channel connection and termination details, refer to Figure 4-1.
- **RXP2** (pin 9): This pin is the receive twisted pair input positive connection to the internal PHY. A 49.9Ω (1.0%) termination resistor with AC coupled to the digital ground through a 0.1 uF capacitor is required on this pin.
- **RXM2** (pin 8): This pin is the receive twisted pair input negative connection to the internal PHY. A 49.9Ω (1.0%) termination resistor with AC coupled to the digital ground through a 0.1 uF capacitor is required on this pin.
- For receive channel connection and termination details, refer to Figure 4-2.

FIGURE 4-1: TRANSMIT CHANNEL CONNECTIONS AND TERMINATIONS

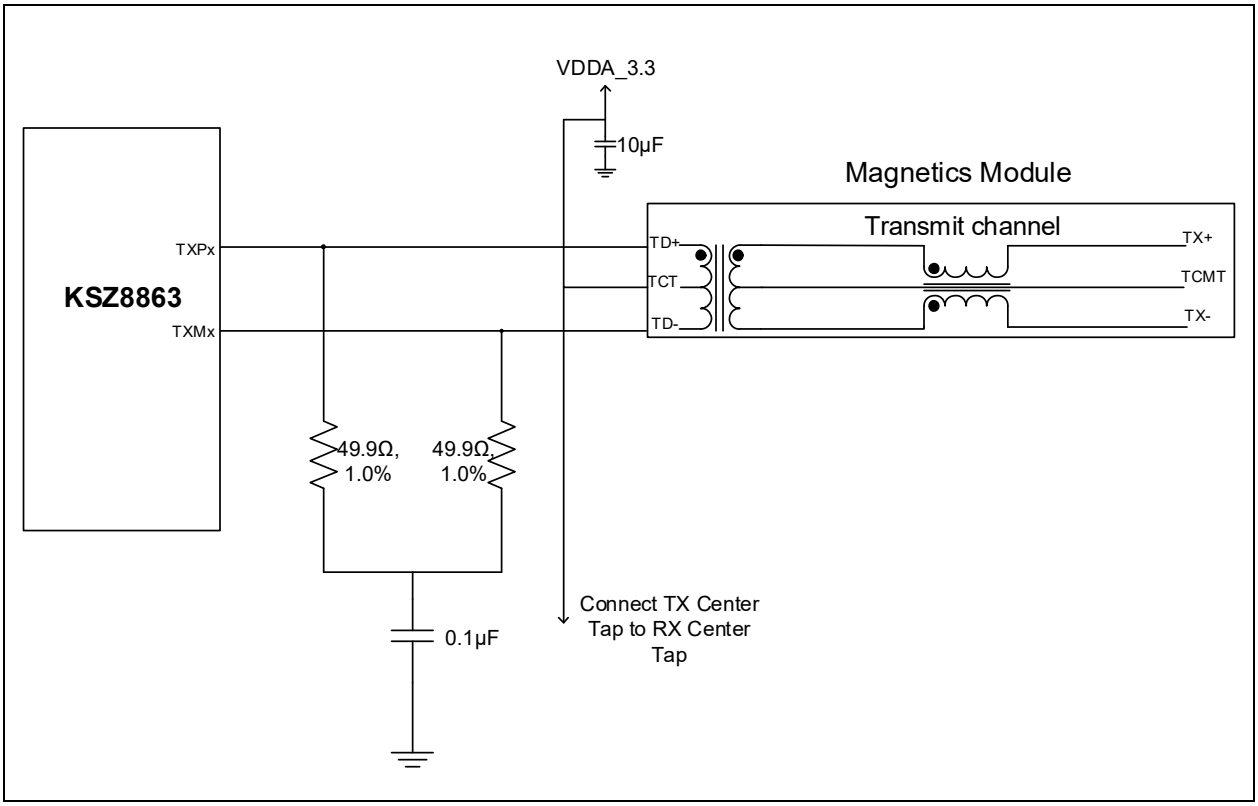
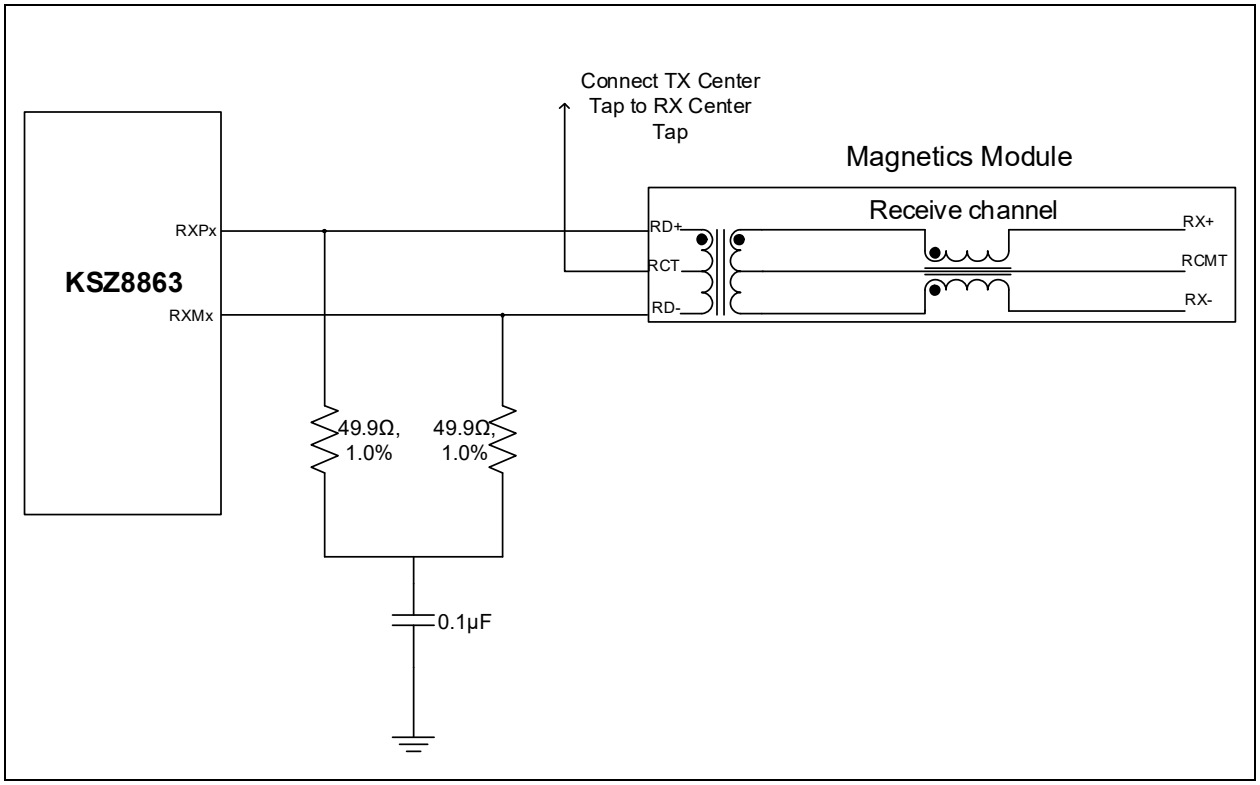


FIGURE 4-2: RECEIVE CHANNEL CONNECTIONS AND TERMINATIONS



4.3 Magnetics Connection

- The center tap connection on the KSZ8863RLL side for the transmit channel must be connected to 3.3V supply (created from +3.3V) directly. The transmit channel center tap of the magnetics also connects to the receive channel center tap of the magnetics. In addition, a 10 uF capacitor is required from the receive channel center tap of the magnetics to digital ground.
- The center tap connection on the cable side (RJ45 side) for the transmit channel should be terminated with a 75Ω resistor through a 1000 pF, 2 KV capacitor to chassis ground.
- The center tap connection on the cable side (RJ45 side) for the receive channel should be terminated with a 75Ω resistor through a 1000 pF, 2 KV capacitor to chassis ground.
- Only one 1000 pF, 2 KV capacitor to chassis ground is required. It is shared by both TX and RX center taps.
- Assuming the design of an end-point device (NIC), pin 1 of the RJ45 is **TX**+ and should trace through the magnetics to **TX**+ (pin 7) of the KSZ8863RLL.
- Assuming the design of an end-point device (NIC), pin 2 of the RJ45 is **TX**– and should trace through the magnetics to **TX**– (pin 6) of the KSZ8863RLL.
- Assuming the design of an end-point device (NIC), pin 3 of the RJ45 is **RX**+ and should trace through the magnetics to **RX**+ (pin 5) of the KSZ8863RLL.
- Assuming the design of an end-point device (NIC), pin 6 of the RJ45 is **RX**– and should trace through the magnetics to **RX**– (pin 4) of the KSZ8863RLL.

4.4 RJ45 Connector

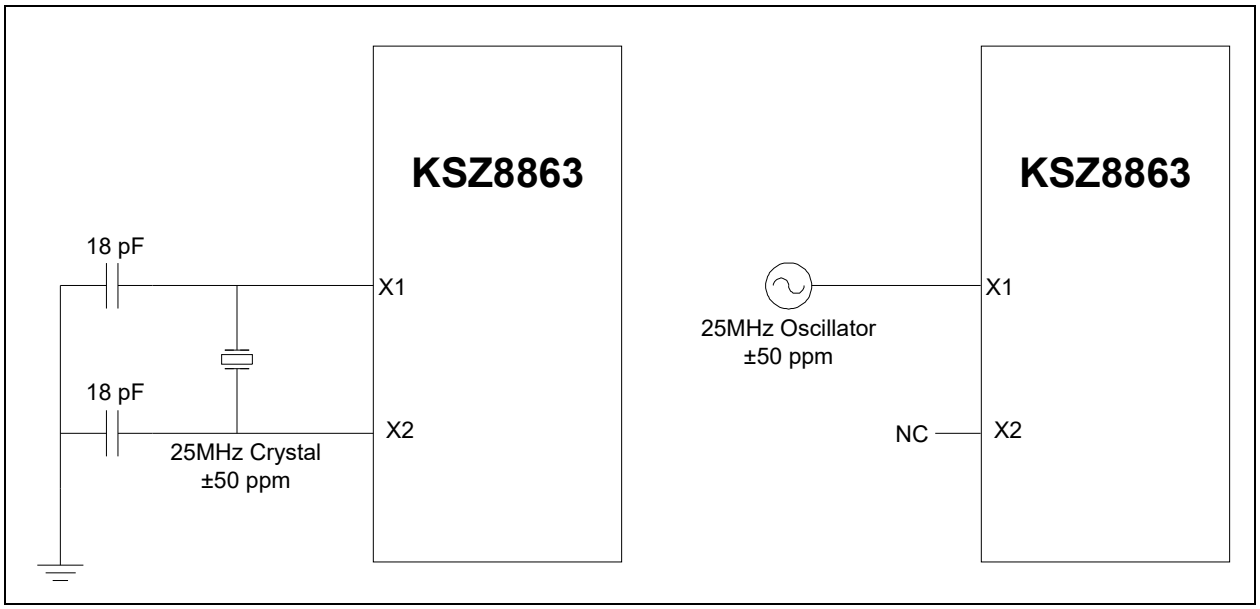
- Pins 4 and 5 of the RJ45 connector interface to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 pF, 2 KV capacitor. There are two methods for accomplishing this:
  - Pins 4 and 5 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω to the 1000 pF, 2 KV capacitor.
  - For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel perform like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω resistor causes the entire circuit to function as a 75Ω resistor. Therefore, by shorting pins 4 and 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 pF, 2 KV capacitor to chassis ground, an equivalent circuit is created.
- Pins 7 and 8 of the RJ45 connector interface to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 pF, 2 KV capacitor. There are two methods for accomplishing this:
  - Pin 7 and 8 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω to the 1000 pF, 2 KV capacitor.
  - For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel perform like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω resistor causes the entire circuit to function as a 75Ω resistor. Therefore, by shorting pins 7 and 8 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 pF, 2 KV capacitor to chassis ground, an equivalent circuit is created.
- The RJ45 shield should be attached directly to chassis ground.

5.0 CLOCK CIRCUIT

5.1 Crystal and External Oscillator/Clock Connections for RMII Mode

- A 25.000 MHz (±50 ppm) crystal should be used to provide the clock source. (See Figure 5-1.) For exact specifications and tolerances, refer to the latest revision of the *KSZ8863RLL Data Sheet*.
- **X1** (pin 14) is the clock circuit input for the KSZ8863RLL device. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- **X2** (pin 15) is the clock circuit output for the KSZ8863RLL device. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- Since every system design is unique, the capacitor values are system dependent, based on the C_L specification of the crystal and the stray capacitance value. The PCB design, crystal, and layout all contribute to the characteristics of this circuit.
- An external single-ended clock of 25 MHz or 50 MHz can also be used to supply the clock to the KSZ8863RLL. Connect the 3.3V external oscillator or clock to the **X1** (pin 14). Also, refer to Table 3-5 of the *KSZ8863RLL Data Sheet* to properly configure the KSZ8863RLL to accept the appropriate frequency.

FIGURE 5-1: CRYSTAL AND OSCILLATOR CONNECTIONS FOR RMII MODE



6.0 DIGITAL INTERFACE

6.1 RMII Interface

The Reduced Media Independent Interface (RMII) provided by the KSZ8863RLL is connected to the device's third MAC3. It complies with the RMII Specification. The RMII specifies a low pin count Media Independent Interface (MII). Table 6-1 describes the signals used by the RMII bus.

TABLE 6-1: RMII CONNECTIONS

KSZ8863RLL PHY-MAC Connections		Pin Descriptions	KSZ8863RLL MAC-MAC Connections	
External PHY Signals	**KSZ8863RLL MAC Signals**		**KSZ8863RLL MAC Signals**	**External MAC Signals**
REF_CLK	REFCLKI_3	Reference Clock	REFCLKI_3	REF_CLK
TX_EN	SMRXDV3	Carrier sense/ Receive data valid	SMRXDV3	CRS_DV
TXD1	SMRXD31	Receive data bit 1	SMRXD31	RXD1
TXD0	SMRXD30	Receive data bit 0	SMRXD30	RXD0
CRS_DV	SMTXEN3	Transmit enable0	SMTXEN3	TX_EN
RXD1	SMTXD31	Transmit data bit 1	SMTXD31	TXD1
RXD0	SMTXD30	Transmit data bit 0	SMTXD30	TXD0
RX_ER	SMTXER3	Receive error	(not used)	(not used)

RMII provides a common interface between two devices with RMII interface and has the following key characteristics:

- Sets 10 Mbps and 100 Mbps data rates for KSZ8863RLL RMII through register 0x06 bit 4. The default is 100 Mbps.
- Uses a single 50 MHz RMII reference clock (provided internally as RMII Clock mode or provided externally as RMII Normal mode).
- Provides independent 2-bit wide (di-bit) transmit and receive data paths.
- Contains two distinct groups of signals: one for transmission and the other for reception.
- SMRXD32, SMRXD33, SMTXD32, and SMRXD33 should be strapped according to the desired configuration, but they do not need to be connected to anything for RMII communication.
- SMRXC3, SCOL3, and SCRS3 are not used in RMII mode, so they can be left unconnected.

6.2 RMII Clock Configuration Modes

For KSZ8863RLL RMII, there are five RMII Clock Configuration modes shown in Table 6-2, which also describes the signals used by the RMII bus in five RMII Reference Clock Configuration modes.

TABLE 6-2: KSZ8863RLL RMII CLOCK CONFIGURATION MODES

RMII Clock Configuration Mode	Reg198 bit [3]	Pin 17 SMTXD33/ EN_REFCLKO_3 Internal Pull-Up	Pin 18 SMTXD32 Internal Pull-Up (For Rev A3)	Clock Source	Note
1	0	0 (pull down by 1 kΩ)	0 (pull down by 1 kΩ)	External 50 MHz OSC input to SMTXC3/ REFCLKI_3 and X1 pin directly	EN_REFCLKO_3 = 0 to Disable REF-CLKO_3 for better EMI
2	0	1	0	50 MHz on X1 pin as clock source. REFCLKO_3 Output is Feedback to REF-CLKI_3 externally	EN_REFCLKO_3 = 1 to Enable REF-CLKO_3

TABLE 6-2: KSZ8863RLL RMII CLOCK CONFIGURATION MODES (CONTINUED)

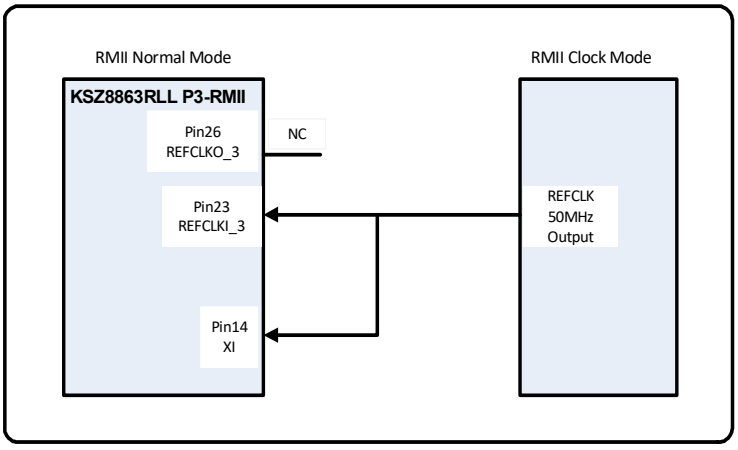
RMII Clock Configuration Mode	Reg198 bit [3]	Pin 17 SMTXD33/ EN_REFCLKO_3 Internal Pull-Up	Pin 18 SMTXD32 Internal Pull-Up (For Rev A3)	Clock Source	Note
3	0	1	1	25 MHz on X1 pin as clock source. REFCLKO_3 Output is connected to REF-CLKI_3 externally	EN_REFCLKO_3 = 1 to Enable REF-CLKO_3
4	1	1	0	50 MHz on X1 pin as clock source. REFCLKO_3 Output is connected to REF-CLKI_3 externally	EN_REFCLKO_3 = 1 to Enable REF-CLKO_3
5	1	1	1	25 MHz on X1 pin as clock source. REFCLKO_3 Output is connected to REF-CLKI_3 internally	EN_REFCLKO_3 = 1 to Enable REF-CLKO_3

1. **Mode 1:** KSZ8863RLL RMII is RMII Normal mode (receive 50 MHz REFCLK clock) with PHY/MAC RMII Clock mode (output 50 MHz REFCLK clock). See Table 6-3. Refer to Figure 6-1 for the RMII Configuration mode 1 diagram.

TABLE 6-3: STRAP PINS AND REGISTER SETTINGS FOR MODE 1

Strap Pins and Register Bit for Mode Configuration	Strap and Register Settings	Description
Pin 17 EN_REFCLKO_3	Strap-low, pull-down	Disable pin 26 REFCLKO_3 RMII 50 MHz output
Pin 18 SMTXD32	Strap-low, pull-down	50 MHz to XI pin as KSZ8863RLL clock source
Register 198 bit [3] = 0	Keep default	—

FIGURE 6-1: KSZ8863RLL RMII REFCLK CLOCK CONNECTION MODE 1

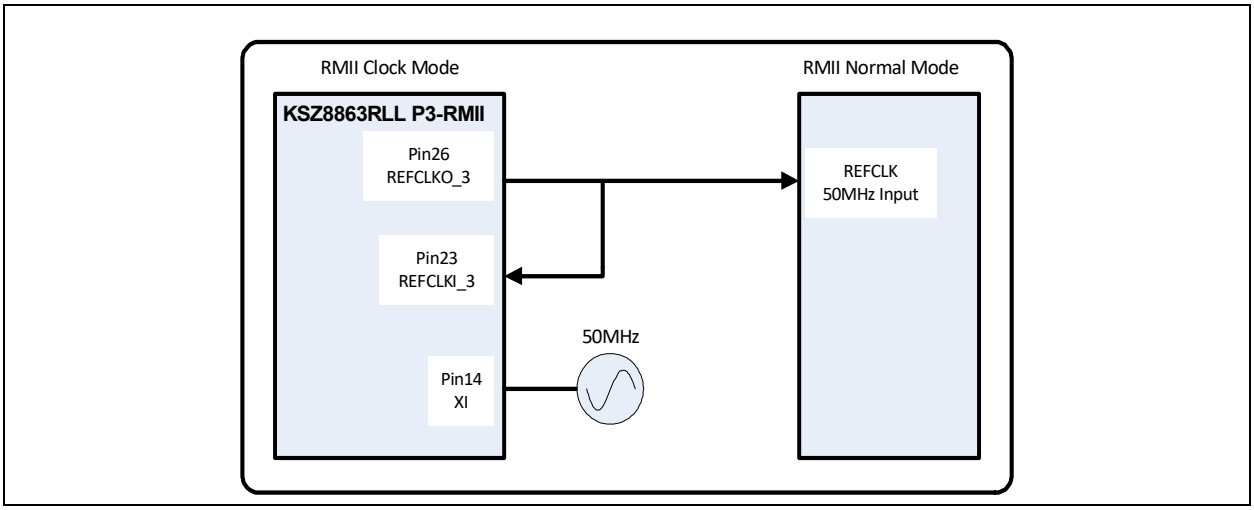


2. **Mode 2:** KSZ8863RLL RMII is RMII Clock mode (output 50 MHz REFCLK clock) with PHY/MAC RMII Normal mode (input 50 MHz REFCLK clock). See Table 6-4. Refer to Figure 6-2 for the RMII Configuration mode 2 diagram.

TABLE 6-4: STRAP PINS AND REGISTER SETTINGS FOR MODE 2

Strap Pins and Register Bit for Mode Configuration	Strap and Register Settings	Description
Pin 17 EN_REFCLKO_3	Pull-up (Default)	Enable pin 26 REFCLKO_3 RMII 50 MHz output
Pin 18 SMTXD32	Strap-low, pull-down	50 MHz to XI pin as KSZ8863RLL clock source
Register 198 bit [3] = 0	Keep default	—

FIGURE 6-2: KSZ8863RLL RMII REFCLK CLOCK CONNECTION MODE 2

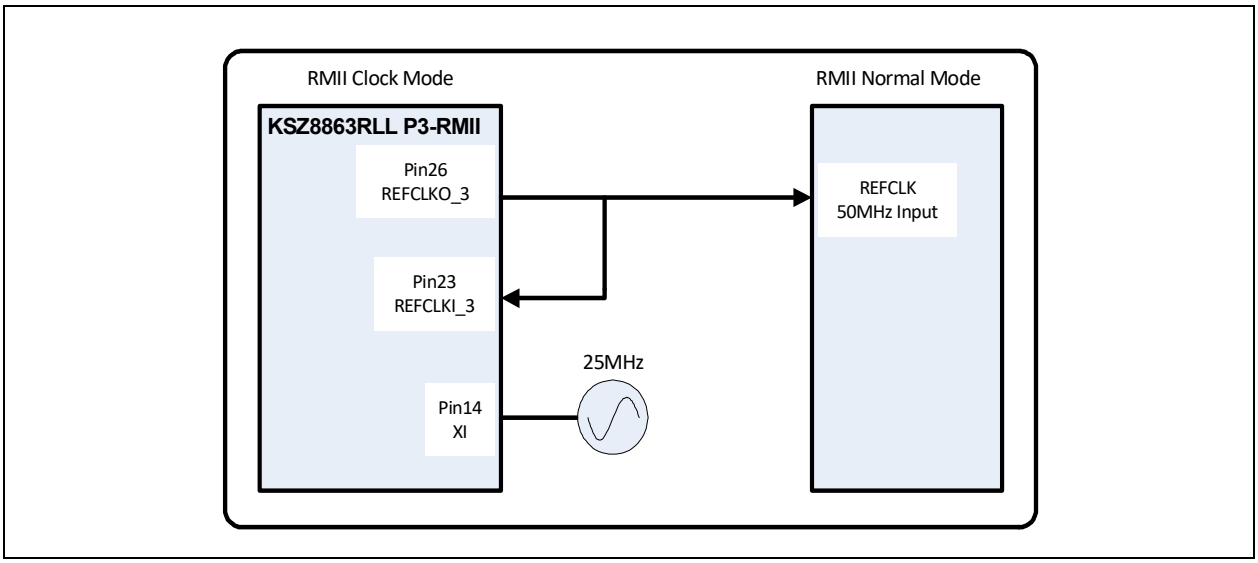


3. **Mode 3:** KSZ8863RLL RMII is RMII Clock mode (output 50 MHz REFCLK clock) with PHY/MAC RMII Normal mode (input 50 MHz REFCLK clock). See Table 6-5. Refer to Figure 6-3 for the RMII Configuration mode 3 diagram.

TABLE 6-5: STRAP PINS AND REGISTER SETTINGS FOR MODE 3

Strap Pins and Register Bit for Mode Configuration	Strap and Register Settings	Description
Pin 17 EN_REFCLKO_3	Pull-up (Default)	Enable pin 26 REFCLKO_3 RMII 50 MHz output
Pin 18 SMTXD32	Pull-up (Default)	25 MHz to XI pin as KSZ8863RLL clock source
Register 198 bit [3] = 0	Keep default	—

FIGURE 6-3: KSZ8863RLL RMII REFCLK CLOCK CONNECTION MODE 3

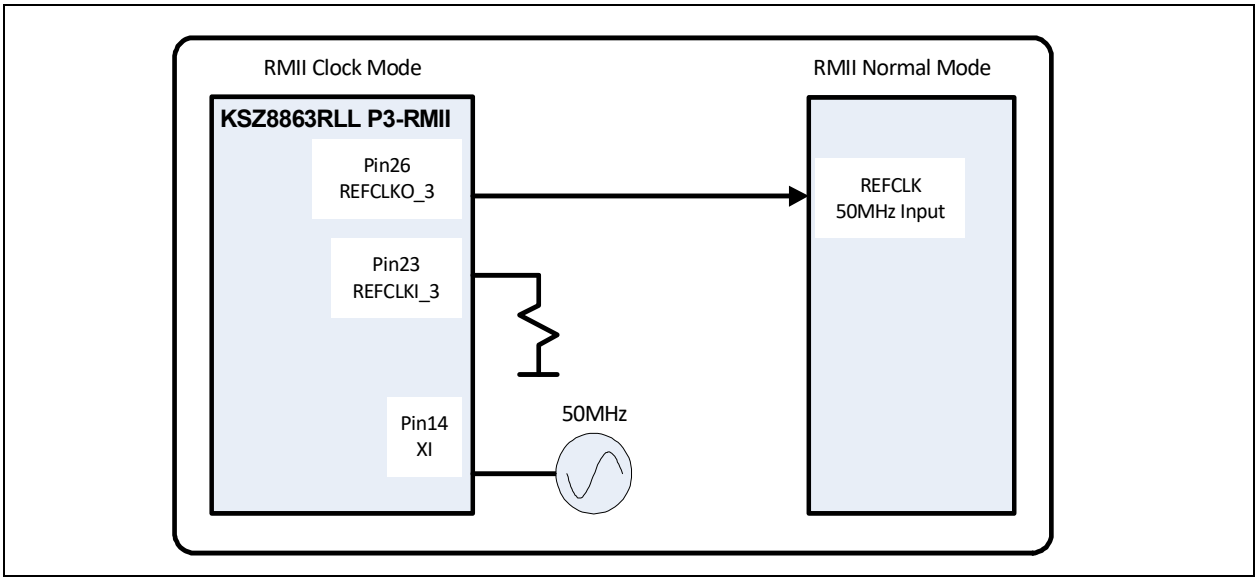


4. **Mode 4:** KSZ8863RLL RMII is RMII Clock mode (output 50 MHz REFCLK clock) with PHY/MAC RMII Normal mode (input 50 MHz REFCLK clock). See Table 6-6. Refer to Figure 6-4 for the RMII Configuration mode 4 diagram.

TABLE 6-6: STRAP PINS AND REGISTER SETTING FOR MODE 4

Strap Pins and Register Bit for Mode Configuration	Strap and Register Settings	Description
Pin 17 EN_REFCLKO_3	Pull-up (Default)	Enable pin 26 REFCLKO_3 RMII 50 MHz output
Pin 18 SMTXD32	Strap-low, pull-down	50 MHz to XI pin as KSZ8863RLL clock source
Register 198 bit [3] = 1	Set REG 198 (0XC6) bit 3	Internal RMII REFCLK 50 MHz clock loopback

FIGURE 6-4: RMII REFCLK CLOCK CONNECTION MODE 4

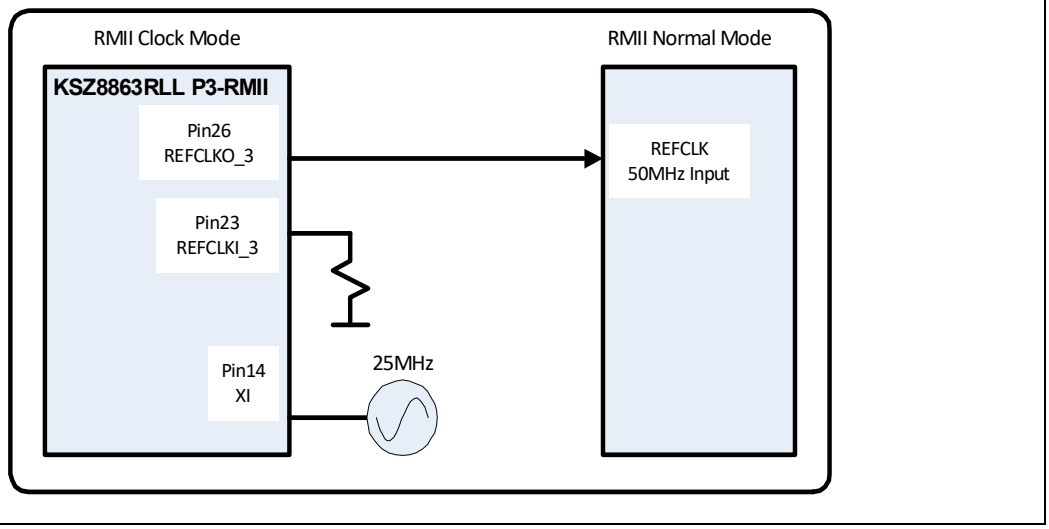


5. **Mode 5:** KSZ8863RLL RMII is RMII Clock mode (output 50 MHz REFCLK clock) with PHY/MAC RMII Normal mode (input 50 MHz REFCLK clock). See Table 6-7. Refer to Figure 6-5 for the RMII Configuration mode 2 diagram.

TABLE 6-7: STRAP PINS AND REGISTER SETTING FOR MODE 5

Strap Pins and Register Bit for Mode Configuration	Strap and Register Settings	Description
Pin 17 EN_REFCLKO_3	Pull-up (Default)	Enable pin 26 REFCLKO_3 RMII 50 MHz output
Pin 18 SMTXD32	Pull-up (Default)	25 MHz crystal or singled-ended source on the XI pin. See Section 5.1, "Crystal and External Oscillator/Clock Connections for RMII Mode," on page 6.
Register 198 bit [3] = 1	Set REG 198 (0XC6) bit 3	Internal RMII REFCLK 50 MHz clock loopback

FIGURE 6-5: KSZ8863RLL RMII REFCLK CLOCK CONNECTION MODE 5



Note 1: Mode 5 is highly recommended because there is no external loopback from REFCLKO to REFCLKI for 50 MHz clock without external noise interference.

2: The KSZ8863RLL provides the MTXER signal. If PHY device RMII does not have a RXER pin, KSZ8863RLL MTXER input pin needs to be tied low by a pull-down resistor.

3: Provisions should be made for series terminations for all outputs on the RMII interface. Series resistors will enable the designer to closely match the output driver impedance of the KSZ8863RLL and PCB trace impedance to minimize ringing on these signals. Exact resistor values are application dependent and must be analyzed in-system. A suggested starting point for the value of these series resistors would be 22Ω.

6.3 RMII Series Termination Resistor Values

TABLE 6-8: RMII SERIES TERMINATIONS AT KSZ8863RLL SIDE

Signals	Series Resistors at KSZ8863RLL RMII Drive Pins	Series Resistors at the Other End RMII Drive Pins
SMRXD31	22Ω	—
SMRXD30	22Ω	—
SMRXDV3	22Ω	—
SMRXD33/REFCLKO_3	22Ω	—
SMTXD31	—	22Ω
SMTXD30	—	22Ω
SMTXEN3	—	22Ω
SMTXC3/REFCLKI_3	—	22Ω (if using mode 1)

Note 1: The series resistors should be placed as close as possible to both KSZ8863RLL RMII drive pins and the other end drive pins in PCB layout.

6.4 Required External Pull-Ups

- When using the RMII interface of the KSZ8863RLL with a MAC device on board, a pull-up resistor of 4.7 kΩ on the **SDA_MDIO** signal (pin 37) is required.
- **INTRN** (pin 35) requires a 4.7 kΩ external pull-up resistor as this output is an open-drain type. If **INTRN** is not used, the pull-up resistor is not required.

7.0 STARTUP

7.1 Reset Circuit

RSTN (pin 47) is an active-low reset input. This signal resets all logic and registers within the KSZ8863RLL. A hardware reset (**RSTN** assertion) is required following power-up. Please refer to the latest copy of the *KSZ8863RLL Data Sheet* for reset timing requirements. Figure 7-1 shows a recommended reset circuit for powering up the KSZ8863RLL device when reset is triggered by the power supply.

FIGURE 7-1: RESET TRIGGERED BY POWER SUPPLY

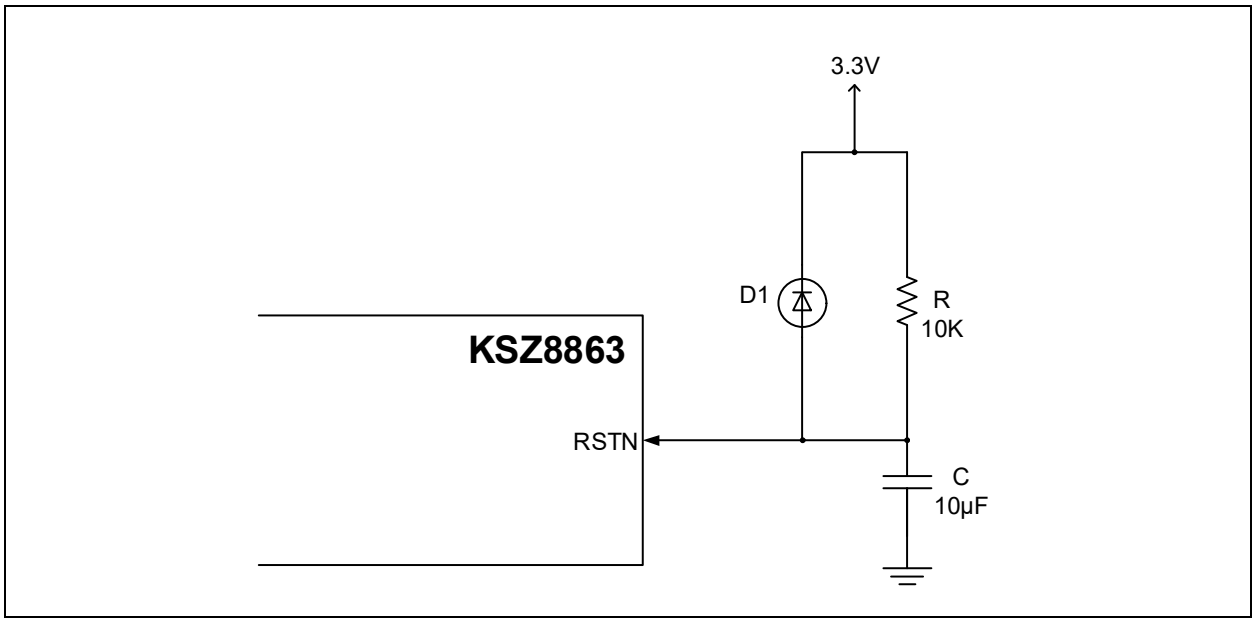
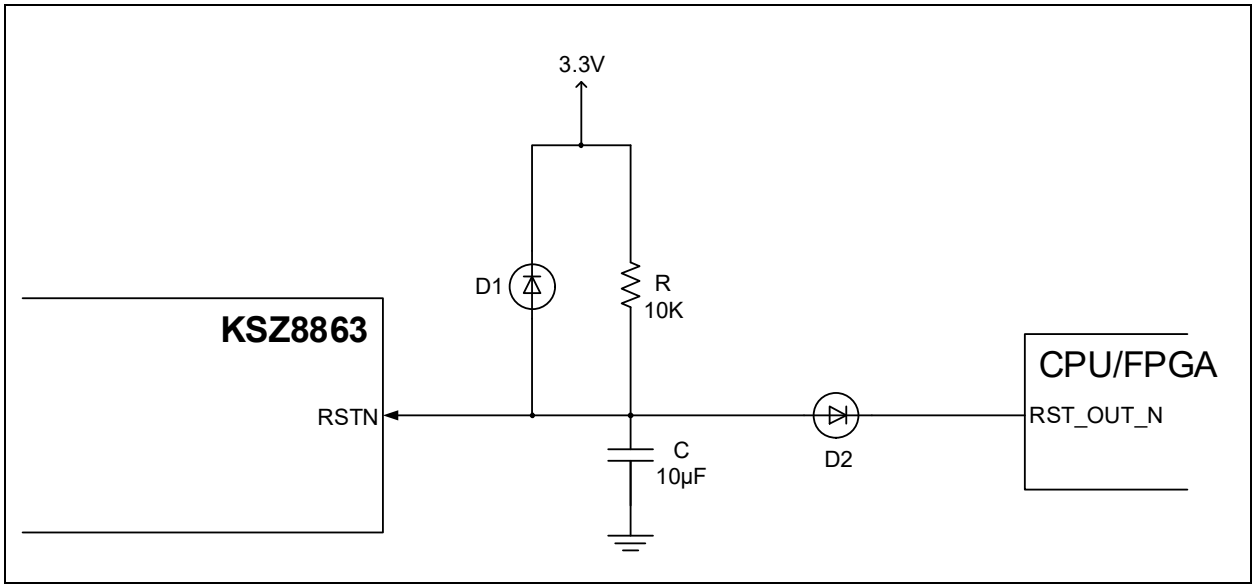


Figure 7-2 shows the recommended reset circuit for applications where reset is driven by external CPU or FPGA. The reset out pin, RST_OUT_N, from CPU/FPGA provides the warm reset after power-up. If the Ethernet device and CPU/FPGA use the same VDDIO voltage, D2 can be removed and both reset pins can be connected directly.

FIGURE 7-2: RESET CIRCUIT INTERFACE WITH CPU/FPGA RESET OUTPUT



7.2 Configuration Mode Pins (Strapping Options)

The KSZ8863RLL utilizes configuration strap pins to configure the device for different modes. Pull-up/down resistors are used to create High or Low states on these pins, which are internally sampled at the rising edge of **RSTN**. All these pins have a weak internal pull-up or pull-down resistor which provides a default level for strapping. To strap an LED pin low, use a 1 kΩ external pull-down resistor. To strap a non-LED pin high, use an external 1 kΩ to 10 kΩ pull-up resistor to VDDIO.

Note:	Other device connected to the RMII interface may have internal pull-ups or pull-downs that influence the strapping pin voltages during reset. Because of this, an external resistor is recommended whenever the strap pin connects to another device, regardless of the desired strap level.

The configuration strap pins and their associated functions are detailed in Table 7-1.

TABLE 7-1: CONFIGURATION STRAP DESCRIPTIONS

Configuration Strap Pin	Description
SMTXD33/ EN_REFCLKO_3	**RMII mode Clock selection** PU = Enable REFCLKO_3 output PD = Disable REFCLKO_3 output
SMTXD32	**X1 pin Clock selection (for Rev A3 and behind A3)** PU = 25 MHz to X1 pin as clock source (default) PD = 50 MHz to X1 pin as clock source to provide or receive 50 MHz RMII reference clock for RLL part
SMRXDV3	**Force Duplex mode (P1DPX)** PU = Port 1 default to Full-Duplex mode if P1ANEN = 1 and auto-negotiation fails. Force port 1 in Full-Duplex mode if P1ANEN = 0. PD = Port 1 default to Half-Duplex mode if P1ANEN = 1 and auto-negotiation fails. Force port 1 in Half-Duplex mode if P1ANEN = 0.
SMRXD33/ REFCLKO_3	**Output reference clock in RMII mode.** **Enable auto-negotiation on port 2 (P2ANEN)** PU = Enable PD = Disable
SMRXD32	**Force the speed on port 2 (P2SPD)** PU = Force port 2 to 100BT if P2ANEN = 0 PD = Force port 2 to 10BT if P2ANEN = 0
SMRXD31	**Force duplex mode (P2DPX)** PU = Port 2 default to Full-Duplex mode if P2ANEN = 1 and auto-negotiation fails. Force port 2 in Full-Duplex mode if P2ANEN = 0. PD = Port 2 set to Half-Duplex mode if P2ANEN = 1 and auto-negotiation fails. Force port 2 in Half-Duplex mode if P2ANEN = 0.
SMRXD30	**Force flow control on port 2 (P2FFC)** PU = Always enable (force) port 2 flow control feature. PD = Port 2 flow control feature enable is determined by auto-negotiation result.
SPIQ	**Force flow control on port 1 (P1FFC)** PU = Always enable (force) port 1 flow control feature PD = Port 1 flow control feature enable is determined by auto-negotiation result.
P1LED1	**Force the speed on port 1 (P1SPD)** PU = Force port 1 to 100BT if P1ANEN = 0 PD = Force port 1 to 10BT if P1ANEN = 0
P1LED0	**Enable auto-negotiation on port 1 (P1ANEN)** PU = Enable (better to pull up in design) PD = Disable (default)

TABLE 7-1: CONFIGURATION STRAP DESCRIPTIONS (CONTINUED)

Configuration Strap Pin	Description
P2LED1	**Serial bus configuration** Serial bus configuration pins to select mode of access to KSZ8863MLL/FLL/RLL internal registers. **[P2LED1, P2LED0] = [0, 0] - I2C Master (EEPROM) mode** (If EEPROM is not detected, the KSZ8863MLL/FLL/RLL is configured with the default values of its internal registers and the values of its strap-in pins.) **Interface Signals:** SPIQ – Not used (tri-stated) SCL_MDC – I^2C clock SDA_MDIO – I^2C data I/O SPISN – Not used **[P2LED1, P2LED0] = [0, 1] — I2C Slave mode** The external I2C Master drives the SCL_MDC clock. The KSZ8863MLL/FLL/RLL device addresses are: 1011_1111 <read> 1011_1110 <write>
P2LED0	**Interface Signals:** SPIQ – Not used (tri-stated) SCL_MDC – I^2C clock SDA_MDIO – I^2C data I/O SPISN – Not used **[P2LED1, P2LED0] = [1, 0] - SPI Slave mode** **Interface Signals:** SPIQ – SPI data out SCL_MDC – SPI clock SDA_MDIO – SPI data in SPISN – SPI chip select **[P2LED1, P2LED0] = [1, 1] - SMI/MIIM mode** In SMI mode, KSZ8863MLL/FLL/RLL provides access to all its internal 8-bit registers through its SCL_MDC and SDA_MDIO pins. In MIIM mode, KSZ8863MLL/FLL/RLL provides access to its 16-bit MIIM registers through its SDC_MDC and SDA_MDIO pins.

7.3 LED Pins

The KSZ8863RLL provides two LED signals per port. These indicators will display speed, link, and activity information about the current state of the switch ports. The LED pins are active low and require a series resistor to a power supply to properly light the LED. Series resistance is dependent on the LED used.

By default, the PxLED0 pin indicates the link and activity status while the PxLED1 pin indicates the speed status, as shown in Table 7-2.

TABLE 7-2: LED PIN DEFINITION

LED Pin	Pin State	Pin LED Definition	Link/Activity
PxLED0	L	ON	Link On
	Toggle	Blinking	Activity
	H	OFF	No Activity
PxLED1	H	OFF	OFF
	L	ON	Speed

The register 195 bit [5:4] is used to change the default LED behavior. Table 7-3 shows the register information.

TABLE 7-3: REGISTER 195: POWER MANAGEMENT AND LED MODE

Bits	Name	Description	Default
5-4	LED Mode Selection	00 = LED0: Link/ACT, LED1: Speed 01 = LED0: Link, LED1: ACT 10 = LED0: Link/ACT, LED1: Duplex 11 = LED0: Link, LED1: Duplex	00

8.0 MISCELLANEOUS

8.1 ISET Resistor

ISET (pin 6) on the KSZ8863RLL should connect to digital ground through a 11.8 kΩ resistor with a tolerance of 1%. This is used to set up critical bias currents for the embedded 10/100 Ethernet physical device.

8.2 Other Considerations

- Incorporate a large SMD footprint (SMD_1210) to connect the chassis ground to the digital ground. This will allow some flexibility at EMI testing for different grounding options. Leaving the footprint open will allow the two grounds to remain separate. Shorting them together with a zero-ohm resistor will connect them. For best performance, short them together with a cap or a ferrite bead.
- Be sure to incorporate enough bulk capacitors (4.7 µF to 22 µF) in each power plane.

NOTES:

9.0 HARDWARE CHECKLIST SUMMARY

TABLE 9-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Required Reference"	All necessary documents are on hand.		
	Section 2.2, "Pin Check"	The pins match the data sheet.		
	Section 2.3, "Ground"	Connect all **GND** and **AGND** pins to the same board ground. A solid board ground plane is essential.		
Section 3.0, "Power"	Section 3.0, "Power"	When **VDDIO** is 2.5V or above, the chip outputs 1.8V on **VDDCO**. Connect this externally to power **VDDA_1.8** and **VDDC**. Decoupling caps are needed.		
		Ensure **VDDA_3.3** is in the range 3.135V to 3.465V, and **VDDIO** is in the range 1.71V to 3.465V, and a 22 µF capacitor is on each pin.		
Section 4.0, "Ethernet Signals"	Section 4.1, "PHY No. 1 Interface" and Section 4.2, "PHY No. 2 Interface"	Verify the termination resistors (49.9Ω, 1%) and capacitors (0.1 uF) on the TX and RX pins.		
	Section 4.3, "Magnetics Connection"	Verify if the center taps are connected to the **VDDA_3.3** (pin 3) supply on the KSZ8863RLL device side and are terminated with 75Ω resistors through a 1000 pF, 2 kV capacitor to chassis ground on the RJ45 line side.		
	Section 4.4, "RJ45 Connector"	Verify if pins 4/5 and 7/8 of the RJ45 are connect to CAT-5 cable and are terminated to chassis ground through a 1000 pF, 2 kV capacitor.		
Section 5.0, "Clock Circuit"	Section 5.1, "Crystal and External Oscillator/Clock Connections for RMII Mode"	Verify the usage of 25 MHz ±50 ppm crystal/oscillator. Verify the usage of 50 MHz ±50 ppm oscillator.		
Section 6.0, "Digital Interface"	Section 6.1, "RMII Interface"	Verify RMII connections.		
	Section 6.2, "RMII Clock Configuration Modes"	There are five RMII Clock Configuration modes. Select one of the five modes based on Figure 6-1, Figure 6-2, Figure 6-3, Figure 6-4, and Figure 6-5 in this design and confirm the strap-in configuration correctly.		
	Section 6.3, "RMII Series Termination Resistor Values"	Check if there are 22Ω resistors for all drive pins of KSZ8863RLL and another end device if the trace length is more than about one inch.		
	Section 6.4, "Required External Pull-Ups"	Check if there are 4.7 kΩ pull-up resistors for MDIO pin and INTRN pin if this pin is used.		
Section 7.0, "Startup"	Section 7.1, "Reset Circuit"	Confirm proper reset circuit design: standalone reset or external CPU/FPGA reset.		
	Section 7.3, "LED Pins"	If used, confirm proper connections, taking into consideration the configuration strapping requirements. Use 750Ω to 1kΩ when strapping low or 10kΩ to strap high.		
Section 8.0, "Miscellaneous"	Section 8.1, "ISET Resistor"	Confirm proper ISET resistor (11.8 kΩ, 1%).		
	Section 8.2, "Other Considerations"	Incorporate a large SMD footprint (SMD_1210) to connect the chassis ground to the digital ground. Incorporate sufficient power plane bulk capacitors (4.7 µF to 22 µF).		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00003048B (09-18-19)	Section 6.0, "Digital Interface"	Modified the numbering of subsections.
	Table 9-1	Added Section 6.1, "RMII Interface", Section 6.2, "RMII Clock Configuration Modes"Section 6.3, "RMII Series Termination Resistor Values" and Section 6.4, "Required External Pull-Ups".
	All	Made minor text changes.
DS00003048A (05-14-19)	Initial release.	

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