PIC24FJ128GL306 Family Silicon Errata and Data Sheet Clarification

The PIC24FJ128GL306 family devices conform functionally to the current Device Data Sheet (DS30010198**B**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC24FJ128GL306 family silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A4**).

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC24FJ128GL306 family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)
		A4
PIC24FJ128GL306	0x220E	0x03
PIC24FJ64GL306	0x2206	
PIC24FJ128GL305	0x220C	
PIC24FJ64GL305	0x2204	
PIC24FJ128GL303	0x220A	
PIC24FJ64GL303	0x2202	
PIC24FJ128GL302	0x2208	
PIC24FJ64GL302	0x2200	

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC24FJ128GL306 Family Flash Programming Specification"* (DS30010194) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions[1]
				A4
Oscillator	Clock Switch	1.	Clock switch to FRC+PLL does not occur after $\overline{\text{MCLR}}$.	X
Oscillator	FSCM	2.	`RESET` instruction in oscillator trap locks up device.	X
UART	Break Character Transmission	3.	The Transmit Shift Register Empty (TRMT) bit is unreliable when there are back-to-back Break character transmissions.	X
CCP	32-Bit Mode	4.	MCCP timer in 32-bit mode cannot be cleared by writing a zero to the Timer register.	X
I2C	Client Mode	5.	In Client mode, an address cannot be received when the device is in Idle and the module is set for discontinue in Idle (I2CSIDL = `1`).	X
I2C	Multiple Client Mode	6.	In applications with multiple I^2C Clients and General Call enabled, unexpected behavior is observed in the unaddressed Client.	X
I2C	Client Transmit	7.	Client transmits 0xFF if ACKDT bit is set prior to transmission.	X
LCD	Frame Counter	8.	Frame counter can be written at any time.	X
Flash Program Memory	Double Error Trap	9.	Using software breakpoints in the last page of program memory can lead to an ECC double error trap getting generated.	X
Power	Retention Sleep Mode	10.	For temperatures below -20ºC, a Reset may occur when the device wakes from Retention Sleep mode.	X
Power	I/O Leakage	11.	At high temperatures, the device pin leakage current can increase up to 2 µA.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A4**).

1. Module: Oscillator

A clock switch to FRC+PLL after POR will cause the device to hang if the POSC is disabled/not present and PLLSS = PRI is selected.

Work around

If POSC is disabled/not present, then PLLSS should be set to FRC. PLLSS = PRI is an invalid configuration when POSC is not present.

Affected Silicon Revisions

A4							
X							

2. Module: Oscillator

When the device is clocked from the Primary Oscillator with PLL (XT+PLL, HS+PLL or EC+PLL), it may not recover from the oscillator failure (Fail-Safe Clock Monitor event) if a `RESET` instruction is executed in the oscillator trap. The device will lock up.

Work around

In the application code, the device should be started from FRC (defined in the Configuration bits). Then the clock should be switched to the Primary Oscillator with PLL.

Affected Silicon Revisions

A4							
X							

3. Module: UART

The Transmit Shift Register Empty (TRMT) bit is unreliable when there are back-to-back Break character transmissions. For back-to-back Break characters, the TRMT bit may not reflect the actual status. If user software is polling for this bit to be set, it may result in dummy bytes getting transmitted instead of Break characters.

Work around

Poll the UARTx Transmit Break bit, UTXBRK (UxSTA[11]), to be cleared instead of the TRMT bit (U1STA[8]) to be set. The UTXBRK status bit will be cleared after a Break character transmission.

Affected Silicon Revisions

A4							
X							

4. Module: CCP

The MCCP timer in 32-bit mode cannot be cleared by writing a zero to the Timer register.

Work around

Switch to 16-bit mode, clear both low and high words and then go back to 32-bit mode.

Affected Silicon Revisions

A4							
X							

5. Module: I^2C

In I^2C In Client mode, an address cannot be received when the device is in Idle and the module is set for discontinue in Idle (I2CSIDL = `1`).

Work around

None.

Affected Silicon Revisions

A4							
X							

6. Module: I²C

In applications with multiple I²C Clients and General Call (GCEN (I2CxCONL[7]) = 1) is enabled, unexpected behavior is observed in the unaddressed Client when the data payload of the addressed Client matches the general call address (00h).

When the issue occurs, unexpected data might be received in the unaddressed Client. If Address Hold is enabled (AHEN (I2CxCONH[1]) = 1), then I²C will erroneously ACK the byte.

Work around

If Address Hold is enabled (I2CxCONH[1] = 1), Acknowledge Data (ACKDT (I2CxCONL[5]) = 1) should be set during initialization.

Instead of Client interrupt, poll the Receive Buffer Full Status bit and read the receive buffer to clear the unwanted data.

Affected Silicon Revisions

A4							
X							

7. Module: I²C

When the Client is transmitting data, if Acknowledge Data (ACKDT (I2CxCONL[5]) = 1) is set before the Client starts transmission, then the second data transmitted will be 0xFF, irrespective of the actual data in I2CxTRN.

Work around

Clear the ACKDT bit before Client transmission.

Affected Silicon Revisions

A4							
X							

8. Module: LCD

The LCD Frame Counter register (LCDFCx) can be written while the LCD Enhanced mode is active, which can impact blink and blank frame timings configured before Enhanced mode was enabled.

Work around

Software should only write FCx register bits when LCD Frame Counter x is disabled or ELCDEN = 0.

Affected Silicon Revisions

A4							
X							

9. Module: Flash Program Memory

Using software breakpoints in the last page of program memory can lead to an ECC double error trap getting generated.

Work around

Avoid using software breakpoints in the last page; use hardware breakpoints instead.

Affected Silicon Revisions

A4							
X							

10. Module: Power

For a temperature below -20ºC, a device Reset may occur occasionally when the device wakes from Retention Sleep mode (RETEN bit (RCON[12]) = 1, LPCFG bit (FPOR[2]) = 0). The BOR, POR and EXTR bits in the RCON register are set erroneously for this Reset.

Work around

None.

Affected Silicon Revisions

A4							
X							

11. Module: Power

For temperatures between +65ºC and +125ºC, the device pin leakage current specified by parameters DI50, DI51, DI55 and DI56 can increase up to 2 µA.

Work around

None.

Affected Silicon Revisions

A4							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS30010198**B**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Electrical Characteristics

Note 3 in **TABLE 30-32: A/D Module Specifications"** has been changed as shown below in **bold**:

Code 511 and 2559 can have a DNL error of -1LSB to < +1LSB, Code 1023 can have a DNL error of ≥ -1.5 LSB to < 1 LSB, code 2047 can have a DNL error of ≥ **-1.5** LSB to < 1.5 LSB and code 3071 can have a DNL error of > **-1** LSB to < 2.5 LSB.

2. Module: UART

REGISTER 17-6: UxADMD: UARTx Address Detect and Match Register is unimplemented.

The address match detect feature is not available in this device.

3. Module: Electrical Characteristics

Parameter No. D300 in **Table 30-13 "Comparator DC Specifications"** has been changed as shown below.

TABLE 30-13: COMPARATOR DC SPECIFICATIONS

Operating Conditions:		-40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Comments
D300	VIOFF	Input Offset Voltage	—	12	**40(3)**	mV	**-10°C ≤ TA ≤ +125°C (Note 1)**
			—	**12**	**55(3)**	**mV**	**-40°C ≤ TA ≤ -10°C (Note 1)**

Note 1: Parameters are characterized but not tested.

2: Measured with one input at VDD/2 and the other transitioning from VSS to VDD, 40 mV step, 15 mV overdrive.

3: Due to the effect of aging, this value may drift up to an additional 10 mV over the lifetime of the device.

4. Module: On-Chip Voltage Regulator

In **Section 27.3.3 "Low-Voltage Retention Regulator"**, changes shown below in bold have been removed:

This regulator, which operates at 1.2V nominal, maintains power to data RAM and the RTCC, **while all other core digital logic is powered down**.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (7/2020)

Initial release of this document; issued for Silicon Revision A4.

Rev B Document (5/2021)

Adds silicon issue 10 (Power).

The I^2C standard uses the terminology “Master” and “Slave.” The equivalent Microchip terminology used in this document is “Host” and “Client”, respectively.

Rev C Document (9/2021)

Adds data sheet clarifications 3 (Electrical Characteristics) and 4 (On-Chip Voltage Regulator).

Rev D Document (4/2023)

Updates existing data sheet clarifications 1 (Electrical Characteristics) and 3 (Electrical Characteristics).

Rev E Document (7/2024)

Adds silicon issue 11 (Power).

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable" Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Trademarks

ISBN: 978-1-6683-4937-3

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880- 3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4485-5910
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-72400

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Hod Hasharon
Tel: 972-9-775-5100

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7288-4388

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820