

**PIC24FJ128GL306 Family  
Silicon Errata and Data Sheet Clarification**

The PIC24FJ128GL306 family devices conform functionally to the current Device Data Sheet (DS30010198B), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in [Table 1](#). The silicon issues are summarized in [Table 2](#).


The errata described in this document will be addressed in future revisions of the PIC24FJ128GL306 family silicon.

**Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of [Table 2](#) apply to the current silicon revision (**A4**).

Data Sheet clarifications and corrections start on [page 5](#), following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip’s programmers, debuggers and emulation tools, which are available at the Microchip corporate website ([www.microchip.com](http://www.microchip.com)).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
  - a) For MPLAB IDE 8, select *Programmer > Reconnect*.
  - b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon (  ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

**Note:** If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC24FJ128GL306 family silicon revisions are shown in [Table 1](#).

**TABLE 1: SILICON DEVREV VALUES**

Part Number	Device ID <sup>(1)</sup>	Revision ID for Silicon Revision <sup>(2)</sup>
		A4
PIC24FJ128GL306	0x220E	0x03
PIC24FJ64GL306	0x2206	
PIC24FJ128GL305	0x220C	
PIC24FJ64GL305	0x2204	
PIC24FJ128GL303	0x220A	
PIC24FJ64GL303	0x2202	
PIC24FJ128GL302	0x2208	
PIC24FJ64GL302	0x2200	

- Note 1:** The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format “DEVID DEVREV”.
- 2:** Refer to the “*PIC24FJ128GL306 Family Flash Programming Specification*” (DS30010194) for detailed information on Device and Revision IDs for your specific device.

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**TABLE 2: SILICON ISSUE SUMMARY**

Module	Feature	Item Number	Issue Summary	Affected Revisions <sup>(1)</sup>
				A4
Oscillator	Clock Switch	1.	Clock switch to FRC+PLL does not occur after MCLR.	X
Oscillator	FSCM	2.	RESET instruction in oscillator trap locks up device.	X
UART	Break Character Transmission	3.	The Transmit Shift Register Empty (TRMT) bit is unreliable when there are back-to-back Break character transmissions.	X
CCP	32-Bit Mode	4.	MCCP timer in 32-bit mode cannot be cleared by writing a zero to the Timer register.	X
I2C	Client Mode	5.	In Client mode, an address cannot be received when the device is in Idle and the module is set for discontinue in Idle (I2CSIDL = 1).	X
I2C	Multiple Client Mode	6.	In applications with multiple I <sup>2</sup> C Clients and General Call enabled, unexpected behavior is observed in the unaddressed Client.	X
I2C	Client Transmit	7.	Client transmits 0xFF if ACKDT bit is set prior to transmission.	X
LCD	Frame Counter	8.	Frame counter can be written at any time.	X
Flash Program Memory	Double Error Trap	9.	Using software breakpoints in the last page of program memory can lead to an ECC double error trap getting generated.	X
Power	Retention Sleep Mode	10.	For temperatures below -20°C, a Reset may occur when the device wakes from Retention Sleep mode.	X
Power	I/O Leakage	11.	At high temperatures, the device pin leakage current can increase up to 2 μA.	X

**Note 1:** Only those issues indicated in the last column apply to the current silicon revision.

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## Silicon Errata Issues

**Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A4**).

### 1. Module: Oscillator

A clock switch to FRC+PLL after POR will cause the device to hang if the POSC is disabled/not present and PLLSS = PRI is selected.

#### Work around

If POSC is disabled/not present, then PLLSS should be set to FRC. PLLSS = PRI is an invalid configuration when POSC is not present.

#### Affected Silicon Revisions

A4								
X								

### 2. Module: Oscillator

When the device is clocked from the Primary Oscillator with PLL (XT+PLL, HS+PLL or EC+PLL), it may not recover from the oscillator failure (Fail-Safe Clock Monitor event) if a RESET instruction is executed in the oscillator trap. The device will lock up.

#### Work around

In the application code, the device should be started from FRC (defined in the Configuration bits). Then the clock should be switched to the Primary Oscillator with PLL.

#### Affected Silicon Revisions

A4								
X								

### 3. Module: UART

The Transmit Shift Register Empty (TRMT) bit is unreliable when there are back-to-back Break character transmissions. For back-to-back Break characters, the TRMT bit may not reflect the actual status. If user software is polling for this bit to be set, it may result in dummy bytes getting transmitted instead of Break characters.

#### Work around

Poll the UARTx Transmit Break bit, UTXBRK (UxSTA[11]), to be cleared instead of the TRMT bit (U1STA[8]) to be set. The UTXBRK status bit will be cleared after a Break character transmission.

#### Affected Silicon Revisions

A4								
X								

### 4. Module: CCP

The MCCP timer in 32-bit mode cannot be cleared by writing a zero to the Timer register.

#### Work around

Switch to 16-bit mode, clear both low and high words and then go back to 32-bit mode.

#### Affected Silicon Revisions

A4								
X								

### 5. Module: I<sup>2</sup>C

In I<sup>2</sup>C In Client mode, an address cannot be received when the device is in Idle and the module is set for discontinue in Idle (I2CSIDL = 1).

#### Work around

None.

#### Affected Silicon Revisions

A4								
X								

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## 6. Module: I<sup>2</sup>C

In applications with multiple I<sup>2</sup>C Clients and General Call (GCEN (I2CxCONL[7]) = 1) is enabled, unexpected behavior is observed in the unaddressed Client when the data payload of the addressed Client matches the general call address (00h).

When the issue occurs, unexpected data might be received in the unaddressed Client. If Address Hold is enabled (AHEN (I2CxCONH[1]) = 1), then I<sup>2</sup>C will erroneously ACK the byte.

### **Work around**

If Address Hold is enabled (I2CxCONH[1] = 1), Acknowledge Data (ACKDT (I2CxCONL[5]) = 1) should be set during initialization.

Instead of Client interrupt, poll the Receive Buffer Full Status bit and read the receive buffer to clear the unwanted data.

### **Affected Silicon Revisions**

A4							
X							

## 7. Module: I<sup>2</sup>C

When the Client is transmitting data, if Acknowledge Data (ACKDT (I2CxCONL[5]) = 1) is set before the Client starts transmission, then the second data transmitted will be 0xFF, irrespective of the actual data in I2CxTRN.

### **Work around**

Clear the ACKDT bit before Client transmission.

### **Affected Silicon Revisions**

A4							
X							

## 8. Module: LCD

The LCD Frame Counter register (LCDFCx) can be written while the LCD Enhanced mode is active, which can impact blink and blank frame timings configured before Enhanced mode was enabled.

### **Work around**

Software should only write FCx register bits when LCD Frame Counter x is disabled or ELCDEN = 0.

### **Affected Silicon Revisions**

A4							
X							

## 9. Module: Flash Program Memory

Using software breakpoints in the last page of program memory can lead to an ECC double error trap getting generated.

### **Work around**

Avoid using software breakpoints in the last page; use hardware breakpoints instead.

### **Affected Silicon Revisions**

A4							
X							

## 10. Module: Power

For a temperature below -20°C, a device Reset may occur occasionally when the device wakes from Retention Sleep mode (RETEN bit (RCON[12]) = 1, LPCFG bit (FPOR[2]) = 0). The BOR, POR and EXTR bits in the RCON register are set erroneously for this Reset.

### **Work around**

None.

### **Affected Silicon Revisions**

A4							
X							

## 11. Module: Power

For temperatures between +65°C and +125°C, the device pin leakage current specified by parameters DI50, DI51, DI55 and DI56 can increase up to 2 µA.

### **Work around**

None.

### **Affected Silicon Revisions**

A4							
X							

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## Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS30010198B):

**Note:** Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

### 1. Module: Electrical Characteristics

**Note 3** in **TABLE 30-32: A/D Module Specifications** has been changed as shown below in **bold**:

**Code 511 and 2559 can have a DNL error of -1LSB to < +1LSB, Code 1023 can have a DNL error of  $\geq -1.5$  LSB to < 1 LSB, code 2047 can have a DNL error of  $\geq -1.5$  LSB to < 1.5 LSB and code 3071 can have a DNL error of > -1 LSB to < 2.5 LSB.**

### 2. Module: UART

**REGISTER 17-6: UxADMD: UARTx Address Detect and Match Register** is unimplemented.

The address match detect feature is not available in this device.

### 3. Module: Electrical Characteristics

Parameter No. D300 in **Table 30-13 “Comparator DC Specifications”** has been changed as shown below.

TABLE 30-13: COMPARATOR DC SPECIFICATIONS

Operating Conditions: $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended							
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Comments
D300	V <sub>IOFF</sub>	Input Offset Voltage	—	12	<b>40<sup>(3)</sup></b>	mV	<b><math>-10^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}</math> (Note 1)</b>
			—	<b>12</b>	<b>55<sup>(3)</sup></b>	<b>mV</b>	<b><math>-40^{\circ}\text{C} \leq T_A \leq -10^{\circ}\text{C}</math> (Note 1)</b>

Note 1: Parameters are characterized but not tested.

2: Measured with one input at  $V_{DD}/2$  and the other transitioning from  $V_{SS}$  to  $V_{DD}$ , 40 mV step, 15 mV overdrive.

3: **Due to the effect of aging, this value may drift up to an additional 10 mV over the lifetime of the device.**

### 4. Module: On-Chip Voltage Regulator

In **Section 27.3.3 “Low-Voltage Retention Regulator”**, changes shown below in **bold** have been removed:

This regulator, which operates at 1.2V nominal, maintains power to data RAM and the RTCC, **while all other core digital logic is powered down.**

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## APPENDIX A: DOCUMENT REVISION HISTORY

### Rev A Document (7/2020)

Initial release of this document; issued for Silicon Revision A4.

### Rev B Document (5/2021)

Adds silicon issue 10 ([Power](#)).

The I<sup>2</sup>C standard uses the terminology “Master” and “Slave.” The equivalent Microchip terminology used in this document is “Host” and “Client”, respectively.

### Rev C Document (9/2021)

Adds data sheet clarifications 3 ([Electrical Characteristics](#)) and 4 ([On-Chip Voltage Regulator](#)).

### Rev D Document (4/2023)

Updates existing data sheet clarifications 1 ([Electrical Characteristics](#)) and 3 ([Electrical Characteristics](#)).

### Rev E Document (7/2024)

Adds silicon issue 11 ([Power](#)).

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