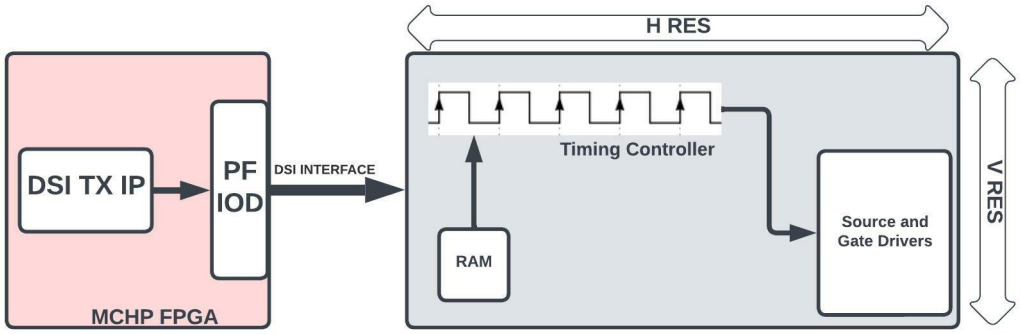
MIPI DSI TX IP User Guide

Introduction

Mobile Industry Processor Interface (MIPI) Display Serial Interface (DSI) is a standard specification defined by the MIPI Alliance display working group. The DSI specification defines an interface between a display device and a host processor. It is built on the existing MIPI Alliance specifications by adopting pixel formats and command set specified in DPI-2, DBI-2, and DCS standards. This user guide describes the MIPI DSI transmitter IP developed for Microchip FPGAs. The following figure shows the block diagram of DSI TX IP.

Figure 1. Microchip DSI TX IP Use Case



Microchip's FPGAs have high-speed serial interface capabilities with their IOD blocks. The DSI TX IP interfaces with a video timing generator on the input side and an IOD block on the output side to drive a DSI display. The DSI IP transmitter encodes the pixel data compliant to the MIPI DSI standards. This IP Core supports 4 lanes RGB-888 and YCbCr-422 data types and operates in two modes on the physical layer high-speed mode and low-power mode. In high-speed mode, MIPI DSI supports the transmission of image data using short and long packets. Short packets are used to send control information, and long packets are used to send video content on the DSI lanes. For video data, one long packet is equivalent to one image data line. Low power is used for power saving purpose.

Key Features

The MIPI DSI Transmitter IP supports:

- Command Mode
- Video Mode

Supported Data format: 24-bit RGB 8:8:8 and 16-bit YCbCr 4:2:2

Supported Lane Configuration: 4 Lanes

Supported Families

- PolarFire® SoC FPGA
- PolarFire FPGA

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1. Command and Video Modes

DSI-compliant peripherals support two basic modes of operation: Command and Video modes. Depends on the architecture and capabilities of the display module you can select either Command or Video mode. A few Video mode display modules also include a simplified form of Command mode operation.

1.1 Command Mode

Transactions in Command mode primarily take the form of sending commands and data to the display module, that incorporates the display controller. The display controller might include local registers and a compressed or an uncompressed frame buffer. Systems write to the registers and frame buffers using Command mode. The host processor indirectly controls the activity at the display module by sending commands, parameters, and data to the display controller.

1.2 Video Mode

Transactions from the host processor to the display module take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at a sufficient bandwidth to avoid flicker or other artifacts in the displayed image. Video mode information must only be transmitted in high-speed mode.

Some Video mode architectures might include a simple timing controller and a partial frame buffer used to make the the interface to be shutdown to reduce power consumption.

1.3 Timing of Video Mode Interface

Video Mode peripherals require pixel data delivered in real time. This section specifies the format and timing of DSI traffic for this type of display module.

DSI supports several formats or packet sequences, for Video Mode data transmission. The peripheral's timing requirements tells which format is appropriate.

- Non-Burst Mode with Sync Pulses—enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.
- Non-Burst Mode with Sync Events—similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.
- Burst Mode – RGB pixel packets are time—compressed, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link.

Important:

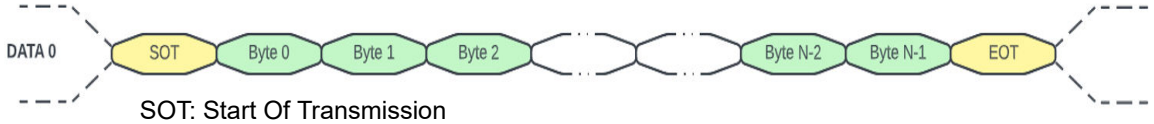
1. Accurate reconstruction of timing, packet overhead including Data ID, ECC, and Checksum bytes must be taken into consideration. For more information on Video Mode Interface Timing Legend, see Specification for Display Serial Interface (DSI®).
2. The MIPI DSI Transmitter IP supports Non-Burst Mode with Sync Events.

2. DSI Physical Layer

This section briefs about the physical layer used in DSI.

Information is transferred between the host processor and peripheral (display module) using one or more serial data signals and accompanying serial clock. The action of sending the high-speed serial data across the bus is called a High Speed (HS) transmission or burst. Between transmissions, a differential data signal or a lane goes to a Low-Power State (LPS). Interfaces must be in LPS when they are not actively transmitting or receiving the high-speed data. The following figure shows the basic structure of a HS transmission. N is the total number of bytes sent during transmission.

Figure 2-1. Basic HS Transmission



SOT: Start Of Transmission

EOT: End Of Transmission

D-PHY low-level protocol specifies a minimum data unit of one byte, and a transmission contains an integer number of bytes. For more information, see MIPI Alliance Specification for D-PHY.

3. General Packet Structure

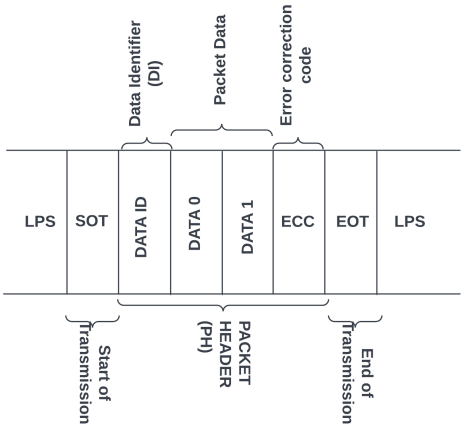
Two packet structures are defined for a low-level protocol communication.

- Short Packets
- Long Packets

3.1 Short Packet

A short packet contains an 8-bit Data ID followed by two command or data bytes and an 8-bit ECC. A packet footer must not be present. Short packet must be four bytes in length. The following figure shows the structure of a short packet.

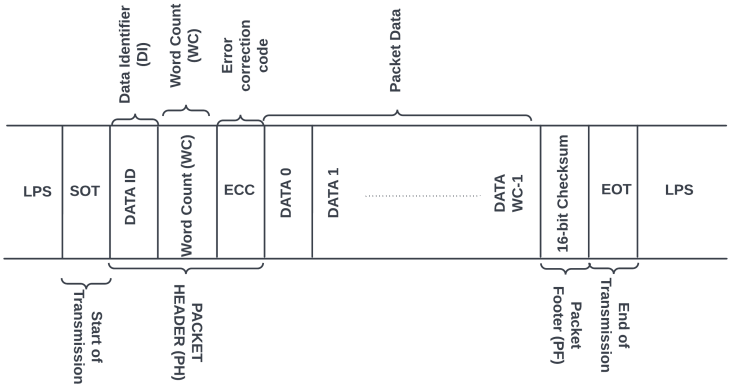
Figure 3-1. Short Packet Structure



3.2 Long Packets

Long packet consists three elements: a 32-bit Packet Header (PH), an application specific data payload of word count no of bytes, and a 16-bit Packet Footer (PF). PH is composed of three elements: an 8-bit Data Identifier ([7:6] - Virtual channel no and [5:0] - Data type), a 16-bit word count, and an 8-bit ECC. PF has a 16-bit checksum (CRC) element. Long packets can be from 6 to 65541 bytes in length. The following figure shows the structure of a long packet.

Figure 3-2. Long Packet Structure



4. Processor to Peripheral Data Types

The following table lists the supported DSI Data types from processor to display module.

Table 4-1. Processor to Peripheral Data Types

Data Type	Description	Packet	DSI Mode
0x01	Sync Event - V sync Start	Short	Video
0x11	Sync Event - V sync End	Short	Video
0x21	Sync Event - H sync Start	Short	Video
0x31	Sync Event - H sync End	Short	Video
0x02	Color Mode (CM) OFF	Short	Video
0x12	Color Mode (CM) ON	Short	Video
0x22	Shut Down Peripheral	Short	Video
0x32	Turn ON Peripheral	Short	Video
0x05	DCS short Write, no parameters	Short	Command
0x15	DCS short Write, 1 parameter	Short	Command
0x29	Generic Long Packet	Long	Command
0x39	DCS Long Write/LUT Write	Long	Command
0x2C	Packed pixel stream 16-bit YCbCr 4:2:2 format	Long	Video
0x3E	Packed pixel stream 24-bit RGB 8:8:8 format	Long	Video

For more information on Data types, see Specification for Display Serial Interface (DSI®).

5. DCS Commands

The following table lists the supported DCS commands.

Table 5-1. DCS Command List

Command	Hex Code	Description	Number of Parameters
exit_sleep_mode	0x11	Power for the display panel is ON.	0
set_display_on	0x29	Shows the image on the display device.	0
set_display_off	0x28	Blanks the display.	0
set_display_brightness	0x51	Selects Display Brightness Level.	1 or 2
write_control_display	0x53	Writes control mode of display brightness.	1
write_memory_start	0x2C	Transfers image data from the Host Processor to the peripheral.	Variable
write_memory_continue	0x3C	Transfers image information from the Host Processor interface to the peripheral from the last written location.	Variable

For more information on DCS command, see Specification for Display Command Set (DCSSM)

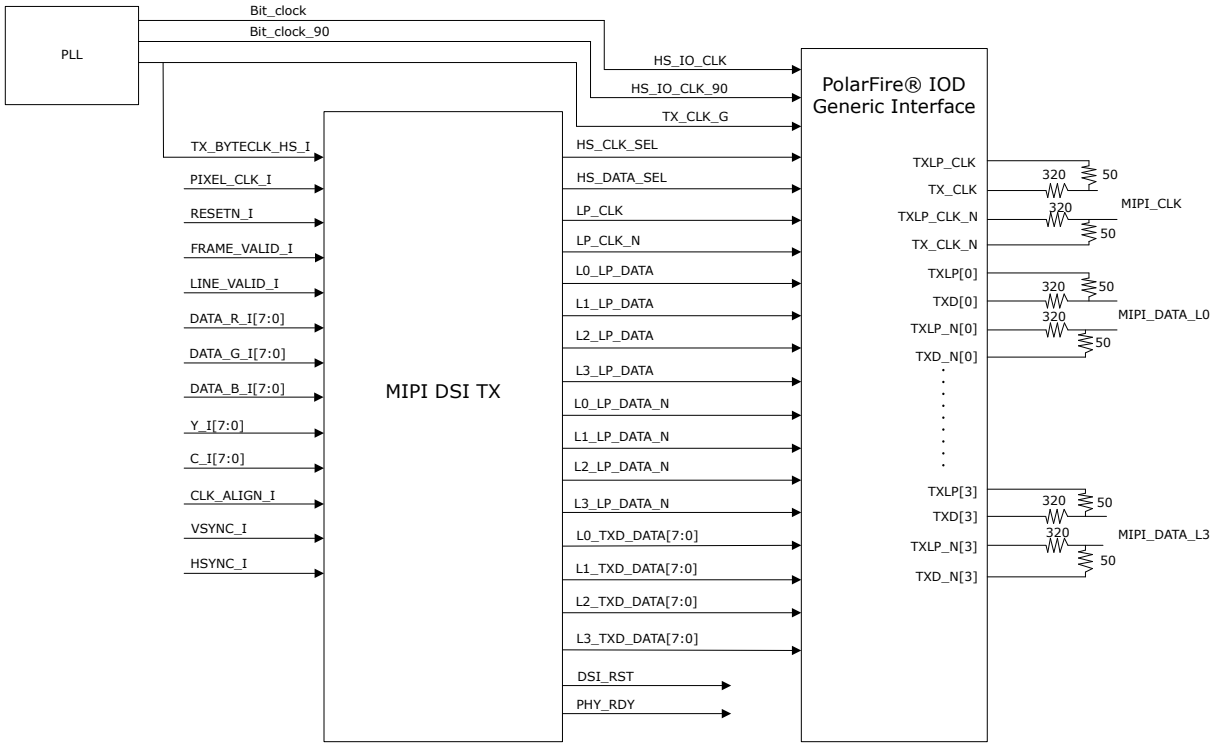
6. Hardware Implementation

The following illustration shows the MIPI DSI2 Transmitter solution that contains MIPI DSI TX IP. This IP is used in conjunction with the PolarFire MIPI IOD generic interface block and PLL. The illustration shows the pin connections from the MIPI DSI TX IP to the PolarFire IOD. In clocking architecture, DSI IP needs the following clocks:

- **Pixel clk**: Parallel video pixel clock
- **TxByteClkHs_I**: Byte clk (3/4th of pixel clk for four lane configuration and RGB-888 data format)
- **Bitclk**: High-speed serial clock for PF IOD
- **Bitclk90**: High-speed 90° shifted serial clock for PF IOD

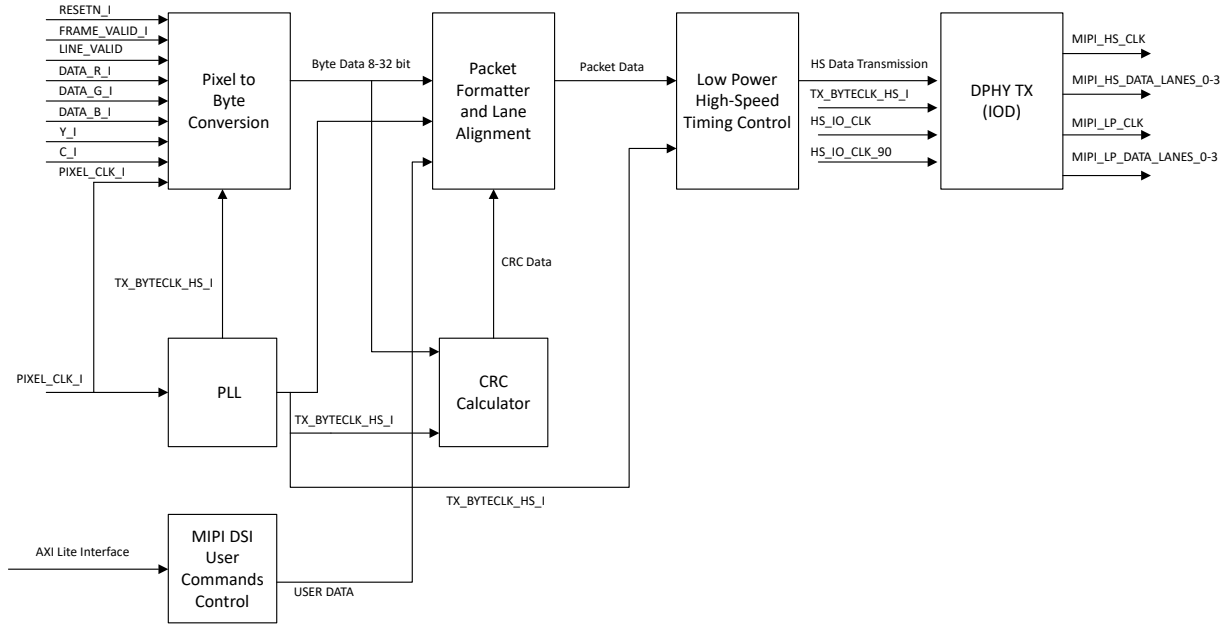
A PLL is required to generate the Byte clock. The PLL is configured to produce the Byte clock, MIPI high-speed Bitclk, and 90° phase shifted bitclk. An external resistor network is needed to accommodate Low Power (LP) and High Speed (HS) mode transitioning on the same signal pairs, see the following figure. It is also needed to set the voltage swing to 200 mV during HS clock and data transfers.

Figure 6-1. Architecture of MIPI DSI Transmitter Solution



The following figure shows the block diagram of MIPI DSI Transmitter core.

Figure 6-2. Implementation of MIPI DSI Transmitter Core



6.1 Design Description

This section describes the different internal modules of the MIPI DSI transmitter core.

6.1.1 Pixel to Byte Conversion

The DSI lanes transmit data using a high-speed bit clock, though the video data is generated using a pixel clock. The video is transmitted on the lanes in the format of bytes. The DSI IP contains a module to convert the incoming pixel data to bytes. You are expected to transmit the pixels along with the control signals LINE_VALID_I and FRAME_VALID_I. An internal clock crossing FIFO is used to convert the incoming data from pixel clock to byte clock domain. The pixel to byte conversion module also generates the byte enable signal, which indicates the valid byte data.

There are some initial settings (see 6.1.2. Packetizer), where the DSI IP is required to complete before accepting video data from the video generator. There is a PHY_RDY signal from the DSI IP, which must be used to enable the video timing generator. Sending a video to the DSI IP before this ready signal is active might get shifted or rolling image outputs.

6.1.2 Packetizer

The packetizer module in DSI TX IP implements a packet forming state machine. The packets contain header and payload data. In each packet, it appends ECC in headers and CRC in the payload data. It generates long and short packets as required by the Display Command Set (DCS). In initial states, this state machine generates the following packets:

- Display sleep-exit packet
- Display switch-on packet
- Display default brightness and backlight on packets

After the basic settings are done, the packetizer is ready for sending a video stream to a display. At this time, it generates a PHY_RDY signal, which is used to enable a video timing generator. For Command mode display modules, the packetizer writes this video data to the right-hand side of the display RAM. This process is followed for each line in each frame. The memory start command and memory continue commands are used as per the DSI specification.

- Write memory start (DCS command 0x2C)
- Write memory continue (DCS command 0x3C)

The packetizer module also writes new brightness and backlight values to the display registers. These new values are given by you using a command, address, and data interface defined in different sections on this document using AXI4 LITE Interface. It checks for these values in every frame and updates during the vertical blanking period.

Figure 6-3. Packetizer Output in Command Mode

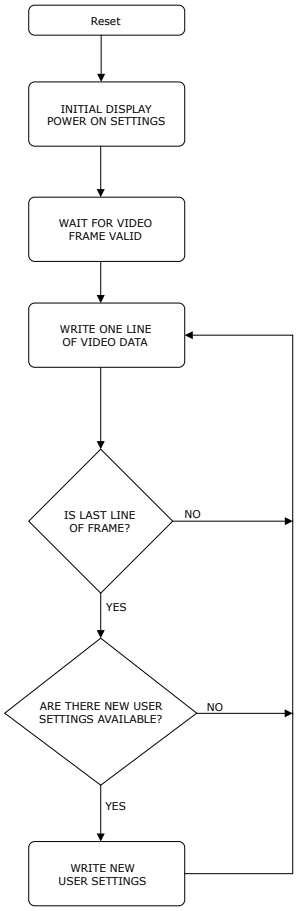
DATAID 0X39	WC[7:0]	WC[15:8]	ECC	DCS CMD	PAYLOAD DATA	CRC[7:0]	CRC[15:8]

For Video mode display modules, the packetizer writes this video data in real time. The packetizer sends Sync Events along with Payload data as per the DSI specification. In initial states, this state machine generates the following packets:

- Display sleep-exit packet
- Display switch-on packet
- Display default brightness and backlight on packets
- Manufacturer Command Access Protect and Interface settings

The packetizer module also sends Shutdown and Turn ON commands, Color Mode ON/OFF Commands, which are given by you using AXI4 LITE Interface. It checks for these values in every frame and updates during the vertical blanking period.

Figure 6-4. Sequence for HS Data Generation



6.1.3 PLL

PIXEL_CLK_I is the input clock with which incoming pixels are sampled. PLL is used to generate the Byte clock (TX_BYTECLK_HS_I), and bit clocks are used by the MIPI DPHY block (PolarFire IOD). TX_BYTECLK_HS_I must be configured such that the output MIPI DSI compliant packets sent on the interface are sampled.

The following equations show the relation between PIXEL_CLK_I and TX_BYTECLK_HS_I depending on the number of lanes configured.

- TX_BYTECLK_HS_I = (PIXEL_CLK_I × Bits per pixel)/(Number of Lanes × 8)
- MIPI bit clock = 4 × TX_BYTECLK_HS_I
- Bits per pixel = 24 bits for RGB 8:8:8 and 16 bits for YCbCr 4:2:2
- Number of lanes = 4

Two serial MIPI bit clocks are required for 0° and 90° phase shifted.

6.1.4 Low Power/High-Speed

After powering up, the DSI IP must complete the initialization sequence of the display. The Low-Power module in the IP follows the DPHY specification and takes all the clock and data lanes from low power mode to high-speed mode. Currently, all the transactions are done in high-speed mode. Transition to high-speed mode follows the following sequence: LP-11, LP-01, LP-00, and HS0/1. It indicates the HS request path and following the timing based on MIPI DPHY Specification version 1.1. Once in high-speed mode, the clock always remains in that mode. The data lanes move to the high-speed mode when there is data to send, and they return to low power mode when not sending DSI packets.

An example is when in the video blanking period, the data lanes remain in low power mode. The Low-Power module generated SoT and EoT sequences as per the DPHY specification. This IP does not support LP requests, Escape mode, and Turn around modes.

6.1.5 DPHY TX

This module uses PolarFire IOD generic blocks to convert Byte data to serial data. A gearing ratio of four is used to convert the parallel data to serial data. It generates both HS and LP signals (for both clock and data). It also switches between HS and LP modes using the HS_CLK_SEL and HS_DATA_SEL signals.

In the PF IOD configuration, you must specify various parameters as required by the supported data rates by the display.

6.1.6 CRC Calculator

This module uses the bytes generated from the pixel to byte conversion module and calculates the 16-bit CRC for the generated bytes. This 16-bit CRC is sent to the Packetizer, which appends the value at the end of the long packet.

6.1.7 User Control

DSI IP has a user control module. The user control module is controlled by using AXI4 LITE Interface and works on TX_BYTECLK_HS_I. In Command Mode, this module provides a user interface to write brightness, backlight, and display on-off commands to the display. In Video mode, this module provides a user interface to write initial display register settings after device power up, Shutdown, Turn ON, and Color Mode ON/OFF commands to the display. Corresponding register details and waveform examples are shown as follows for clarity.

Table 6-1. Register Details of a User Control

Register Address	Register Name	Description	Register Data Details
0x80	User_Write_Control	This register is used to send write request, Single Register Write Done, and Register Configuration done (after all registers are configured) to MIPI DSI TX IP	Bit 0 = 1: Write Request Bit 1 = 1: Single Register Write Done Bit 2 = 1: Registers Configuration Done Bits 31:3 = Reserved

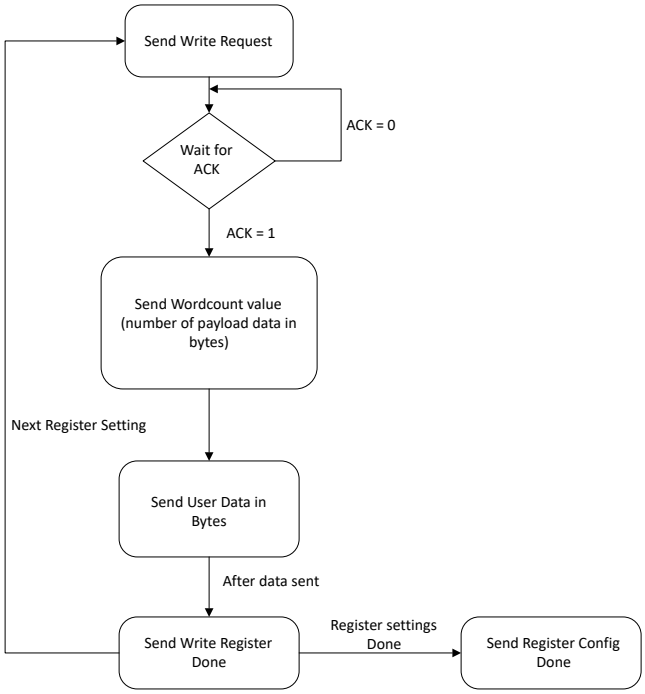
.....continued			
Register Address	**Register Name**	**Description**	**Register Data Details**
0x84	User_Word_Count	This register is used to send Word count value to MIPI DSI TX IP	Bits 15:0 = Word count Value Bits 31:16 = Reserved
0x88	User_Data_Control	This register is used to send User data in bytes. You can send 4 bytes in a single clock,	Bits 31:0 = User Data
0x8C	User_Display_ON_OFF	This register is used to make a display ON or OFF in Command mode display modules	Bit 0 = 1: Display ON Bit 0 = 0: Display OFF
0x90	User_Brightness_Control	This register is used to change the brightness level of a display module in Command mode	Bit 7:0: min Brightness = 0x00 Bit 7:0: max Brightness = 0xFF Bits 31:8 = Reserved
0x94	User_Back_Light_Control	This register is used to control back light of a display module in Command mode	Bit 7:0: Back light value Bits 31:8 = Reserved
0x98	User_TON_OFF	This register is used to make a display ON or OFF in Video mode display modules	Bit 0 = 1: Turn ON Display Bit 0 = 0: Shutdown Display
0x9C	User_CM_ON_OFF	This register is used to make a color mode ON or OFF in Video mode display modules	Bit 0 = 1: Color Mode ON Bit 0 = 0: Color Mode OFF

Important:

1. Default AXI4 LITE Interface Data width is 32.
2. Unused Register Data bits: Reserved

The following flowchart shows the sequence for a user register write operation.

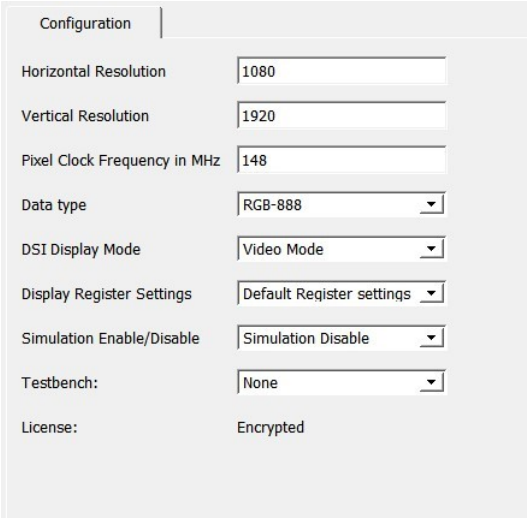
Figure 6-5. Sequence of a User Register Write Operation



6.2 IP Configurator

The following figure shows the MIPI DSI TX IP Configurator.

Figure 6-6. MIPI DSI TX IP Configurator



The following table lists the configuration parameters used in the hardware implementation of the MIPI DSI transmitter block. These are generic parameters and can vary based on the application requirements.

Table 6-2. Configuration Parameters

Name	Description
Horizontal Resolution	Active Horizontal Resolution

.....continued	
Name	**Description**
Vertical Resolution	Active Vertical Resolution
Pixel Clock Frequency in MHz	Input Pixel clock frequency
Data type	Pixel Data type Supports RGB-888 and YCbCr-422
DSI Display Mode	Supports Command mode and Video mode
Display Register Settings	Supports Initial Default Register settings or User Register Settings
Simulation Enable/Disable	Simulation Enable and Disable Simulation Enable is used to reduce the time of initial power up settings Simulation Disable is used for Hardware
Testbench	User Testbench is supported only for RGB 888 and Video mode

6.3 Inputs and Outputs

The following table lists the input and output ports of the MIPI DSI TX configuration parameters.

Table 6-3. Input and Output Ports of the MIPI DSI Transmitter

Signal Name	Direction	Width in Bits	Description
PIXEL_CLK_I	Input	1	Input clock with which incoming pixels are sampled
TX_BYTECLK_HS_I	Input	1	TX Byte clock (gearing ratio 4) This clock must be configured such that the pixels sent on the MIPI DSI interface are sampled according to it
RESETN_I	Input	1	Active low asynchronous reset signal to design
FRAME_VALID_I	Input	1	Asserts high for every valid frame
LINE_VALID_I	Input	1	Asserts high when the valid packet is available
VSYNC_I	Input	1	Vertical Sync Input
HSYNC_I	Input	1	Horizontal Sync Input
DATA_R_I	Input	8	Input Pixel Data Red, valid when Data type is RGB-888
DATA_G_I	Input	8	Input Pixel Data Green, valid when Data type is RGB-888
DATA_B_I	Input	8	Input Pixel Data Blue, valid when Data type is RGB-888
Y_I	Input	8	Input Luma Pixel, valid when Data type is YCbCr-422
C_I	Input	8	Input Chroma Pixel, valid when Data type is YCbCr-422
DSI_RST	Output	1	Active low reset to the display device
PHY_RDY	Output	1	Asserts when DSI IP is ready to take the video data
HS_CLK_SEL	Output	1	Selects HS clock or LP clock mode (only supports continuous clock)
HS_DATA_SEL	Output	1	Selects HS data or LP data mode
LP_CLK	Output	1	Low power clock (P side)
LP_CLK_N	Output	1	Low power clock (N side)

.....continued			
Signal Name	**Direction**	**Width in Bits**	**Description**
L0_LP_DATA	Output	1	Low power data (P side) for Lane 0
L1_LP_DATA	Output	1	Low power data (P side) for Lane 1
L2_LP_DATA	Output	1	Low power data (P side) for Lane 2
L3_LP_DATA	Output	1	Low power data (P side) for Lane 3
L0_LP_DATA_N	Output	1	Low power data (N side) for Lane 0
L1_LP_DATA_N	Output	1	Low power data (N side) for Lane 1
L2_LP_DATA_N	Output	1	Low power data (N side) for Lane 2
L3_LP_DATA_N	Output	1	Low power data (N side) for Lane 3
L0_TXD_DATA	Output	8	Lane 0 Transmit Byte
L1_TXD_DATA	Output	8	Lane 1 Transmit Byte
L2_TXD_DATA	Output	8	Lane 2 Transmit Byte
L3_TXD_DATA	Output	8	Lane 3 Transmit Byte

6.4 AXI4 LITE Interface Signals

The following table lists the AXI4 LITE Interface signals description.

Table 6-4. AXI4 LITE Interface Signals

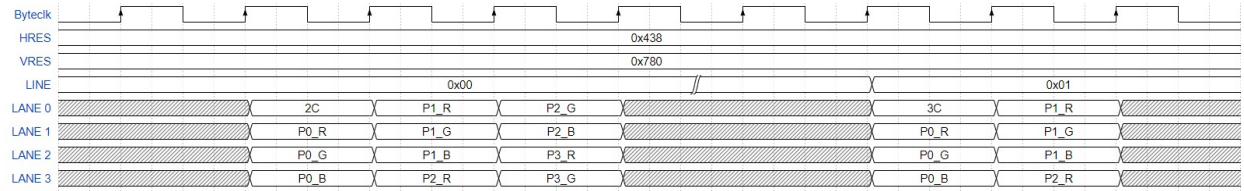
Port Name	Type	Width in Bits	Description
AXI_RESETN_I	Input	1	AXI4-Lite asynchronous reset signal
AXI_CLK_I	Input	1	AXI4-Lite clock signal
AXI_AWVALID_I	Input	1	AXI4-Lite Write address Valid
AXI_AWADDR_I	Input	32	AXI4-Lite Write address
AXI_AWPROT_I	Input	3	AXI4-Lite Protection type
AXI_AWREADY_O	Output	1	AXI4-Lite Write address ready
AXI_WDATA_I	Input	32	AXI4-Lite Write Data
AXI_WVALID_I	Input	1	AXI4-Lite Write Data Valid
AXI_WREADY_O	Output	1	AXI4-Lite Write Data Ready
AXI_BREADY_I	Input	1	AXI4-Lite Write Response Ready
AXI_BVALID_O	Output	1	AXI4-Lite Write Response Valid
AXI_BRESP_O	Output	2	AXI4-Lite Write Response
AXI_ARVALID_I	Input	1	AXI4-Lite Read Address Valid
AXI_ARADDR_I	Input	32	AXI4-Lite Read Address
AXI_ARREADY_O	Output	1	AXI4-Lite Read Address Ready
AXI_RREADY_I	Input	1	AXI4-Lite Read Data Ready
AXI_RDATA_O	Output	32	AXI4-Lite Read Data
AXI_RVALID_O	Output	1	AXI4-Lite Read Data Valid

.....continued			
Port Name	**Type**	**Width in Bits**	**Description**
AXI_RRESP_O	Output	2	AXI4-Lite Read Response

7. Timing Diagrams

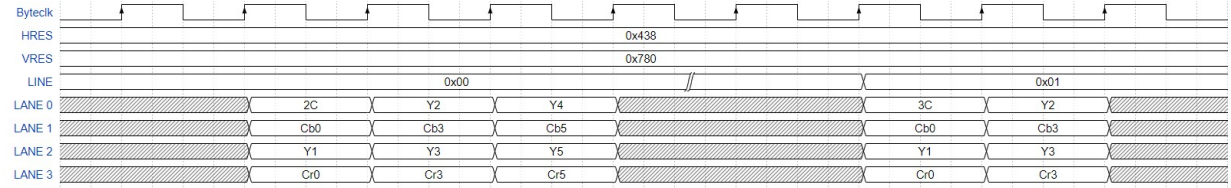
The following figure shows a portrait 1080 × 1920 display of 24-bit RGB data packets using long packets in Command Mode.

Figure 7-1. 24-Bit RGB 8:8:8 Data Packets Using Long Packets in Command Mode



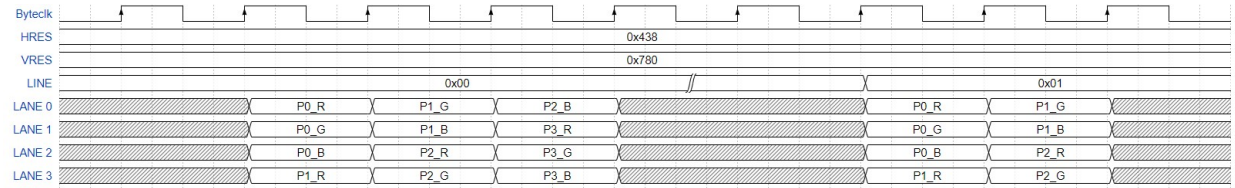
The following figure shows a portrait 1080 × 1920 display of 16-bit YCbCr 4:2:2 data packets using long packets in Command Mode.

Figure 7-2. 16-Bit YCbCr 4:2:2 Data Packets Using Long Packets in Command Mode



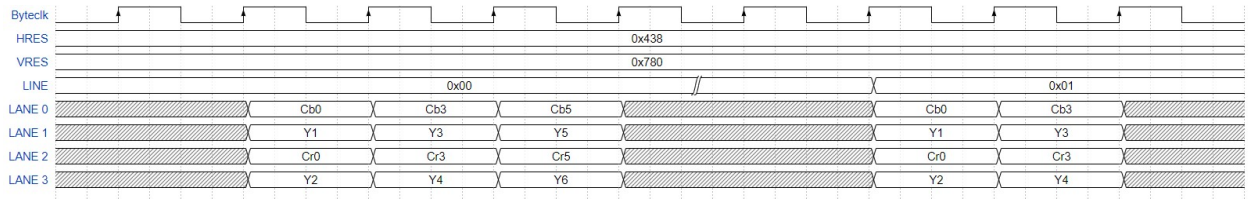
The following figure shows a portrait 1080 × 1920 display of 24-bit RGB data packets using long packets in Video Mode.

Figure 7-3. 24-Bit RGB 8:8:8 Data Packets Using Long Packets in Video Mode



The following figure shows a portrait 1080 × 1920 display of 16-bit YCbCr 4:2:2 data packets using long packets in Video Mode.

Figure 7-4. 16-Bit YCbCr 4:2:2 Data Packets Using Long Packets in Video Mode



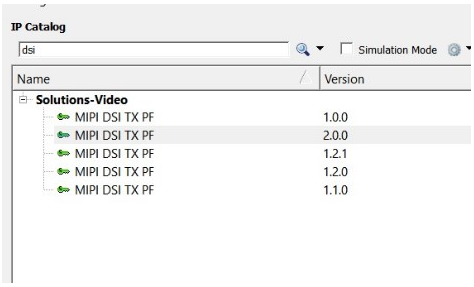
8. Testbench

Testbench is provided to check the functionality of the MIPI DSI Transmitter IP for 24-bit RGB 8:8:8 in Video mode. Simulation uses a 1080 × 1920 image in 24-bit RGB 888 format for Video mode.

To simulate the core using testbench, perform the following steps:

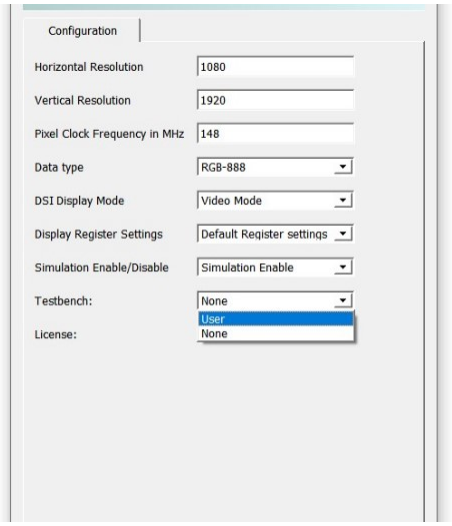
1. Launch the Libero SoC software, navigate to **Catalog** > **View** > **Windows** > **Catalog**, and then expand **Solutions** > **Video**. Double click on **MIPI DSI TX** and click **OK**.

   Figure 8-1. Libero Catalog



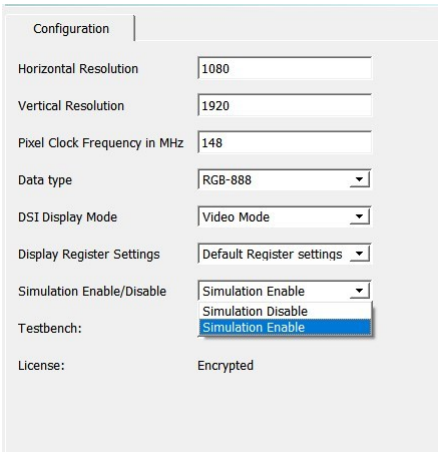
2. Select **Testbench as User**, as shown in the following figure.

   Figure 8-2. IP Configurator for Testbench



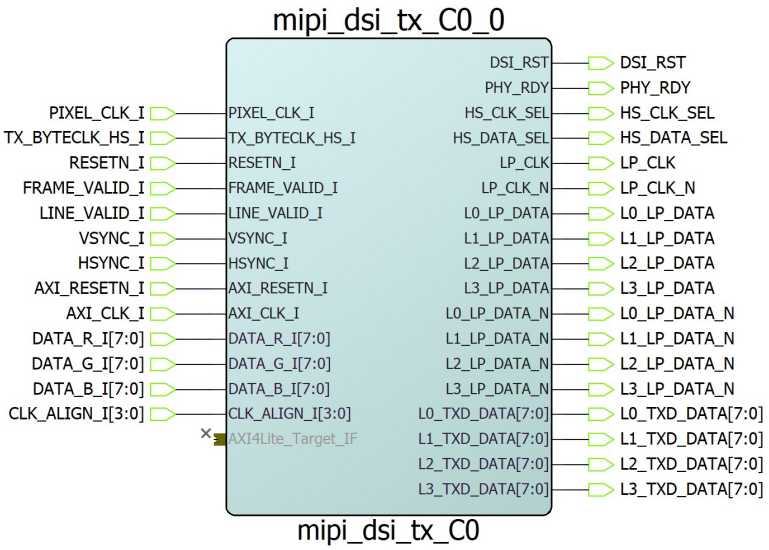
3. Select **Simulation Enable/Disable** parameter as Simulation Enable and then click **OK**.

   Figure 8-3. IP Configurator Simulation Parameter



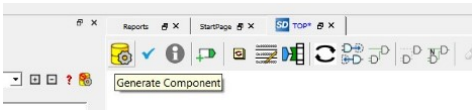
4. Promote the Top level IP ports as shown in the following figure and make AXI4 LITE Interface as Mark Un-used.

Figure 8-4. Top Level Ports of MIPI DSI Transmitter IP



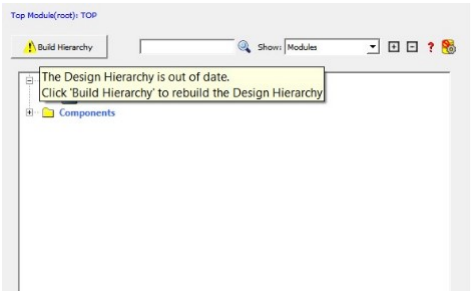
5. Click **Generate Component**.

Figure 8-5. Generate Component



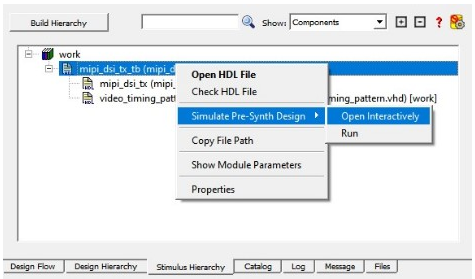
6. Click **Build Hierarchy**.

Figure 8-6. Build Hierarchy



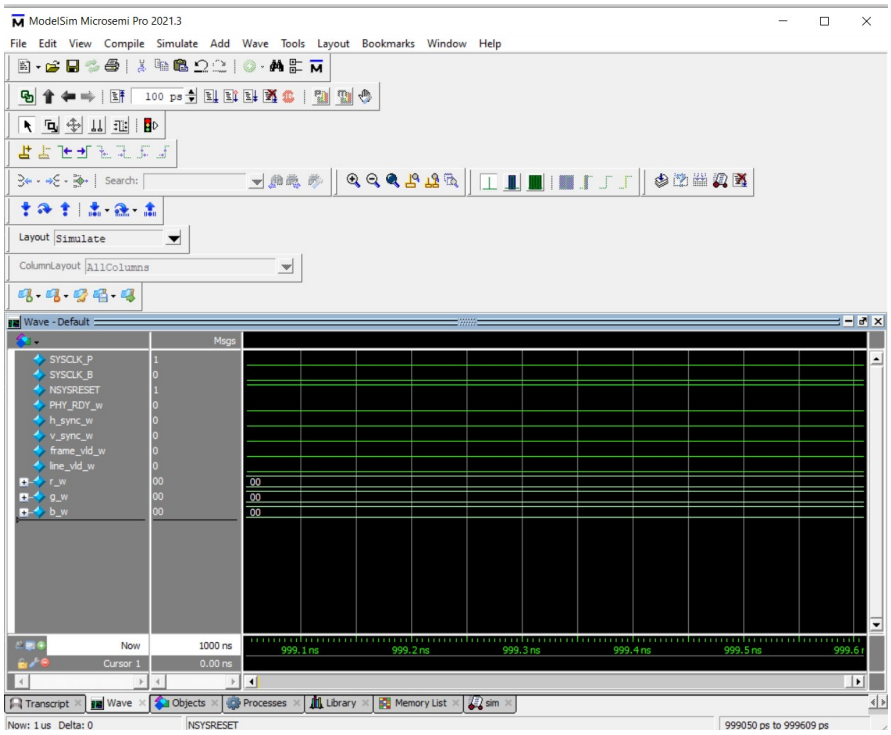
7. Go to the **Simulation Hierarchy** tab and right click **mipi_dsi_tx_tb** and select **Simulate Pre-synth Design** > **Open Interactively**.

Figure 8-7. Running Simulation from Libero SoC Software



The **Modelsim Simulation** window is displayed.

Figure 8-8. Modelsim Simulation Window



Important: If the simulation is interrupted due to the run time limit specified in the DO file, use the run-all command to complete the simulation.

9. License

The core is license locked for clear text RTL. It supports the generation of Encrypted RTL for the Verilog version of core with no license.

10. Resource Utilization

The following table lists the resource utilization of a sample MIPI DSI transmitter core implemented in a PolarFire MPF300T-1FCG1152I device for 24-bit RGB-888 and four lanes configuration in Video Mode.

Table 10-1. Resource Utilization of the MIPI DSI Transmitter

Element	Usage
Fabric DFFs	1136
Fabric LUTs	763
LSRAM	10

11. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 11-1. Revision History

Revision	Date	Descriptions
A	11/2022	The following is the list of changes made in revision A of the document: • The document was migrated to the Microchip template • Added the Video Mode section. • Added the General Packet Structure section. • Added Table 4-1 for Processor to Peripheral Data Types. • Added Table 5-1 for DCS Commands. • Updated Figure 6-1. • Updated Figure 6-2. • Modified the Register Map Address in Table 6-1. • Updated Configuration Parameters in Table 6-2. • Updated Table 6-3. • Added AXI4 LITE support for Display Register Configuration in 6.1.7. User Control. • Added 8. Testbench.
2.0	—	Added support for Packed Pixel Stream 16-bit YCbCr 4:2:2 format.
1.0	—	Initial release.

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ISBN: 978-1-6683-1527-9

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