Application Note

AT91SAM ARM-based Embedded MPU

Gigabit Ethernet Implementation on SAMA5D3 Series

1. Introduction

The SAMA5D3 series is a member of the Atmel® microprocessor family which is based on the ARM® Cortex™-A5 processor core.

This Application Note outlines the Gigabit Ethernet function embedded on SAMA5D3 Series.

2. Associated Documentation

Before going further into this document, please refer to the latest documentation for the corresponding SAMA5D3 devices available on the Atmel® web site at http//:www.atmel.com.

- SAMA5D3 Series Datasheet: lit° 11121
- SAMA5D3-EK User Guide: lit° 11180

3. Gigabit Ethernet Implementation on SAMA5D3 Series

- Compatible with IEEE Standard 802.3
- 10, 100 and 1000 Mbit/s Operation
- Full and Half Duplex Operation at All Three Speeds of Operation
- Statistics Counter Registers for RMON/MIB
- MII/GMII/RGMII Interface to the Physical Layer
- RMII is Not Supported
- Integrated Physical Coding
- Direct Memory Access (DMA) Interface to External Memory
- Support for up to Eight Priority Queues in DMA
- Programmable Burst Length and Endianism for DMA
- Interrupt Generation to Signal Receive and Transmit Completion, or Errors
- Automatic Pad and Cyclic Redundancy Check (CRC) Generation on Transmitted Frames
- Frame Extension and Frame Bursting at 1000 Mbit/s in Half Duplex Mode
- Automatic Discard of Frames Received with Errors
- Receive and Transmit IP, TCP and UDP Checksum Offload. Both IPv4 and IPv6 Packet Types Supported
- Address Checking Logic for Four Specific 48-bit Addresses, Four Type IDs, Promiscuous Mode, Hash Matching of Unicast and Multicast Destination Addresses and Wake-on-LAN
- Management Data Input/Output (MDIO) Interface for Physical Layer Management

- Support for Jumbo Frames up to 10240 Bytes
- Full Duplex Flow Control with Recognition of Incoming Pause Frames and Hardware Generation of Transmitted Pause Frames
- Half Duplex Flow Control by Forcing Collisions on Incoming Frames
- Support for 802.1Q VLAN Tagging with Recognition of Incoming VLAN and Priority Tagged Frames
- Support for 802.1Qbb Priority-Based Flow Control
- Programmable Inter Packet Gap (IPG) Stretch
- Recognition of IEEE 1588 PTP Frames
- IEEE 1588 Time Stamp Unit (TSU)
- Support for 802.1AS Timing and Synchronization

4. Signal Description and Connection

The GMAC includes the following signal interfaces:

- GMII, MII, and RGMII to an external PHY
- MDIO interface for external PHY management
- Slave APB interface for accessing GMAC registers
- Master AHB interface for memory access

Table 4-1. GMAC Connections in Different Modes

Signal Name	Function	MII	GMII	RGMII
GTXCK	Transmit Clock or Reference Clock	TXCK	Not Used	TXCK
G125CK	125 MHz input Clock	Not Used	125 MHz Ref Clk	125 MHz Ref Clk
G125CKO	125 MHz output Clock	Not Used	TXCK	Not Used
GTXEN	Transmit Enable	TXEN	TXEN	TXCTL
GTX[7..0]	Transmit Data	TXD[3:0]	TXD[7:0]	TXD[3:0]
GTXER	Transmit Coding Error	TXER	TXER	Not Used
GRXCK	Receive Clock	RXCK	RXCK	RXCK
GRXDV	Receive Data Valid	RXDV	RXDV	Not Used
GRX[7..0]	Receive Data	RXD[3:0]	RXD[7:0]	RXD[3:0]
GRXER	Receive Error	RXER	RXER	RXCTL/RXDV
GCRS	Carrier Sense and Data Valid	CRS	CRS	Not Used
GCOL	Collision Detect	COL	COL	Not Used
GMDC	Management Data Clock	MDC	MDC	MDC
GMDIO	Management Data Input/Output	MDIO	MDIO	MDIO

Figure 4-1. Connection between Ethernet PHY and Ethernet MAC in the MII/GMII Mode.

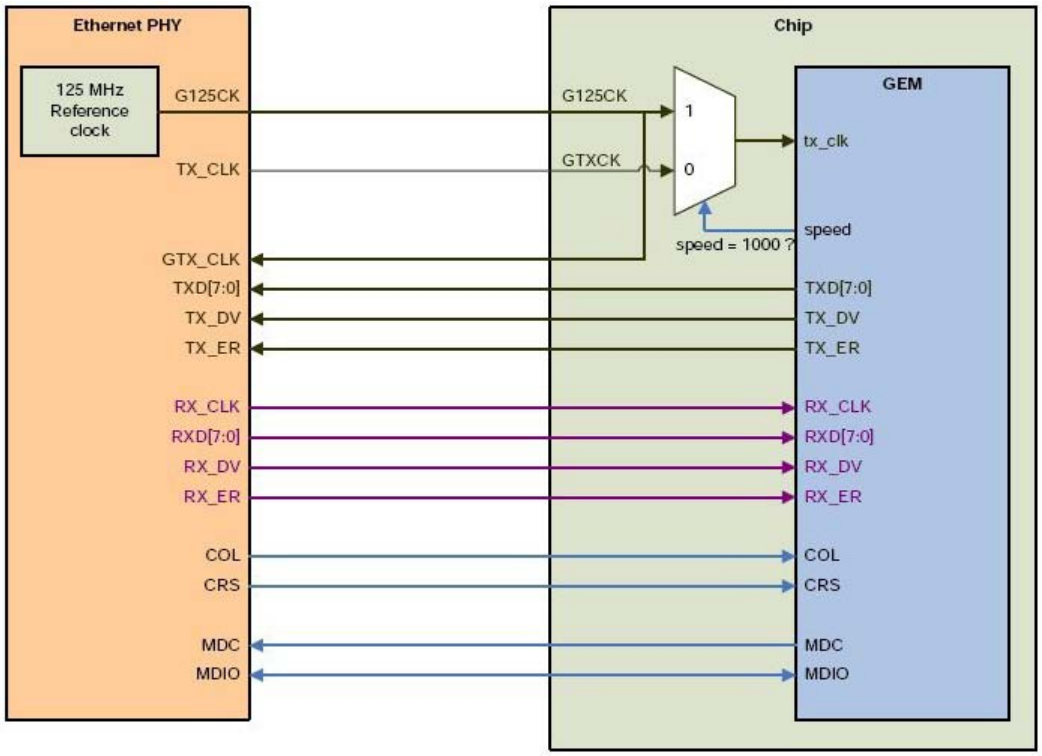
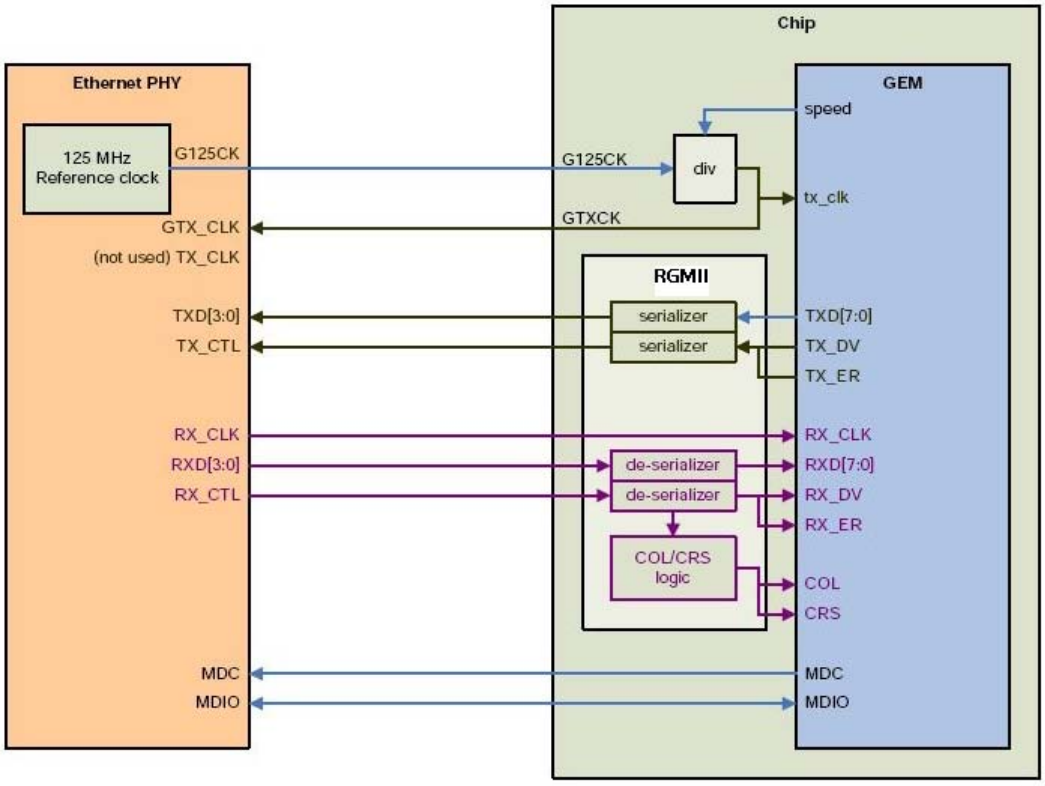


Figure 4-2. Connection between Ethernet PHY and Ethernet MAC in the RGMII Mode



5. MII: Media Independent Interface

The MII bus (standardized by IEEE 802.3) is a generic bus that connects different types of PHYs to the same network controller (MAC). The network controller may interact with any PHY using the same hardware interface, independent of the media the PHYs are connected to. The MII transfers data using 4bit words (nibble) in each direction, clocked at 25 MHz to achieve 100 Mbit/s speed.

The basic operation of data transmission is that the enable signal (TXEN) is set active to indicate start of frame and until it is completed. Then the clock signal (TXCLK) is set active for every group of bits (TXD[3:0]), at 2.5 MHz for 10 Mbit/s mode and 25 MHz for 100 Mbit/s mode. When the reception is valid, the RXDV signal goes active when the frame starts and throughout the frame duration. Then the clock signal (RXCLK) goes active for every group of bits (RXD[3:0]). For the shortest possible frame this means ~130 clocks. Any frame transferred begins with sync bits before the data payload. At power-up, the PHY adapts to whatever it is connected to, unless you alter settings via the MDIO interface.

The following table describes MII signals:

Table 5-1. MII Signals

Channel	Signal	Direction(1)	Description
PHY to MAC	TXCK	IN	Transmit clock (generated by the PHY): 2.5 MHz for 10 Mbit/s and 25 MHz for 100 Mbit/s
	TXD[4:0]	OUT	Data to be transmitted
	TXEN	OUT	Transmitter enable
	TXER	OUT	Transmitter error (used to corrupt a packet)
MAC to PHY	RXCK	IN	Received clock
	RXD[4:0]	IN	Received data
	RXDV	IN	Signifies that received data is valid
	RXER	IN	Signifies that received data has errors
Carrier and Collision	CRS	IN	Carrier Sense (half-duplex connections only)
	COL	IN	Collision Detect (half-duplex connections only)
PHY Management	MDCK	OUT	
	MDIO	INOUT	

Note: 1. Direction is defined from the chip side: IN = PHY to MAC, OUT = MAC to PHY.

6. GMII: Gigabit Media Independent Interface

GMII is an addendum to MII interface. It has been added to handle Gigabit Ethernet 1000 Mbit/s transfer rate. GMII does not replace MII, as it is not specified to work with 10 and 100 Mbit/s transfer rates. Therefore, for 10 or 100 Mbit/s transfer rates, MII interface is used instead of GMII.

One of the major differences between MII and GMII is that TX clock (MAC to PHY clock) is not provided by the PHY anymore, it is the MAC that provides the clock. Then each of RX and TX channels provides its own clock. This prevents timing closure issues, as Gigabit mode frequency clock is 125 MHz (4 ns period). Four additional bits have been added on Data signals in order to reach the 1000 Mbit/s rate (frequency is 5 times the one of 100 Mbit/s rate, and data bus width is doubled, then the factor of 10 is reached).

The following table describes GMII signals:

Table 6-1. GMII Signals

Channel	Signal	Direction[1]	Description
PHY to MAC	GTXCK	OUT	Transmit clock for 1000 Mbit/s: 125 MHz
	TXCK	IN	Transmit clock (generated by the PHY for MII compatibility): 2.5 MHz for 10 Mbit/s and 25 MHz for 100 Mbit/s
	TXD[7:0]	OUT	Data to be transmitted (4 bits more than MII)
	TXEN	OUT	Transmitter enable
	TXER	OUT	Transmitter error (used to corrupt a packet)
MAC to PHY	RXCK	IN	Received clock
	RXD[7:0]	IN	Received data (4 bits more than MII)
	RXDV	IN	Signifies that received data is valid
	RXER	IN	Signifies that received data has errors
Carrier and Collision	CRS	IN	Carrier Sense (half-duplex connections only)
	COL	IN	Collision Detect (half-duplex connections only)
PHY Management	MDCK	OUT	SMI clock
	MDIO	INOUT	SMI data

Note: 1. Direction is defined from the chip side: IN = PHY to MAC, OUT = MAC to PHY.

7. RGMII: Reduced Gigabit Media Independent Interface

RGMII uses half the number of data pins used in the GMII interface. This reduction is achieved by clocking data on both the rising and the falling edges of the clock, and by eliminating non-essential signals (carrier sense and collision indication).

Thus RGMII consists only of: RXC, RD[3:0], RX_CTL, TXC, TXD[3:0], and TX_CTL (12 pins, as opposed to 24 pins for GMII).

Unlike MII, the transmit clock signal is always provided by the MAC on the TXC line, rather than being provided by the PHY for 10/100 Mbit/s operation and by the MAC at 1000 Mbit/s.

RGMII supports Ethernet speeds of 10 Mbit/s, 100 Mbit/s and 1000 Mbit/s.

The following table describes RGMII signals:

Table 7-1. RGMII Signals

Channel	Signal	Direction[1]	Description
Clock	GTXCK	IN	125 MHz reference clock
PHY to MAC	TX_CLK / GTXCKO	OUT	Transmit clock (generated by the MAC with master clock GTXCK): 2.5 MHz for 10 Mbit/s, 25 MHz for 100 Mbit/s and 125 MHz for 1000 Mbit/s
	TXD[3:0]	OUT	Data to be transmitted
	TXCTL	OUT	Transmitter enable / Transmitter error
MAC to PHY	RXC	IN	Received clock: 2.5 MHz for 10 Mbit/s, 25 MHz for 100 Mbit/s and 125 MHz for 1000 Mbit/s
	RXD[3:0]	IN	Received data
	RXCTL	IN	Signifies that received data has errors
PHY Management	MDCK	OUT	SMI clock
	MDIO	INOUT	SMI data

Note: 1. Direction is defined from the chip side: IN = PHY to MAC, OUT = MAC to PHY.

8. Routing Considerations

The user should refer to the design and layout guidelines of the PHY provider.

8.1 SAMA5D3 Example

This example shows how SAMA5D3-EK connects to KSZ9021GN PHY.

The functional mode is defined by the software. PHY is configured to operate in GMII, RGMII or MII mode, according to the chosen hardware connection.

Figure 8-1. Functional Connection.

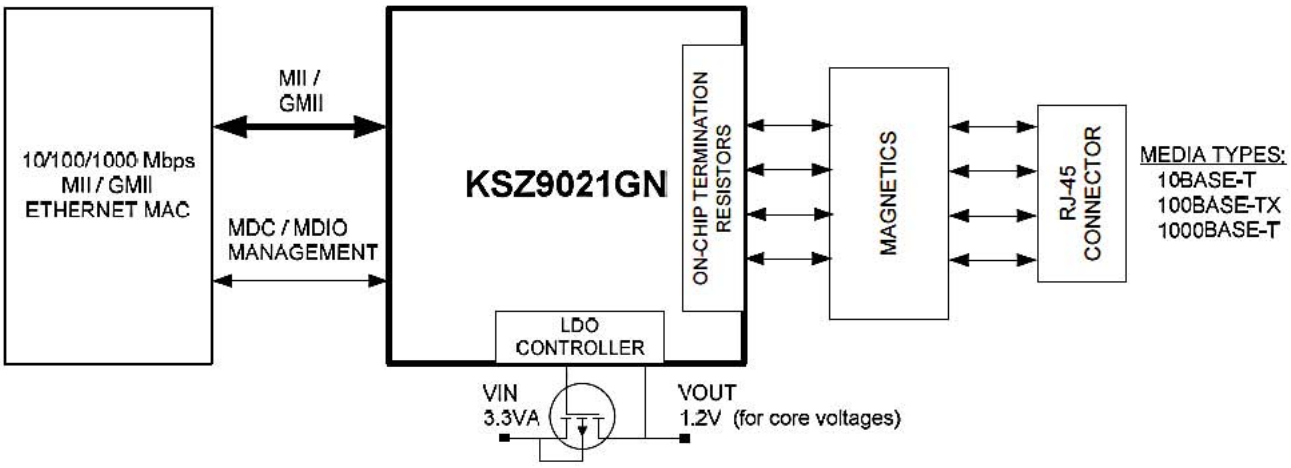
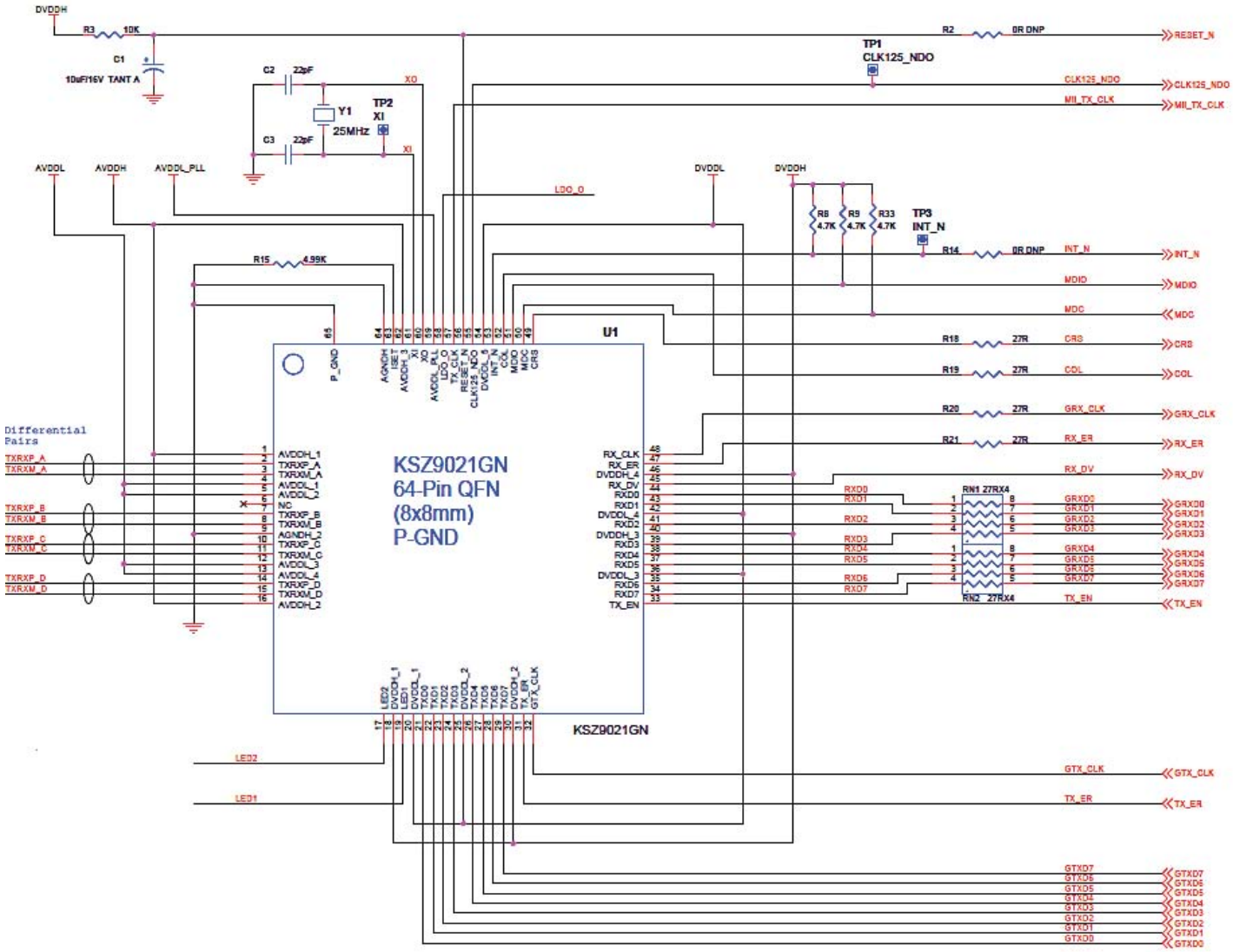


Figure 8-2. Schematics Extract of SAMA5D3-EK



Revision History

In the table that follows, the most recent version of the document appears first.

“rfo” indicates changes requested during the document review and approval loop.

Doc. Rev	Comments	Change Request Ref.
11164A	First issue.	

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